DATA SHEET

TDA4887PS
160 MHz bus-controlled monitor video preamplifier

Product specification
File under Integrated Circuits, IC02

2001 Oct 19

Philips
Semiconductors

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CONTENTS

160 MHz bus-controlled monitor video preamplifier

TDA4887PS

1 FEATURES

- 160 MHz pixel rate
- 2.7 ns rise time, 3.6 ns fall time
- I²C-bus control
- I²C-bus data buffer for synchronization of adjustments
- 8-bit Digital-to-Analog Converters (DACs)
- 200 ns input clamping pulse
- 4.6 V (p-p) output signal
- Brightness control with grey scale tracking for user-friendly performance (4 dB more than TDA4885 and TDA4886)
- Brightness control without grey scale tracking for easy alignment
- On Screen Display (OSD) mixing with 50 MHz pixel rate
- OSD contrast
- Negative feedback for DC-coupled cathodes
- Especially for AC-coupled cathodes
  - Bus controlled black level adaptable to post amplifier type
  - Internal positive feedback
  - DAC outputs for black level restoration
- Integrated black level storage capacitors
- Beam current limiting
- Subcontrast/contrast modulation
- Adjustable pedestal blanking
- Sync clipping.

2 GENERAL DESCRIPTION

The TDA4887PS is a monolithic integrated RGB preamplifier for colour monitor systems (e.g. 15" and 17") with I²C-bus control and OSD. In addition to bus control, beam current limiting and contrast modulation are possible. The IC offers brightness control with or without grey scale tracking for easy alignment. The signals are amplified to drive commonly used video modules or discrete solutions. A choice can be made between individual black level control with negative feedback from the cathode (DC coupling), or black level control with positive feedback and three DAC outputs for external cut-off control (AC coupling).

The circuit can be used with special advantages in conjunction with the TDA485x monitor deflection IC family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4887PS	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
I_P	supply current (pin 7)		–	25	30	mA
$V_{P(n)}$	supply voltage; channels 1, 2 and 3 (pins 21, 18 and 15)		7.6	8.0	8.8	V
$I_{P(n)}$	supply current; channels 1, 2 and 3 (pins 21, 18 and 15)		–	20	25	mA
$V_{i(n)(b\text{-}w)}$	input voltage; channels 1, 2 and 3 (pins 6, 8 and 10) (black-to-white value)		–	0.7	1.0	V
$V_{o(n)(b\text{-}w)(max)}$	maximum output voltage swing (black-to-white value); channels 1, 2 and 3 (pins 22, 19 and 16)	maximum contrast; maximum gain; $V_{i(n)(b\text{-}w)}$ = 0.7 V; R_L = 2 kΩ	4.2	4.6	4.9	V
$V_{o(n)}$	output voltage level (pins 22, 19 and 16)		0.1	–	$V_{P(n)}$ – 1	V
$I_{o(n)(source)(M)}$	peak output source current (pins 22, 19 and 16)	during fast positive signal transients	–40	–	–	mA
$I_{o(n)(sink)(M)}$	peak output sink current (pins 22, 19 and 16)	during fast negative signal transients	–	–	20	mA
$V_{bl(n)(ref)}$	black level reference voltage (pins 22, 19 and 16)	typical values				
	DC coupling	control bit FPOL = 0	0.5	–	2.0	V
	AC coupling	control bit FPOL = 1; no pedestal blanking	0.53	–	1.89	V
$t_{r(n)}$	rise time of fast transients at signal outputs (pins 22, 19 and 16)		–	2.7	–	ns
$t_{f(n)}$	fall time of fast transients at signal outputs (pins 22, 19 and 16)		–	3.6	–	ns
$\delta V_{o(n)}$	overshoot/undershoot at signal outputs (pins 22, 19 and 16)	input rise/fall times = 1 ns; maximum colour signal	–	–	10	%
$\alpha_{ct(f)}$	crosstalk suppression by frequency	f = 50 MHz	25	–	–	dB
δ_C	contrast control: colour signal related to maximum colour signal		–45	–	0	dB
ΔG_{track}	tracking of output colour signals of channels 1, 2 and 3	contrast control from maximum to minimum	–	0	0.5	dB
δG	gain control related to maximum gain		–13.5	–	0	dB
$\Delta V_{bl(n)}$	brightness control (difference between video black level and reference black level at signal outputs related to maximum colour signal)	control bit BRI = 0	–10	–	+33	%
$\Delta V_{DA(n)}$	brightness control range (DAC output voltages for AC coupling or internal feedback reference voltage for DC coupling)	from maximum to minimum; control bit BRI = 1	–1.4	–	0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{FB/Rn}$	DAC output voltage range without brightness control (for black level restoration) (pins 23, 20 and 17)	control bit FPOL = 1; control bit BRI = 0	3.95	–	5.75	V
$V_{OSDn(max)}$	maximum OSD colour signal related to maximum colour signal (pins 22, 19 and 16)	maximum OSD contrast; maximum gain	–	96	–	%
δ_{OC}	OSD colour signal related to maximum OSD colour signal	OSD contrast control from maximum to minimum	–12	–	0	dB

5 BLOCK DIAGRAM

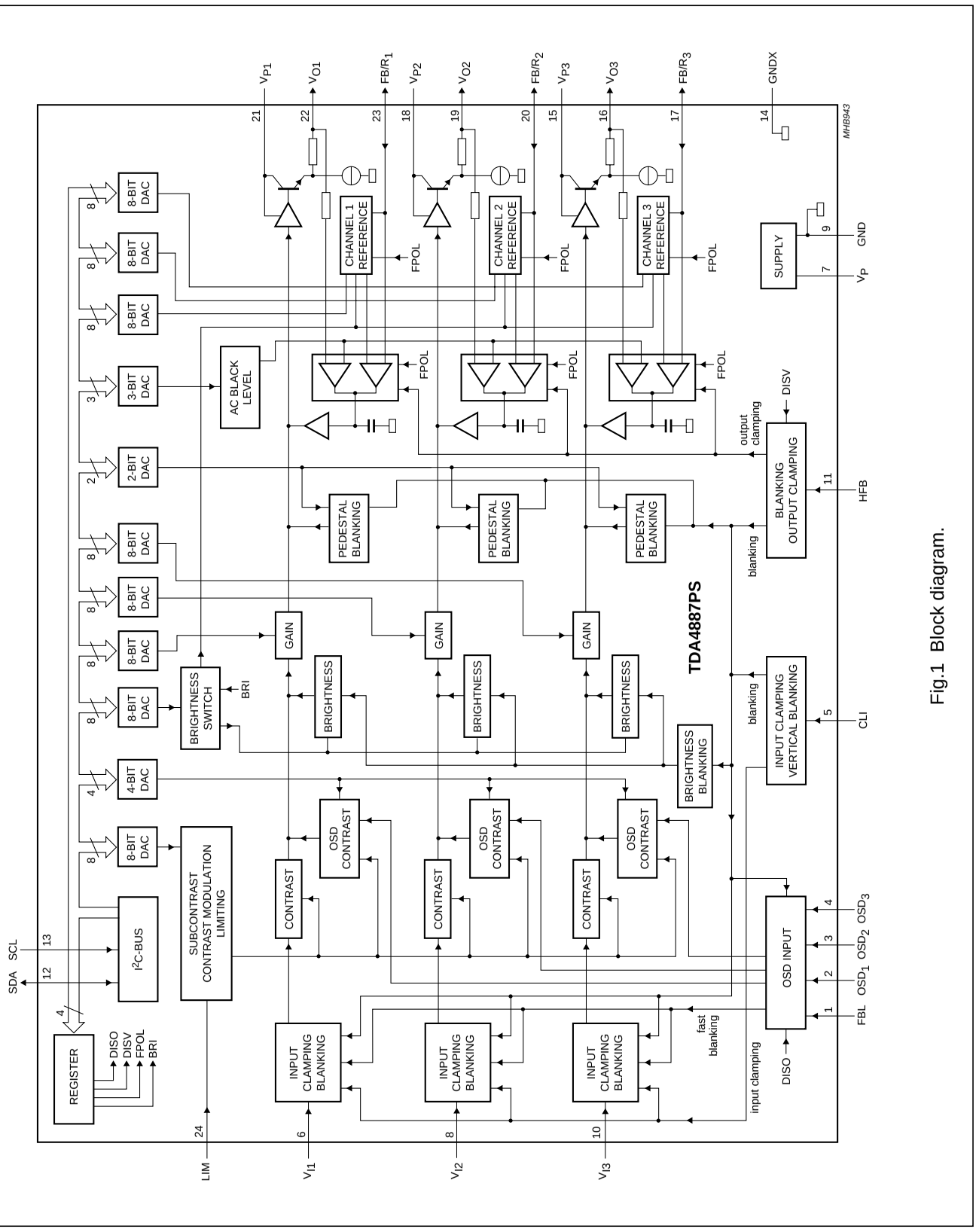


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
FBL	1	fast blanking input for OSD insertion
OSD_1	2	OSD input, channel 1
OSD_2	3	OSD input, channel 2
OSD_3	4	OSD input, channel 3
CLI	5	input clamping and vertical blanking input
V_{I1}	6	signal input, channel 1
V_P	7	supply voltage
V_{I2}	8	signal input, channel 2
GND	9	ground
V_{I3}	10	signal input, channel 3
HFB	11	output clamping and blanking input
SDA	12	I^2C-bus serial data input/output
SCL	13	I^2C-bus clock input
GNDX	14	ground signal, channels 1, 2 and 3
V_{P3}	15	supply voltage, channel 3
V_{O3}	16	signal output, channel 3
FB/R_3	17	feedback input/reference voltage output channel 3
V_{P2}	18	supply voltage, channel 2
V_{O2}	19	signal output, channel 2
FB/R_2	20	feedback input/reference voltage output, channel 2
V_{P1}	21	supply voltage, channel 1
V_{O1}	22	signal output, channel 1
FB/R_1	23	feedback input/reference voltage output, channel 1
LIM	24	subcontrast adjustment, contrast modulation and beam current limiting input

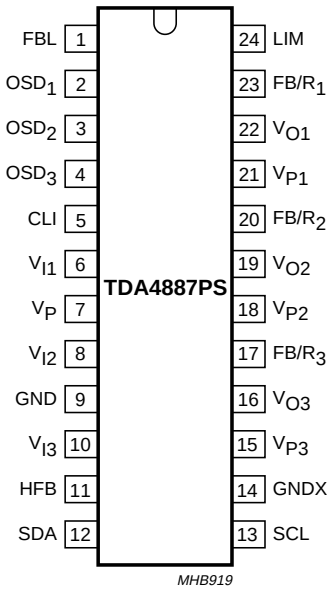


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

Refer also to block diagram (Fig.1) and definitions of levels and signals (Chapter 10).

7.1 Signal input stage

The RGB input signals are capacitively coupled into the TDA4887PS from a low-ohmic source (75 Ω recommended) and actively clamped to the internal reference black level during signal black level. The signal amplitude is $0.7V_{i(b-w)}$ and should not exceed 1 V. The high-ohmic input impedance of the TDA4887PS allows the coupling capacitor to be relatively small (10 nF recommended). The coupling capacitor also functions as a storage capacitor between clamping pulses. Very small input currents will discharge the coupling capacitor resulting in black output signals for missing input clamping pulses.

Composite signals will not disturb normal operation because a clipping circuit cuts all signal parts below black level.

A fast signal blanking circuit included in the input stage is driven by several blanking pulses (see Section 7.6) and control bit DISV = 1. During the off condition the internal reference black level is inserted instead of the input signals.

7.2 Electronic potentiometer stages

7.2.1 CONTRAST CONTROL

The contrast control is driven by an 8-bit DAC via the I^2C-bus. The input signals related to the internal reference black level can be adjusted simultaneously by contrast control with a control range of 32 dB (typical). The nominal setting is for maximum contrast.

7.2.2 BRIGHTNESS CONTROL

7.2.2.1 Brightness control with grey scale tracking

The brightness control is driven by an 8-bit DAC via the I^2C-bus; brightness control with grey scale tracking is selected when control bit BRI = 0.

With brightness control, the video black level is shifted in relation to the reference black level simultaneously for all three channels. With a negative setting (up to 10% of the maximum signal amplitude) dark signal parts will be lost in ultra black; for positive settings (up to 33% of the maximum signal amplitude) the background will alter from black to grey. At nominal brightness setting (40H) there is no shift.

The brightness setting is also valid for OSD signals. During blanking and output clamping the video black level will be blanked to the reference black level (brightness blanking). The brightness information is inserted before the gain potentiometers, background colour temperature will not change with brightness setting (grey scale tracking).

7.2.2.2 Brightness control without grey scale tracking

Brightness control without grey scale tracking is selected when control bit BRI = 1.

The brightness information will be mixed with the DAC outputs for external black level restoration (FPOL = 1, AC-coupled cathodes) or internal feedback reference voltages (FPOL = 0, DC-coupled cathodes). This allows a simple bus-controlled brightness setting without grey scale tracking. With AC-coupled cathodes this is equivalent to brightness control via grid G1.

7.2.3 GAIN CONTROL AND GREY SCALE TRACKING

The gain control is driven by an 8-bit DAC via the I^2C-bus.

Gain control is used for white point adjustment (correction for different voltage-to-light amplification of the three colour channels) and therefore individually for R, G and B. The video signals related to the reference black level can be gain-controlled within a range of 14 dB (typical). This range is large enough to accommodate the maximum output amplitude for different applications. The nominal setting is maximum gain. The gain setting is also valid for OSD signals and brightness shift (BRI = 0), therefore the complete ‘grey scale’ is effected by gain control.

7.3 Output stage

In the output stage the nominal input signal will be amplified to provide a 4.6 V (typical) output colour signal at maximum contrast and maximum gain settings. Reference or pedestal black levels are adjusted by output clamping. In order to achieve fast rise and fall times of the output signals with minimum crosstalk between the channels, each signal stage has its own supply voltage pin.

7.4 Pedestal blanking

The pedestal blanking is driven by a 2-bit DAC via the I^2C-bus. Pedestal blanking inserts a negative output level related to the reference black level (should always correspond to the 'extended cut-off voltage' at the cathode) during blanking and output clamping. In this way retrace lines during vertical flyback are suppressed (blanking to spot cut-off). The depth of pedestal blanking (voltage difference between reference black level and pedestal black level) is bus-controlled (2 bits, 0 to 13.5% of the maximum colour signal) and does not change with any other control or adjustment. The pedestal blanking level is used for output clamping instead of the reference black level (see Section 7.5). If the pedestal blanking level is the most negative output signal and if the application is for AC-coupled cathodes, a very simple black level restoration with a DC diode clamp can be used.

7.5 Output clamping and feedback references

The aim of the output clamping is to set the reference black level of the signal outputs to a value which corresponds to the 'extended cut-off voltage' of the CRT cathodes. With missing output clamping pulses the integrated storage capacitors will be discharged resulting in output signals going to switch-off voltage. If using pedestal blanking, the pedestal black level will be controlled by output clamping (see Fig.5). It is therefore not allowed to change the pedestal depth after black level adjustment of the monitor.

Feedback references are driven via the I^2C-bus and controlled by an 8-bit DAC for DC feedback references or by a 3-bit DAC for AC feedback references:

1. **DC-coupled cathodes** (control bit FPOL = 0)

   The cathode voltage is divided by a voltage divider and fed back to the IC (pins FB/R_1, FB/R_2 and FB/R_3). During the output clamping pulse it is compared with a bus-controlled feedback reference voltage with a range of approximately 5.75 to 3.95 V. Any difference will lead to a reference black level correction (subaddress 0BH = 00H) or pedestal black level correction (subaddress 0BH $\neq$ 00H) by charging or discharging the integrated capacitors that store the black level information between the output clamping pulses. The DC voltages of the output stages should be designed in such a way that the reference black level/pedestal black level is within the range of 0.5 to 2.4 V at the preamplifier output.

   For correct operation it is necessary that there is enough headroom for ultra black signals (negative brightness setting and pedestal blanking). Any clipping with the video supply voltage at the cathode can disturb the signal rise/fall times or the black level stabilization.

   After power-on, the control bit FPOL is set to logic 1 and all alignment registers are set to logic 0 resulting in the reference black level at its lowest level (0.53 V) with no output signal. Normal operation starts after all data registers have been refreshed via the I^2C-bus.

   Brightness control with grey scale tracking (control bit BRI = 0) can be used as well as brightness control without grey scale tracking (control bit BRI = 1) using the mixing function of bus-controlled brightness offset (0 to −1.4 V) to feedback reference voltages (see Section 7.2).

2. **AC-coupled cathodes** (control bit FPOL = 1)

   For applications with AC-coupled cathodes the signal outputs are fed back internally. During the output clamping pulse they are compared with a bus controlled feedback reference voltage (0.5 to 1.9 V). These values ensure a good adaptability to both discrete and integrated post amplifiers.

   For black level restoration, the DAC outputs (FB/R_1, FB/R_2 and FB/R_3) with a range of approximately 3.95 to 5.75 V can be used. Pedestal blanking is recommended because it allows use of a simple restoration circuit. After power-on, the DAC outputs will be at maximum output voltage (register value logic 0), so when using a non-inverting amplifier for the reference voltages the monitor will start with black.

   Brightness control with grey scale tracking (control bit BRI = 0) can be used as well as simple brightness control without grey scale tracking (control bit BRI = 1) using the mixing function of bus controlled brightness offset (0 to −1.4 V) to DAC output voltages (see Section 7.2).

7.6 Clamping and blanking pulses

There are two pins for clamping and blanking purposes (pins CLI and HFB):

1. **Pin CLI** (input clamping, vertical blanking)

   The pin CLI of TDA4887PS can be connected directly to pin CLBL of e.g. TDA4855 sync processor for input clamping pulses and vertical blanking pulses.

   Input clamping pulses and blanking pulses are completely separated from the sandcastle input, that means there is normally (outside detected vertical blanking) no blanking during input clamping and the clamping pulse is not suppressed during vertical blanking.

   The input pulse is scanned with two thresholds:

   a) 1.4 V (typical) for vertical blanking

   b) 3 V (typical) for input clamping.

   In order to separate the vertical blanking pulse from the sandcastle pulse it is necessary that the input clamping pulse has rise/fall times faster than 75 ns/V during the transition from 1.2 to 3.5 V and vice versa. The leading edge of the internal vertical blanking pulse is delayed by typically 270 ns (after the end of an input clamping pulse or the beginning of a separate blanking pulse), the trailing edge is delayed by typically 115 ns.

   During the vertical blanking pulse signal blanking, brightness blanking and pedestal blanking will be activated. In buffered mode, the leading edge of the internal vertical blanking pulse is used to synchronize data transmitted via the I^2C-bus (see Section 7.10.1).

   For correct input clamping the input signals have to be at black level during the input clamping pulse.

2. **Pin HFB** (output clamping and blanking)

   The input pulse (e.g. horizontal flyback pulse) is scanned with two thresholds. If the input pulse exceeds the first threshold (typically 1.4 V) signal blanking, brightness blanking and pedestal blanking will be activated. If the input pulse exceeds the second threshold (typically 3 V) output clamping will be activated additionally.

   Especially for applications with DC-coupled cathodes (FPOL = 0), it is useful that the leading edge of the (internal) clamping pulse is slightly delayed with respect to the leading edge of the (internal) blanking pulse in order to avoid initial misclamping due to the delay of the feedback signal from the cathodes.

7.7 On Screen Display insertion and OSD contrast

On Screen Display (OSD) insertion and OSD contrast are controlled by a 4-bit DAC driven via the I^2C-bus.

If the fast blanking input signal at pin FBL exceeds the threshold (typically 1.4 V) the input signals are blanked (signal blanking) and OSD signals are enabled. Then, any signal at pins OSD_1, OSD_2 or OSD_3 exceeding the same threshold will create an insertion signal with an amplitude of 100% of the maximum colour signal. The amplitude can be controlled by OSD contrast (driven via the I^2C-bus) with a range of 12 dB. The OSD signals are inserted at the same point as the contrast-controlled input signals and will be treated with brightness and gain control as with normal input signals.

Identical pulses at OSD signal input pins and FBL have to be handled very carefully. Each difference in pulse delay at the inputs will produce glitches at pulse edges at signal outputs.

When control bit DISO = 1 the OSD signal insertion and fast blanking (pin FBL) are disabled.

7.8 Subcontrast adjustment, contrast modulation and beam current limiting

The pin LIM is a linear contrast control pin which allows subcontrast setting, contrast modulation and beam current limiting. The maximum contrast is defined by the actual I^2C-bus setting. Input signals at pin LIM act on video and OSD signals and do not affect the contrast bit resolution. If the pin is not used it should be decoupled with a capacitor or tied to the supply voltage.

7.8.1 Beam current limiting

The open-circuit voltage is approximately 5 V, contrast reduction starts at input voltages <4.4 V (typical) and signal amplification will be reduced with descending input voltages. The input resistance of pin LIM is very high to make it possible to choose a time constant sufficient for the open-circuit voltage to recover through the application.

7.8.2 Subcontrast

In order to fit the maximum signal amplification to the post amplifier gain, an input voltage of <4.4 V can be used.

7.8.3 Contrast modulation

To achieve brightness uniformity over the screen, scan dependent contrast modulation is possible. The nominal input voltage should be <4.4 V having enough margin for positive and negative modulation.

7.9 I²C-bus control

The TDA4887PS contains an I²C-bus receiver for several control functions:

- Contrast register with control bits BRI, FPOL, DISV and DISO
- Brightness control with 8-bit DAC
- Contrast control with 8-bit DAC
- OSD contrast control with 4-bit DAC
- Gain control for each channel with 8-bit DAC
- Internal feedback reference and external reference voltage control for each channel with 8-bit DAC
- Black level for AC coupling with 3-bit DAC
- Depth of pedestal blanking with 2-bit DAC.

After power-up and after internal power-on reset of the I²C-bus, the registers are set to the following values (for most applications these settings guarantee a black screen after power-up):

- Control bit FPOL set to logic 1
- Control bits BRI, DISV and DISO set to logic 0
- All other alignment registers set to logic 0 (minimum value for control registers).

After an intermediate power dip, all registers are set to their initial values and an internal Power-on reset bit will be set with the consequence that the device will give no acknowledge on the data byte after being first addressed. The Power-on reset bit will be reset if the control register is addressed. It is recommended to then refresh all registers by using the auto-increment function.

7.10 I²C-bus data buffer

7.10.1 BUFFERED MODE

Adjustments via the I²C-bus are synchronized with vertical blanking pulse at CLI:

- Most significant bit (MSB) of subaddress is set to logic 1
- Only one I²C-bus transmission in buffered mode is accepted before the start of the vertical blanking pulse; following transmissions receive no acknowledge
- Received data is stored in one internal 8-bit buffer
- Adjustments will take effect with detection of the first vertical blanking pulse after the end of the acknowledged I²C-bus transmission
- Waiting for vertical blanking pulse in buffered mode can be interrupted by Power-on reset
- Auto-increment is not possible
- Buffered mode should be used for user adjustments such as contrast, OSD contrast and brightness when a picture is visible on the monitor.

7.10.2 DIRECT MODE

Adjustments via the I²C-bus take effect immediately:

- Most significant bit (MSB) of subaddress is set to logic 0
- Number of I²C-bus transmissions in direct mode is unlimited
- Adjustments take effect directly at the end of each I²C-bus transmission
- Direct mode can be used for all adjustments but large changes of control values may appear as visual disturbances in the picture on the monitor
- Auto-increment is possible
- Vertical blanking pulse is not necessary.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)		0	8.8	V
$V_{P(n)}$	supply voltage; channels 1, 2 and 3 (pins 21, 18 and 15)		0	8.8	V
$V_{i(n)}$	input voltage; channels 1, 2 and 3 (pins 6, 8 and 10)		−0.1	V_P	V
V_{ext}	external DC voltage applied to				
	pins 1 to 4		−0.1	V_P	V
	pins 5 and 11		−0.1	V_P + 0.7	V
	pins 12 and 13		−0.1	V_P	V
	pins 23, 20 and 17		−0.1	V_P + 0.7	V
	pins 22, 19 and 16		note 1	note 1	
	pin 24		−0.1	V_P	V
$I_{o(n)(av)}$	average output current; channels 1, 2 and 3 (pins 22, 19 and 16)		–	20	mA
$I_{o(n)(M)}$	peak output current channels 1, 2 and 3 (pins 22, 19 and 16)		–	50	mA
P_{tot}	total power dissipation		–	1400	mW
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	ambient temperature		−20	+70	°C
T_j	junction temperature		−25	+150	°C
V_{ESD}	electrostatic handling voltage for all pins				
	machine model	note 2	−250	+250	V
	human body model	note 3	−3000	+3000	V

Notes

1. No external voltages.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH inductance (*“SNW-FQ-302B”*).
3. Equivalent to discharging a 100 pF capacitor via a 1500 Ω series resistor (*“SNW-FQ-302A”*).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		5	K/W

10 CHARACTERISTICS

All voltages and currents are measured in a dedicated test circuit (see Fig.17) optimized for best high frequency performance; all voltages are measured with respect to GND (pins 9 and 14); $V_P = V_{P1,2,3} = 8$ V (pins 7, 21, 18 and 15); $T_{amb} = 25$ °C; nominal input signals [0.7 V (p-p) at pins 6, 8 and 10]; maximum colour signals at signal outputs (pins 22, 19 and 16); reference black level ($V_{bl(ref)}$) approximately 0.7 V; nominal setting for brightness; maximum settings for OSD contrast, contrast and gain; no subcontrast, modulation of contrast or limiting ($V_{LIM} \geq 5$ V); no OSD fast blanking (pin 1 connected to ground); notes 1 to 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage (pin 7)		7.6	8.0	8.8	V
$V_{P(SO)}$	supply voltage threshold at pin 7 at which signal outputs are switched off	note 1	6.8	7.0	7.2	V
I_P	supply current (pin 7)	note 4	–	25	30	mA
$V_{P(n)}$	supply voltage; channels 1, 2 and 3 (pins 21, 18 and 15)		7.6	8.0	8.8	V
$I_{P(n)}$	supply current; channels 1, 2 and 3 (pins 21, 18 and 15)	pins 22, 19 and 16 open-circuit; $V_{bl(n)(ref)} = 0.7$ V; notes 4 and 5	–	20	25	mA
Input clamping and vertical blanking input, validation of buffered I²C-bus data (CLI; pin 5)						
V_{CLI}	input clamping and vertical blanking input signal	notes 6 and 7				
		no vertical blanking, no input clamping	–0.1	–	+1.2	V
		vertical blanking, no input clamping	1.6	–	2.6	V
		input clamping, no vertical blanking	3.5	–	V_P	V
I_{CLI}	input current	$V_{CLI} = 1$ V	–	–0.2	–	µA
		pin 5 connected to ground; note 8	–80	–45	–30	µA
		$V_{CLI} = -0.1$ V; note 8	–250	–135	–100	µA
$t_{r/f5}$	rise/fall time for input clamping pulse; disable for vertical blanking	note 6; see Fig.7	–	–	75	ns/V
$t_{W(CLI)}$	width of input clamping pulse		200	–	–	ns
$t_{W(I2C)(valid)}$	width of vertical blanking pulse for validation of buffered I²C-bus data	leading and trailing edge threshold $V_{CLI} = 1.4$ V; note 7	10	–	–	µs
$t_{d(I2C)(valid)}$	delay between leading edge of vertical blanking pulse and validation of buffered I²C-bus data	I²C-bus buffered mode transmission completed; leading edge threshold $V_{CLI} = 1.4$ V; note 7; see Fig.7	–	–	2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{dead(I2C)}$	I^2C-bus receiver dead time after synchronizing vertical blanking pulse following a completed I^2C-bus buffered mode transmission	leading edge threshold V_{CLI} = 1.4 V; note 7	15	–	–	µs
t_{dl5}	delay between leading edges of vertical blanking input pulse and signal blanking at signal outputs	V_{HFB} < 0.8 V; input pulse rising and falling edges = 50 ns/V; threshold for vertical blanking with rising edge V_{CLI} = 1.4 V; threshold for vertical blanking with falling edge V_{CLI} = 3 V; see Fig.7	–	270	–	ns
t_{dt5}	delay between trailing edges of vertical blanking input pulse and signal blanking at signal outputs	V_{HFB} < 0.8 V; input pulse falling edge = 50 ns/V; threshold V_{CLI} = 1.4 V; see Fig.7	–	115	–	ns
Output clamping and blanking input (HFB; pin 11)						
V_{HFB}	output clamping and blanking input signal	note 9				
		no blanking, no output clamping	–0.1	–	+0.8	V
		blanking, no output clamping	2	–	2.6	V
		blanking, output clamping	3.5	–	V_P	V
I_{HFB}	input current	V_{HFB} = 0.8 V	–	–0.4	–	µA
		pin 11 connected to ground; note 8	–80	–45	–30	µA
		V_{HFB} = –0.1 V; note 8	–250	–135	–100	µA
$t_{W(HFB)}$	width of output clamping pulse	V_{HFB} = 3 V	1	–	–	µs
Video signal inputs; channels 1, 2 and 3 (pins 6, 8 and 10)						
$V_{i(n)(b-w)}$	input voltage; black-to-white value (pins 6, 8 and 10)		–	0.7	1.0	V
$I_{i(n)}$	DC input current (pins 6, 8 and 10)	no input clamping; $V_{i(n)} = V_{i(n)(clamp)}$; T_{amb} = –20 to +70 °C	0.02	0.20	0.35	µA
		during input clamping; $V_{i(n)} = V_{i(n)(clamp)}$ ±0.7 V	±350	±420	±500	µA
Signal blanking						
$\alpha_{ct(blank)}$	crosstalk suppression from input to output during blanking	control bit DISV = 1; f = 80 MHz	20	–	–	dB
		control bit DISV = 1; f = 120 MHz	10	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clipping of negative input signals (measured at signal outputs)						
ΔV_{clipp}	offset during sync clipping related to maximum colour signal	$V_{i(n)} = V_{i(n)(clamp)}$; sync amplitude = 0.3 V; note 10; see Fig.3	–	0.6	1.2	%
Contrast control; see Fig.8 and note 11						
δ_C	colour signal related to maximum colour signal	FFH (maximum)	–	0	–	dB
		00H (minimum)	–	–45	–	dB
ΔG_{track}	tracking of output colour signals of channels 1, 2 and 3	FFH to 40H; note 12	–	0	0.5	dB
Fast blanking (pin 1) and OSD signal insertion; channels 1, 2 and 3 (pins 2, 3 and 4); note 13						
V_{FBL}	fast blanking input signal (pin 1)	no video signal blanking; OSD signal insertion disabled	0	–	1.1	V
		video signal blanking; OSD signal insertion enabled	1.7	–	V_P	V
V_{OSDn}	OSD input signal (pins 2, 3 and 4)	V_{FBL} > 1.7 V				
		no internal OSD signal insertion	0	–	1.1	V
		internal OSD signal insertion	1.7	–	V_P	V
$t_{r(OSDn)}$	rise time of OSD colour signals (pins 22, 19 and 16)	10 to 90% amplitude; pulse leading edge = 1.2 ns/V	–	3	4	ns
$t_{f(OSDn)}$	fall time of OSD colour signals (pins 22, 19 and 16)	90 to 10% amplitude; pulse falling edge = 1.2 ns/V	–	4	7	ns
$t_{g(n)(CO)}$	width of (negative going) OSD signal insertion glitch, leading edge (pins 22, 19 and 16)	identical pulses at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4)	0	4	6	ns
$t_{g(n)(OC)}$	width of (negative going) OSD signal insertion glitch, trailing edge (pins 22, 19 and 16)	identical pulses at fast blanking input (pin 1) and OSD signal inputs (pins 2, 3 and 4)	0	5	6	ns
δV_{OSDn}	overshoot/undershoot of OSD colour signal related to actual OSD output pulse amplitude (pins 22, 19 and 16)	pulse with 1.2 ns/V at OSD signal inputs (pins 2, 3 and 4)	–	6	10	%
$V_{OSDn(max)}$	maximum OSD colour signal related to maximum colour signal (pins 22, 19 and 16)	maximum OSD contrast; maximum gain	90	96	110	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OSD contrast control; see Fig.9 and note 14						
δ_{OC}	OSD colour signal related to maximum OSD colour signal	0FH (maximum)	–	0	–	dB
		00H (minimum)	–14	–12	–10	dB
Subcontrast adjustment, contrast modulation and beam current limiting (pin 24); see Fig.8 and note 15						
$V_{LIM(nom)}$	nominal input voltage	pin 24 open-circuit	4.7	5.0	5.3	V
$V_{LIM(start)}$	starting voltage for linear contrast and OSD contrast reduction		4.2	4.4	4.8	V
$V_{LIM(stop)}$	stop voltage for linear contrast and OSD contrast reduction	–40 dB below maximum colour signal (contrast setting FFH)	1.5	2.0	2.5	V
B_{LIM}	bandwidth of contrast modulation	–3 dB	4	–	–	MHz
$I_{LIM(max)}$	maximum input current	V_{LIM} = 0 V	–1	–	+1	µA
Brightness control; see Figs 10, 12 and 14 and notes 16 and 17						
$\Delta V_{bl(n)}$	difference between video black level and reference black level at signal outputs related to maximum colour signal	FFH (maximum); BRI = 0	28	33	38	%
		40H (nominal); BRI = 0	–2	0	+2	%
		00H (minimum); BRI = 0	–12	–10	–8	%
$\Delta V_{DA(n)}$	DAC output voltage shift (pins 23, 20 and 17)	FPOL = 1, see DAC output voltages for AC coupling or feedback reference voltage shift; FPOL = 0, see internal feedback reference voltage for DC coupling				
		FFH (maximum); BRI = 1	–	–1.4	–	V
		00H (minimum); BRI = 1	–	0	–	V
Gain control; see Fig.11 and note 18						
δ_G	video signal related to video signal at maximum gain	FFH (maximum)	–	0	–	dB
		00H (minimum)	–15	–13.5	–12.5	dB
Pedestal blanking; see Fig.5 and note 19						
$\Delta V_{bl(n)(PED-VID)}$	difference between pedestal black level and video black level at nominal brightness, measured at signal outputs (pins 22, 19 and 16) related to maximum colour signal	03H (maximum)	–12	–13.5	–	%
		02H	–8	–9	–	%
		01H	–4	–4.5	–	%
		00H (minimum)	–	0	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Signal outputs; channels 1, 2 and 3 (pins 22; 19 and 16)						
$V_{o(n)(min)}$	minimum output voltage level (pins 22, 19 and 16)		0.01	0.05	0.1	V
$V_{o(n)(max)}$	maximum output voltage level (pins 22, 19 and 16)	arbitrary input signals, contrast, brightness and gain adjustments; without load	$V_{P(n)} - 2$	–	$V_{P(n)} - 1$	V
$I_{o(n)(source)(max)}$	maximum output source current (pins 22, 19 and 16)		–15	–	–	mA
$R_{o(n)}$	output resistance (pins 22, 19 and 16)		65	75	90	Ω
$V_{o(n)(b-w)(max)}$	maximum output voltage swing (black-to-white value); channels 1, 2 and 3 (pins 22, 19 and 16)	maximum contrast; maximum gain; $V_{i(n)(b-w)}$ = 0.7 V; R_L = 2 kΩ	4.2	4.6	4.9	V
$I_{o(n)(source)(M)}$	peak output source current (pins 22, 19 and 16)	during fast positive signal transients	–40	–	–	mA
$I_{o(n)(sink)(M)}$	peak output sink current (pins 22, 19 and 16)	during fast negative signal transients	–	–	20	mA
S/N	signal-to-noise ratio	note 20	48	–	–	dB
Frequency response at signal outputs; channels 1, 2 and 3 (pins 22, 19 and 16)						
$t_{r(n)}$	rise time of fast transients (pins 22, 19 and 16)	input rise time = 1 ns; 10 to 90% amplitude; R_L = 10 kΩ; notes 21, 22 and 23;				
		2.8 V (p-p) signal amplitude; C_L = 5 pF	–	2.7	3.8	ns
		4.5 V (p-p) signal amplitude; C_L = 5 pF	–	3.2	4.2	ns
		4.5 V (p-p) signal amplitude; C_L = 11 pF	–	3.8	4.5	ns
$t_{f(n)}$	fall time of fast transients (pins 22, 19 and 16)	input fall time = 1 ns; 90 to 10% amplitude; R_L = 10 kΩ; notes 21, 22 and 23;				
		2.8 V (p-p) signal amplitude; C_L = 5 pF	–	3.6	4.5	ns
		4.5 V (p-p) signal amplitude; C_L = 5 pF	–	3.6	4.5	ns
		4.5 V (p-p) signal amplitude; C_L = 11 pF	–	5	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\delta V_{o(n)}$	overshoot of output signal pulse related to actual output pulse amplitude (pins 22, 19 and 16)	input rise time = 1 ns; maximum colour signal	–	–	10	%
	undershoot of output signal pulse related to actual output pulse amplitude (pins 22, 19 and 16)	input fall time = 1 ns; maximum colour signal	–	–	10	%
Crosstalk at signal outputs; channels 1, 2 and 3 (pins 22, 19 and 16)						
$\alpha_{ct(tr)(n)}$	transient crosstalk suppression (pins 22, 19 and 16)	input rise/fall time = 1 ns; note 24	10	–	–	dB
$\alpha_{ct(f)}$	crosstalk suppression by frequency	f = 50 MHz; note 25	25	–	–	dB
		f = 100 MHz; note 25	10	–	–	dB
Internal feedback reference voltage for DC coupling; see Fig.12 and note 26						
$V_{ref(DC)}$	internal reference voltage for negative feedback polarity (without brightness control)	FFH; FPOL = 0; BRI = 0	3.7	3.95	4.1	V
		00H; FPOL = 0; BRI = 0	5.6	5.75	5.9	V
	internal reference voltage for negative feedback polarity (with brightness control, see also brightness control $\Delta V_{DA(n)}$)	FFH; FPOL = 0; BRI = 1; maximum brightness	2.3	2.55	2.7	V
		00H; FPOL = 0; BRI = 1; minimum brightness	5.6	5.75	5.9	V
Output clamping, feedback inputs for DC coupling; FB/R_1, FB/R_2 and FB/R_3 (pins 23, 20 and 17)						
$I_{FB/Rn(max)}$	maximum input current (pins 23, 20 and 17)	during output clamping; V_{HFB} > 3.5 V; $V_{FB/Rn}$ = 0.5 V; FPOL = 0	–500	–200	–60	nA
$V_{bl(n)(ref)(min)}$	minimum reference black level/minimum pedestal black level (pins 22, 19 and 16)	V_{HFB} > 3.5 V; FPOL = 0	0.01	0.1	0.5	V
$V_{bl(n)(ref)(max)}$	maximum reference black level/maximum pedestal black level (pins 22, 19 and 16)	V_{HFB} > 3.5 V; FPOL = 0	2.0	2.8	4.0	V
$\Delta V_{bl(CRT)}$	black level variation at CRT	FPOL = 0; note 27	–	–	200	mV
$\Delta V_{bl(n)(lf)}$	black level decrease between clamping pulses related to maximum colour signal (pins 22, 19 and 16)	FPOL = 0; f_{line} = 60 kHz; δ = 10%	–	0.1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output clamping; internal feedback (of signal outputs) reference voltage for AC coupling; see Fig.13 and note 28						
$V_{bl(n)(ref)}$	reference black level voltage/pedestal black level voltage (pins 22, 19 and 16)	V_{HFB} > 3.5 V; FPOL = 1				
		00H (minimum)	0.47	0.53	0.59	V
		0FH (maximum)	1.83	1.89	1.95	V
DAC output voltages for AC coupling; FB/R_1, FB/R_2 and FB/R_3 (pins 23, 20 and 17); see Fig.14 and note 29						
$V_{FB/Rn}$	DAC output voltage (without brightness control)	FFH; FPOL = 1; BRI = 0	3.7	3.95	4.1	V
		00H; FPOL = 1; BRI = 0	5.6	5.75	5.9	V
	DAC output voltage (with brightness control, see also brightness control $\Delta V_{DA(n)}$)	FFH; FPOL = 1; BRI = 1; maximum brightness	2.3	2.55	2.7	V
		00H; FPOL = 1; BRI = 1; minimum brightness	5.6	5.75	5.9	V
$R_{FB/Rn}$	output resistance	FPOL = 1	–	100	–	Ω
$I_{FB/Rn(sink)(max)}$	maximum sink current	FPOL = 1	–	–	400	µA
$I_{FB/Rn(source)(max)}$	maximum source current	FPOL = 1	–	–200	–	µA
I^2C-bus inputs; SDA (pin 12), SCL (pin 13); note 30						
f_{SCL}	SCL clock frequency		–	–	100	kHz
V_{IL}	LOW-level input voltage		0	–	1.5	V
V_{IH}	HIGH-level input voltage		3	–	5	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–10	–	–	µA
I_{IH}	HIGH-level input current	V_{IH} = 5 V	–10	–	–	µA
V_{OL}	LOW-level output voltage	during acknowledge	0	–	0.4	V
$I_{SDA(ack)}$	SDA output current (pin 12) during acknowledge	V_{OL} = 0.4 V	3	–	–	mA
		V_{OL} = 0.6 V	6	–	–	mA
$t_{o(f)}$	output fall time	V_{SDA} = 3 to 1.5 V; bus capacitance C_{SDA} = 400 pF	–	–	250	ns
$V_{th(POR)(r)}$	threshold for Power-on reset on	rising supply voltage	–	1.5	2.0	V
		falling supply voltage	–	3.5	–	V
$V_{th(POR)(f)}$	threshold for Power-on reset off	rising supply voltage	–	–	7	V
		falling supply voltage	–	1.5	–	V

Notes to the characteristics

1. Definition of levels (see Figs 3 to 5)

   Reference black level: this is the level to which the input level is clamped during the input clamping pulse (V_{CLI} > 3.5 V). It is used internally as a reference for the gain settings. It can be observed on the outputs:

   a) When the input is at black and the brightness setting is nominal (subaddress 01H = 40H) or control bit BRI = 1

   b) During output blanking and clamping (V_{HFB} > 3.5 V) if the pedestal blanking depth is set to zero (subaddress 0BH = 00H).

   Video black level: this is the black level of the actual video. At the input it is still equal to the reference black level. At the output it may deviate from it according to the brightness setting. Contrast setting leaves the video black level unaltered. Gain setting biases the video black level due to its influence on brightness. This is important for correct grey scale tracking. It can be observed at the outputs when the input is at black outside output blanking and clamping pulses (V_{HFB} < 0.8 V).

   Pedestal black level: this is an ultra black level which deviates from the reference black level by a bus controlled amount. It can be observed at the output during output blanking and clamping (V_{HFB} > 3.5 V; subaddress 0BH ≠ 00H).

   Switch-off voltage: this is the lowest signal voltage at outputs. The signals will be switched off by discharging the internal black level storage capacitors if the supply voltage is less than $V_{P(SO)}$. It can be observed at the outputs when the input is at black, the brightness setting is nominal and V_P < 6.8 V (subaddress 01H = 40H).

   Blanking level: this level equals reference black (subaddress 0BH 1= 00H) or pedestal black. It can be observed at the outputs during output blanking and clamping (V_{HFB} > 3.5 V).

2. Explanation to black level adjustment:

   The three reference black levels are aligned correctly when they are made equal to the ‘extended cut-off levels’ of the three cathodes. Full raster and spot cut-off can only be achieved by enabling the pedestal blanking or by applying a negative pulse to the grid G1.

   Negative feedback for DC-coupled cathodes (control bit FPOL = 0): the actual blanking level on the outputs depends on the external feedback application for output clamping. The loop will function correctly only if it is within the control range of $V_{bl(n)(ref)(min)}$ to $V_{bl(n)(ref)(max)}$ at pins 22, 19 and 16. It should be noted that changing pedestal blanking in a given application will not affect the blanking level, but instead shifts the video (and needs re-alignment of the three black levels).

   Positive feedback for AC-coupled cathodes (control bit FPOL = 1): the feedback loop for output clamping is closed internally. The actual blanking level is bus controlled between 0.53 and 1.89 V (subaddress 0AH). It should be noted that changing pedestal blanking will not affect the blanking level, but instead shifts the video (and re-alignment of the three black levels is needed).

3. Definition of output signals (see Fig.6):

   Colour signal: all positive voltages are referenced to black level at signal outputs.

   Maximum colour signal: colour signal with nominal input signal $0.7V_{i(b-w)}$, maximum contrast setting and maximum gain setting.

   Video signal: all positive voltages referred to reference black level at signal outputs. The video signal is the superimposing of the brightness information (ΔV_{bl}) and the colour signal.

4. The total supply current $I_{P(tot)} = I_P + I_{P1} + I_{P2} + I_{P3}$ depends on the supply voltage with a factor of approximately 4.4 mA/V and varies in the temperature range from −20 to +70 °C by approximately ±5% ($V_{O(n)}$ = 0.7 V).

5. The channel supply current I_{P1}, I_{P2}, I_{P3} depends on the signal output current I_{O1}, I_{O2}, I_{O3}, the channel supply voltage V_{P1}, V_{P2}, V_{P3} and the signal output voltage V_{O1}, V_{O2}, V_{O3}. With $I_{Px} = I_{P(n)}$ at $I_{O(n)}$ = 0, $V_{P(n)}$ = 8 V and $V_{O(n)}$ = 0.7 V:

   $$I_{P(n)} \approx I_{Px} + I_{O(n)} + 4.4\ \text{mA/V} \times (V_{P(n)} - 8\ \text{V}) - 1\ \text{mA/V} \times (V_{O(n)} - 0.7\ \text{V})$$

6. Pin 5 should be used for input clamping and blanking during vertical retrace (signal blanking, brightness blanking and pedestal blanking). With a fast clamping pulse (transition between V_{CLI} = 1.2 to 3.5 V and 3.5 to 1.2 V in less than 75 ns/V) no blanking will occur during input clamping.

   For 75 ns/V < $t_{r/f5} \leq$ 280 ns/V the generation of the internal blanking pulse is uncertain. For $t_{r/f5}$ > 280 ns/V the internal blanking pulse will be generated.

   If pin 5 is open-circuit, it will activate permanent input clamping and undefined blanking.

7. Pin 5 can be used to synchronize all adjustments via the I²C-bus (one by one). With a completed I²C-bus transmission in buffered mode, only the leading edge of a vertical blanking pulse activates an adjustment (see also Section 7.10).

   After the adjustment has been activated (validation of buffered I²C-bus data) the I²C-bus will be reset and further transmissions in direct or buffered mode are enabled.

   I²C-bus transmissions in direct mode need no synchronization pulses.

8. Input voltages less than −0.1 V can produce internal substrate currents which disturb the leakage currents at the signal inputs. An internal protection circuit creates a current for pin voltages of approximately 0 V or with negative voltage. Feeding clamping and blanking pulses via a resistor (several kΩ) protects the pin from negative voltages.

9. Pin 11 should be used for output clamping and/or blanking. If pin 11 is open-circuit, it will activate permanent blanking and output clamping.

10. Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below input reference black level (see Fig.3).

11. Contrast control acts on internal colour signals under I²C-bus control; subaddress 02H (bit resolution 0.4% of contrast range).

12. $$\Delta G_{track} = 20 \times \text{maximum of} \left\{ \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2}\right) \right| \left| \log\left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3}\right) \right| \left| \log\left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3}\right) \right| \right\} \text{dB}$$

    A_n: colour signal output amplitude in channel n = 1, 2 or 3 at any contrast setting.
    A_{n0}: colour signal output amplitude in channel n = 1, 2 or 3 at maximum contrast setting and same gain setting.

13. When OSD fast blanking is active and OSD inputs OSD_1, OSD_2 and OSD_3 are HIGH (V_{FBL} > 1.7 V, $V_{OSD(n)}$ > 1.7 V) the OSD colour signals will be inserted in front of the gain potentiometers. This ensures a correct grey scale of all video signals. The amplitudes of the inserted OSD signals can be controlled simultaneously by OSD contrast via the I²C-bus.

    The inserted black level change (ΔV_{bl}) due to brightness control is not affected by OSD fast blanking.

14. OSD contrast control acts on inserted OSD colour signals under I²C-bus control; subaddress 03H (bit resolution 6.7% of OSD contrast range).

15. This pin can be used for subcontrast adjustment, beam current limiting and contrast modulation. Both the video and OSD contrast are reduced simultaneously (see Figs 8 and 9). Because of the high-ohmic input impedance the pin should be tied to a voltage of more than 5 V or decoupled with a capacitor (several nF) if not used.

16. Brightness control adds an I²C-bus controlled DC offset to the internal colour signal; subaddress 01H (bit resolution 0.4% of brightness range). When control bit BRI = 1 the internal gain dependent brightness control is switched off and the feedback reference voltages (control bit FPOL = 0) or DAC output voltages for DC restoration (control bit FPOL = 1) at the cathodes are shifted with brightness control.

17. The voltage difference between video black level and reference black level is related to the colour signal (see note 3) with nominal 0.7 V (p-p) input signal, at maximum contrast (subaddress 02H = FFH) and for any gain setting. This voltage difference (in Volts) is proportional to the gain setting (grey scale tracking). Therefore ΔV_{bl} (in percent) is constant for any gain setting. The given values of ΔV_{bl} are valid only for video black levels higher than the minimum output voltage level $V_{o(n)(min)}$.

18. Gain control acts on video signals and inserted OSD video signals under I²C-bus control; subaddress 04H (channel 1), 05H (channel 2) and 06H (channel 3; bit resolution 0.4% of gain range respectively).
19. Pedestal blanking produces an ultra black level during blanking and output clamping which is the most negative signal at the signal output pins. The pedestal depth can be selected by bus control, subaddress 0BH. The reference black level which should correspond to the 'extended cut-off voltage' at the cathodes is approximately $\Delta V_{bl(n)(PED-VID)}$ higher (see Fig.5). The use of pedestal blanking with AC-coupled cathodes (control bit FPOL = 1) allows a very simple black level restoration with a DC diode clamp instead of a complicated pulse restoration circuit.
20. The signal-to-noise ratio is calculated using the formula (range 1 to 120 MHz):

$$\frac{S}{N} = 20 \times \log \frac{\text{peak-to-peak value of the maximum signal output voltage}}{\text{RMS value of the noise output voltage}} \text{ dB}$$

21. The following formula can be used to approximately determine the output rise/fall time for any input rise/fall time other than 1 ns: $t^2_{r/f,\ measured} = t^2_{r/f\ (22,19,16)} + (t^2_{r/f,\ input} - [1\ ns]^2)$
22. The relationship between pixel rate and signal bandwidth is $f_{-3dB} = 0.75 \times f_{pixel}$, which is a compromise between excellent and acceptable video performance. The calculation of the pixel-related rise and fall times can be done using the formula $t_{r/f} = \frac{0.35}{f_{-3dB}} = \frac{0.35}{0.75 \times f_{pixel}}$. Although this formula is valid for low-pass filters of first order only it is used in most cases for simplified estimations. The pixel rate $f_{pixel} = \frac{0.35}{0.75 \times t_r}$ is a good approximation for many filter types.
23. Rise and fall times depend on signal amplitude, temperature, external load, black level and supply voltage. The rise time is affected if the top level of the signal pulse approaches the maximum output voltage level (high black level, large signal amplitude or low supply voltage). The fall time depends on the black level (increase with decreasing black level) and on large capacitive loads. Low-ohmic pull-down loads at the outputs helps towards smaller fall times. Rise and fall times increase with increasing ambient (or crystal) temperature. At maximum operating temperature, rise and fall times are approximately 0.4 ns longer than at T_{amb} = 25 °C.
24. Transient crosstalk between any two output pins:
    a) **Input conditions**: any channel (channel A) with nominal input signal and 1 ns rise time. The inputs of the other two channels (channels B) are capacitively coupled to ground. Gain setting at maximum (FFH). Contrast setting at maximum (FFH). No limiting/modulation of contrast ($V_{LIM} \geq 4.8$ V)
    b) **Output conditions**: black level set to approximately 0.7 V for each channel at signal outputs. Output signals are V_A and V_B respectively
    c) **Transient crosstalk suppression**: $\alpha_{ct(tr)} = 20 \times \log \frac{V_A}{V_B}$ dB
25. Crosstalk by frequency between any two output pins:
    a) **Input conditions**: any channel (channel A) with 0.2 V (p-p) sinusoidal input signal, DC-coupled to approximately 4.3 V, no input clamping. The inputs of the other two channels (channels B) are capacitively coupled to ground. Gain setting at maximum (FFH). Contrast setting at maximum (FFH). No limiting/modulation of contrast ($V_{LIM} \geq 4.8$ V)
    b) **Output conditions**: control bit FPOL = 1, subaddress 0AH set to 01H, no pedestal blanking, nominal brightness setting. Output signals are V_A and V_B respectively
    c) **Crosstalk suppression**: $\alpha_{ct(f)} = 20 \times \log \frac{V_A}{V_B}$ dB

26. **Control bit FPOL = 0**: the internal feedback reference voltages for DC control act under I²C-bus control; subaddress 07H (channel 1), 08H (channel 2) and 09H (channel 3); bit resolution 0.4% of voltage range. Rising values of the data bytes, e.g. 00H to FFH, correspond to rising values of the resulting reference black levels at signal outputs (pins 22, 19 and 16). The internal feedback reference voltages can be measured at feedback inputs (pins 23, 20 and 17) during output clamping (V_{HFB} > 3.5 V) in closed feedback loop. The feedback loop remains operative at reference black levels between the specified values of $V_{o(n)bl(ref)(min)}$ and $V_{o(n)bl(ref)(max)}$.

    Control bit BRI = 1: the internal feedback reference voltages can be shifted under I²C-bus control which allows easy brightness control without grey scale tracking (see Section 7.2.2.2); subaddress 01H (bit resolution 0.4% of voltage shift range). The superimposition of internal feedback reference and brightness control leads to a voltage output range of 5.8 to 2.5 V.

27. Slow variations of video supply voltage V_{CRT} will be suppressed at the CRT cathode by the clamping feedback loop. A change of V_{CRT} with 5 V leads to a specified change of the cathode voltage.

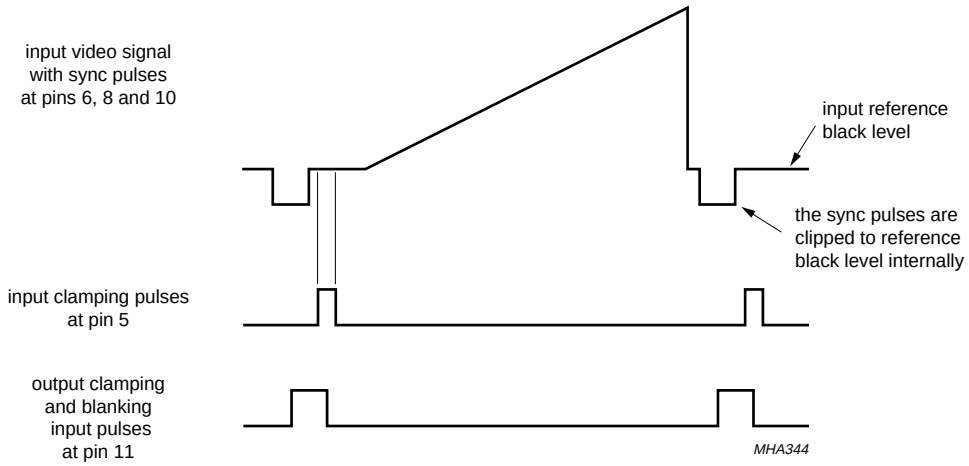
28. To adapt to different types of post amplifier, the internal feedback reference voltage for AC coupling (control bit FPOL = 1) acts under I²C-bus control; subaddress 0AH (bit resolution 14.29%). The internal feedback reference voltage can be measured at signal outputs (pins 22, 19 and 16) during output clamping (V_{HFB} > 3.5 V); reference black level or pedestal black level.

29. The DAC output voltages act under I²C-bus control for control bit FPOL = 1; subaddress 07H (FB/R_1), 08H (FB/R_2) and 09H (FB/R_3); bit resolution 0.4% of voltage range respectively. Using an inverting amplifier for DC restoration, rising values of the data bytes, e.g. 00H to FFH, correspond to changing the light output from dark to bright.

    With control bit BRI = 1 the DAC output voltages can be shifted under I²C-bus control which allows easy brightness control without grey scale tracking (see Section 7.2.2.2); subaddress 01H (bit resolution 0.4% of voltage shift range). The superimposition of black level control and brightness control leads to a voltage output range of 5.8 to 2.5 V.

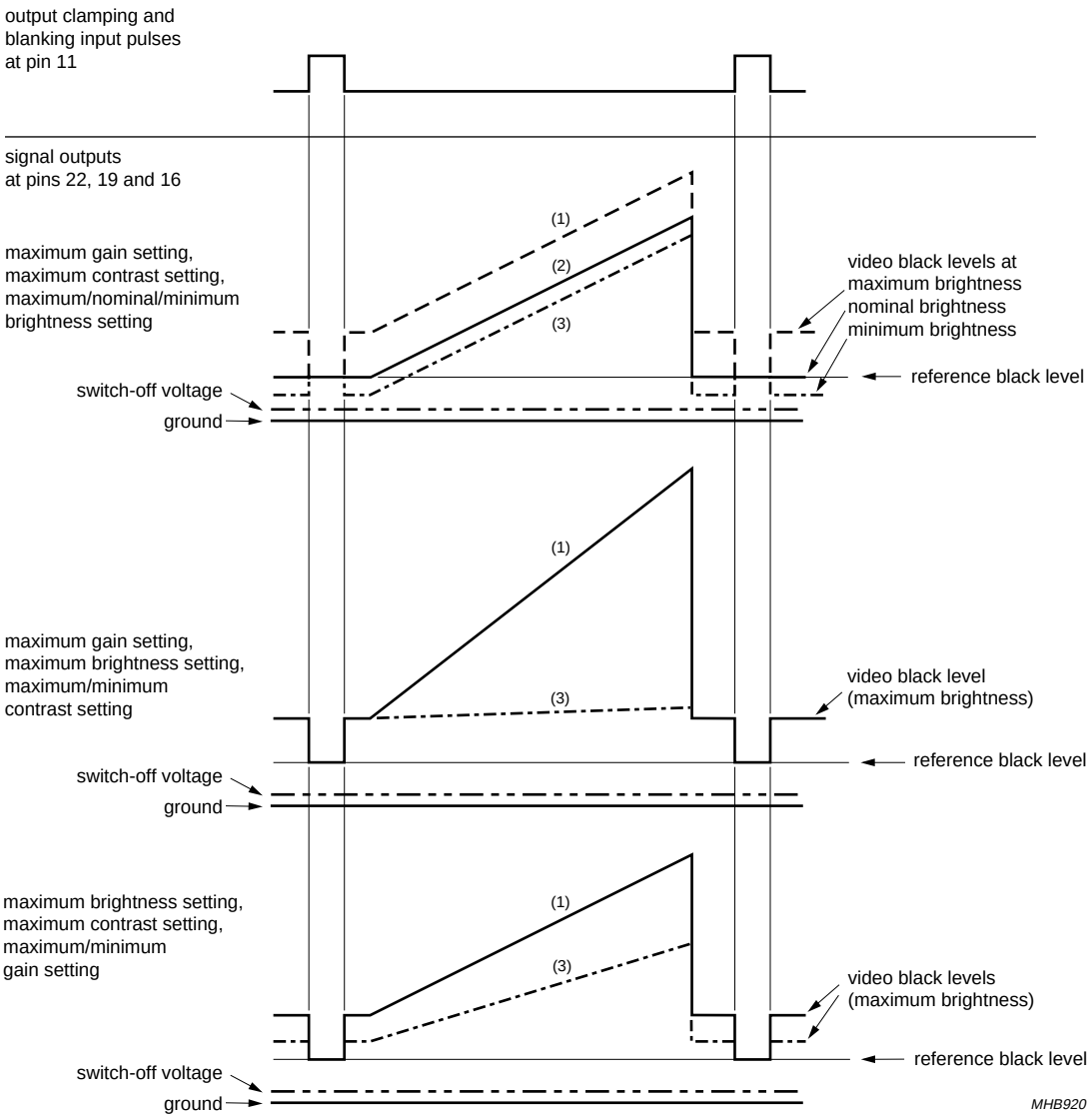
30. All adjustments via the I²C-bus can be synchronized with vertical blanking pulse at pin CLI. This is called I²C-bus transmission in buffered mode. Conversely the adjustments via the I²C-bus will take effect immediately in direct mode.

    The timing of I²C-bus transmissions in buffered mode is related to the vertical blanking. See Section 7.6 and note 7 for specification of vertical blanking input (pin 5).



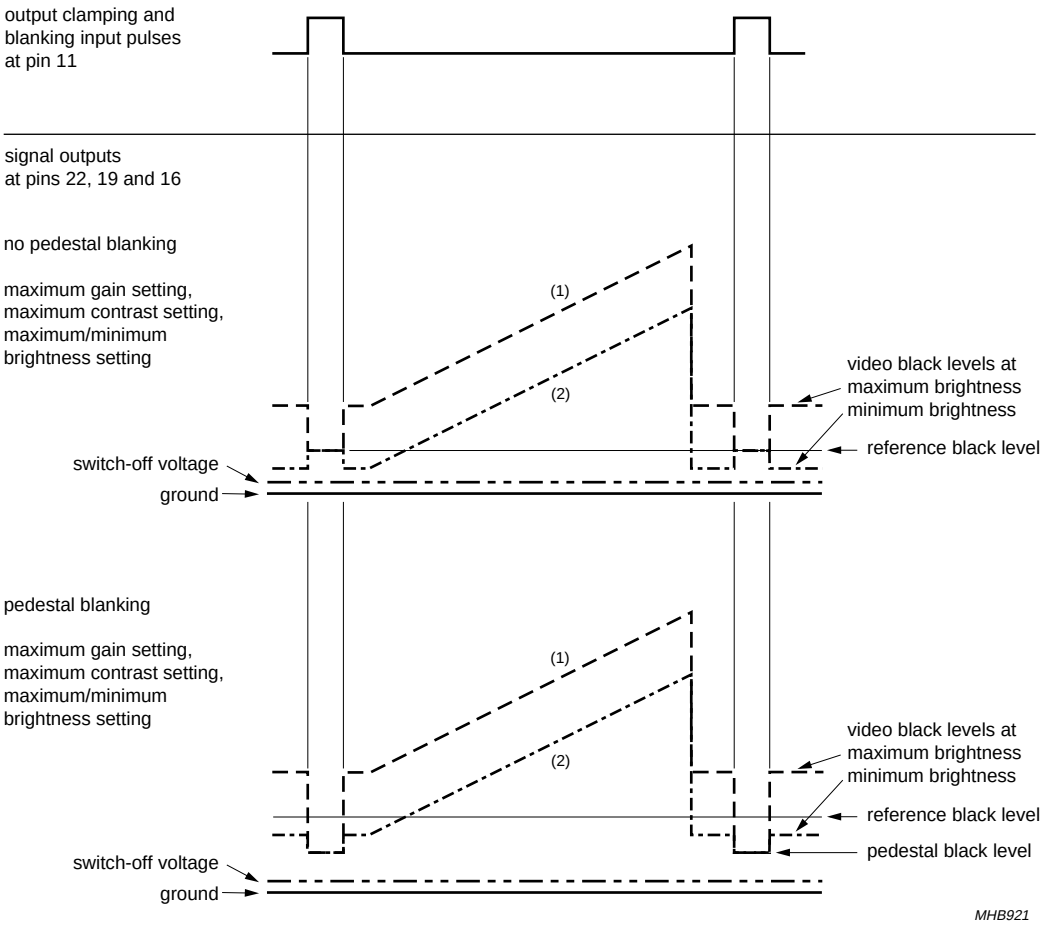
The input video signals have to be at black level during input clamping.

Fig.3 Definition of input signals.



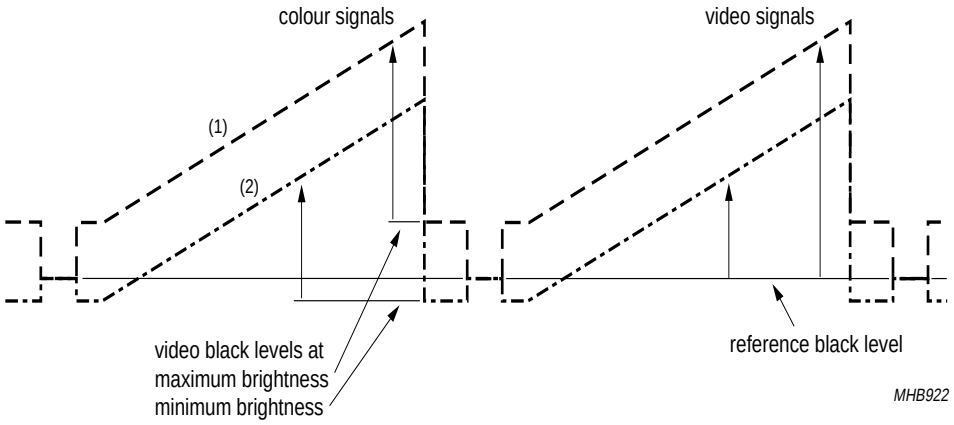
(1) Maximum.
(2) Nominal.
(3) Minimum.

Fig.4 Definition of levels and functions of brightness, contrast and gain with no pedestal blanking.



(1) Maximum.
(2) Minimum.

Fig.5 Output signals with and without pedestal blanking.



(1) Maximum brightness setting.
(2) Minimum brightness setting.

Fig.6 Definition of output signals at pins 22, 19 and 16: maximum gain setting, maximum contrast setting and no pedestal blanking.

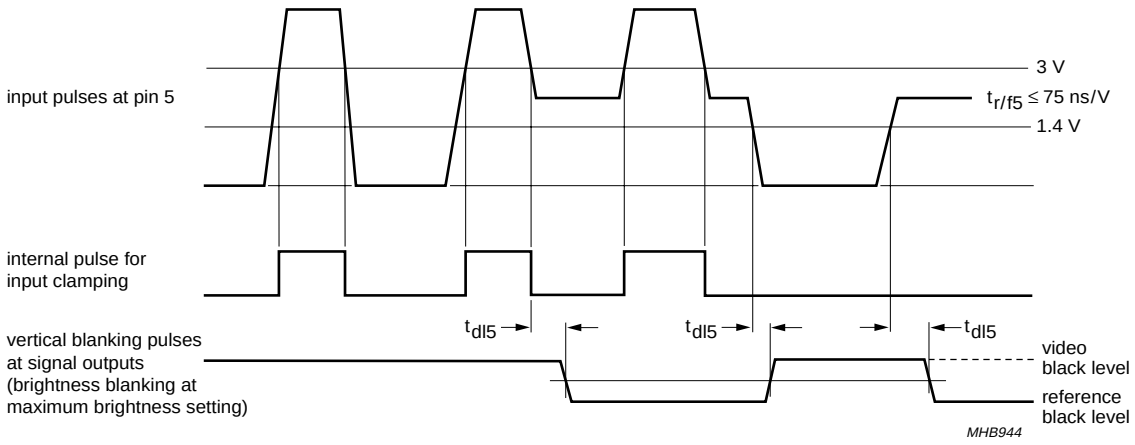
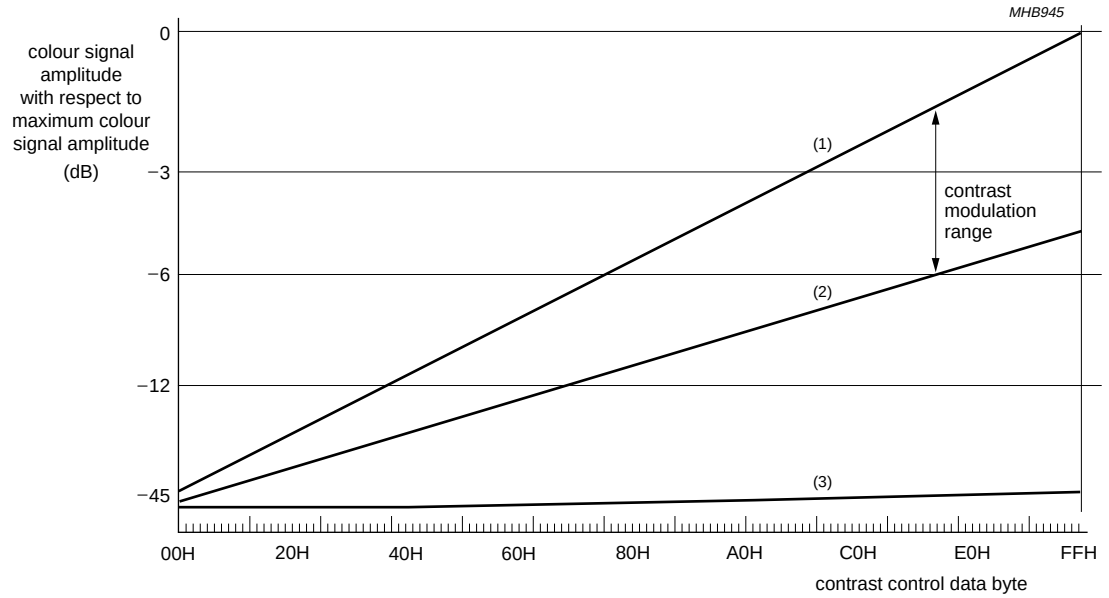
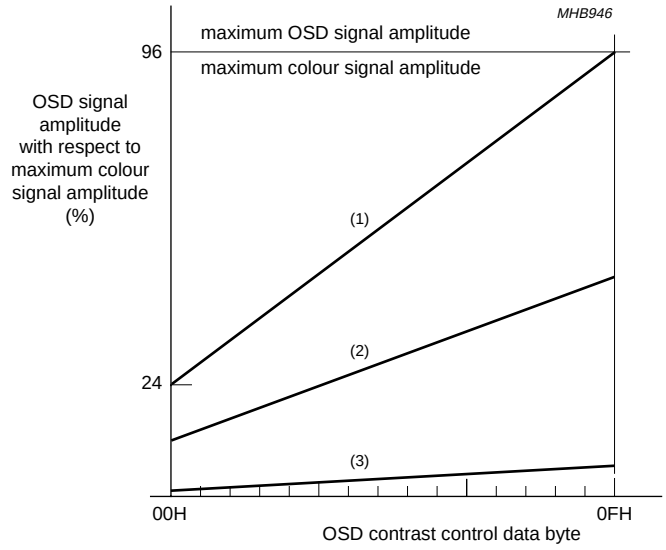


Fig.7 Timing of pulses at pin 5 and derived pulses at maximum brightness setting.



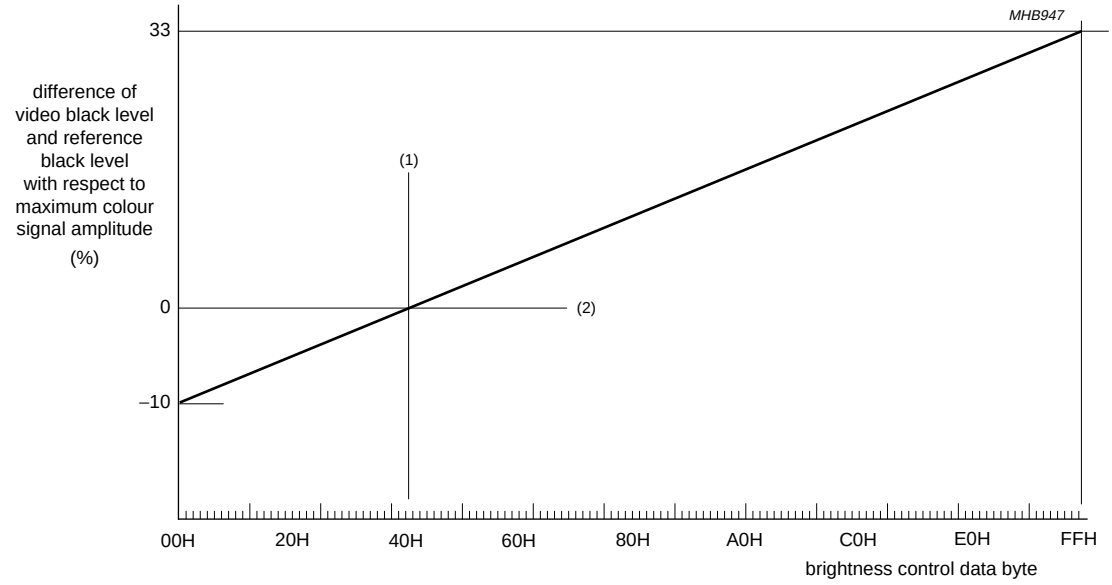
(1) No contrast reduction.
(2) Partial contrast reduction by subcontrast, limiting or contrast modulation.
(3) Full contrast reduction by subcontrast, limiting or contrast modulation.

Fig.8 Contrast control characteristic with subcontrast, limiting or contrast modulation.



(1) No OSD contrast reduction.
(2) Partial OSD contrast reduction by subcontrast, limiting or contrast modulation.
(3) Full OSD contrast reduction by subcontrast, limiting or contrast modulation.

Fig.9 OSD contrast control characteristic with subcontrast, limiting or contrast modulation.



(1) Nominal adjustment.
(2) Nominal brightness reference black level.

Fig.10 Brightness control characteristic; control bit BRI = 0.

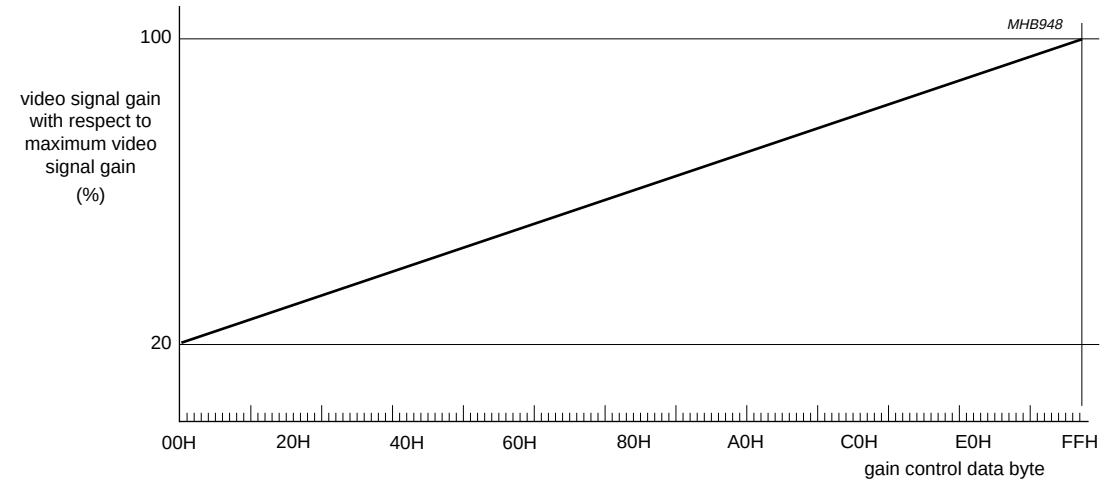
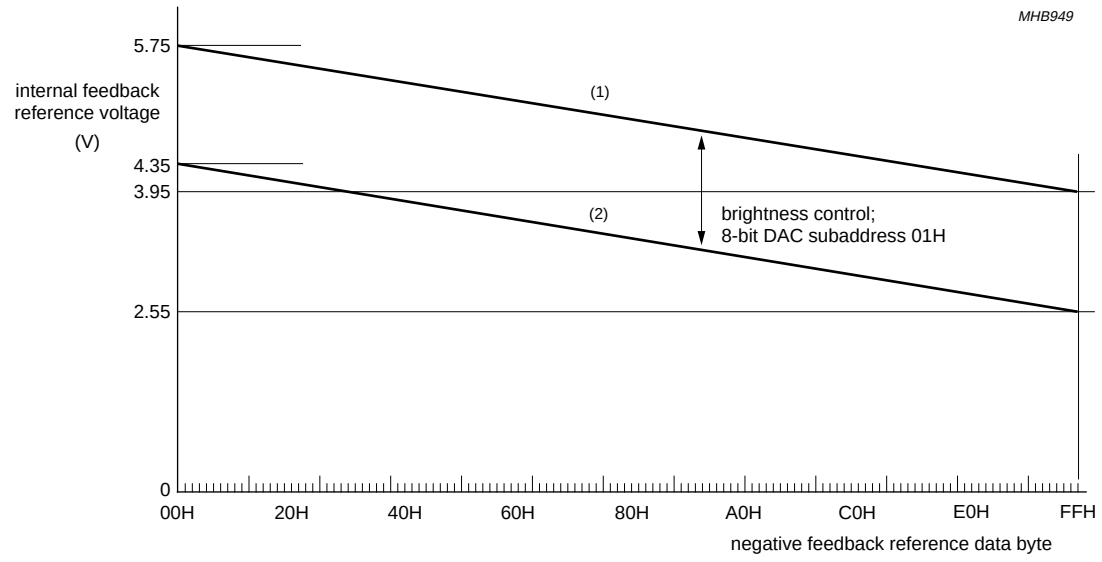


Fig.11 Gain control characteristic.



(1) Control bit BRI = 0 or control bit BRI = 1 and minimum brightness setting (subaddress 01H at 00H).
(2) Control bit BRI = 1 and maximum brightness setting (subaddress 01H at FFH).

Fig.12 Internal feedback reference voltages for negative feedback (FPOL = 0).

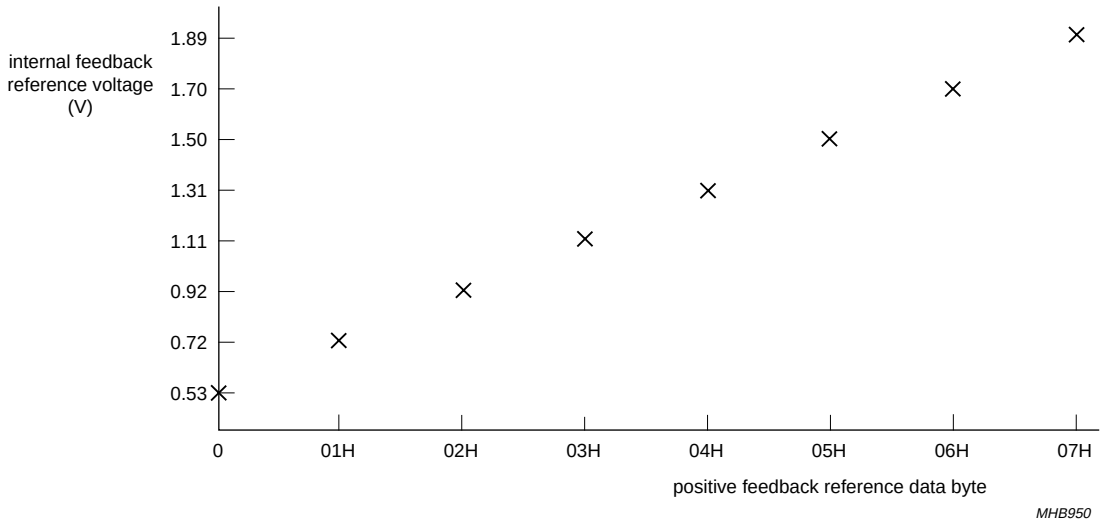
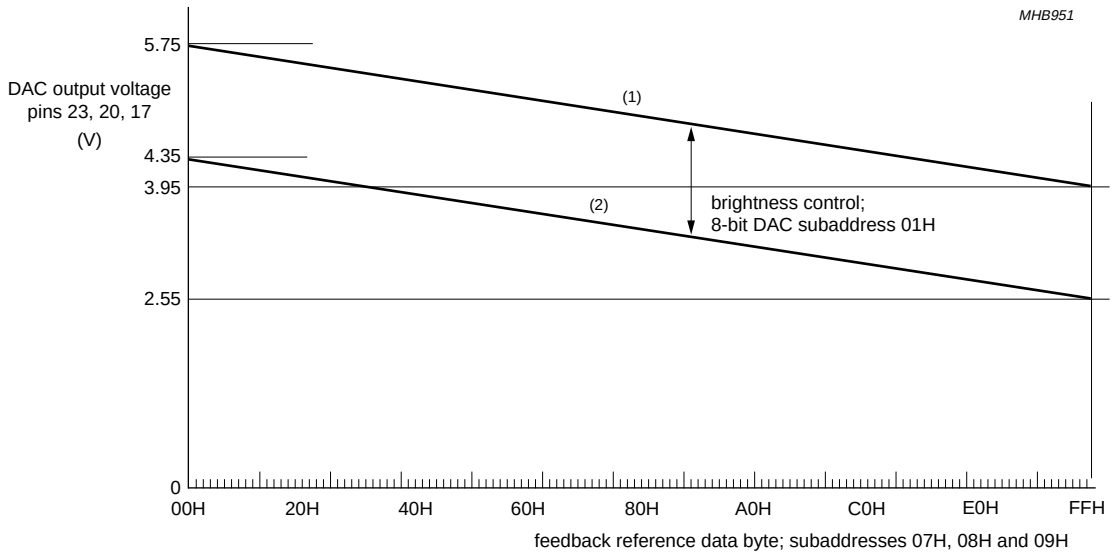


Fig.13 Internal feedback reference voltages for positive feedback (FPOL = 1).



(1) Control bit BRI = 0 or control bit BRI = 1 and minimum brightness setting (subaddress 01H at 00H).

(2) Control bit BRI = 1 and maximum brightness setting (subaddress 01H at FFH).

Fig.14 DAC output voltages (control bit FPOL = 1).

11 I²C-BUS PROTOCOL

Table 1 Slave address

A6(1)	**A5**(1)	**A4**(1)	**A3**(1)	**A2**(1)	**A1**(1)	**A0**(1)	$\overline{\mathbf{W}}$(2)
1	0	0	0	1	0	0	0

Notes

1. Address bit.
2. Write bit.

Table 2 Slave receiver format

S(1)	SLAVE ADDRESS A(2)	SUBADDRESS(3) A	DATA BYTE(4) A	P(5)

Notes

1. START condition.
2. A = acknowledge.

   After an intermediate power dip all registers are set to their initial values (see note 3 at Table 4) and an internal power-on reset bit will be set with the consequence that the device will give no acknowledge on the data byte after a first addressing. The power-on reset bit will be reset if the control register is addressed. It is recommended to then refresh all registers by using the auto-increment function.
3. All subaddresses within the range 00H to 0BH are automatically incremented. The subaddress counter wraps around from 0BH to 00H. For subaddresses within the range 80H to 8FH no auto-increment takes place. Subaddresses outside the ranges 00H to 0BH and 80H to 8BH are acknowledged by the device but no auto-increment or any other internal operation takes place.
4. Single data byte in case of no auto-increment of subaddresses. More than one data byte with auto-increment of subaddresses.
5. STOP condition.

Table 3 Subaddress byte format

FUNCTION	SUBADDRESS[1]		SUBADDRESS BYTE							
	DIRECT MODE	BUFFERED MODE	S7[2]	S6[2]	S5[2]	S4[2]	S3[2]	S2[2]	S1[2]	S0[2]
Control register	00H	80H	B[3]	0	0	0	0	0	0	0
Brightness control	01H	81H	B[3]	0	0	0	0	0	0	1
Contrast control	02H	82H	B[3]	0	0	0	0	0	1	0
OSD contrast control	03H	83H	B[3]	0	0	0	0	0	1	1
Gain control channel 1	04H	84H	B[3]	0	0	0	0	1	0	0
Gain control channel 2	05H	85H	B[3]	0	0	0	0	1	0	1
Gain control channel 3	06H	86H	B[3]	0	0	0	0	1	1	0
Black level reference channel 1	07H	87H	B[3]	0	0	0	0	1	1	1
Black level reference channel 2	08H	88H	B[3]	0	0	0	1	0	0	0
Black level reference channel 3	09H	89H	B[3]	0	0	0	1	0	0	1
Black level for AC coupling	0AH	8AH	B[3]	0	0	0	1	0	1	0
Depth of pedestal blanking	0BH	8BH	B[3]	0	0	0	1	0	1	1
	0CH to 0FH	8CH to 8FH	not used							

Notes

1. The most significant bit (MSB) of the subaddress enables an I^2C-bus transmission in direct or in buffered mode (see note 3). Subaddresses outside the ranges 00H to 0FH and 80H to 8FH are not used.
2. Subaddress bit.
3. Most significant bit of subaddress byte. I^2C-bus transmission in **direct mode: B = 0**. I^2C-bus transmission in **buffered mode: B = 1**.

Table 4 Subaddress and data byte format

FUNCTION	SUBADDRESS(1)		DATA BYTE(2)								NOMINAL VALUE(3)
	DIRECT MODE	BUFFERED MODE	D7(4)	D6(4)	D5(4)	D4(4)	D3(4)	D2(4)	D1(4)	D0(4)	
Control register	00H	80H	X(5)	BRI	X(5)	X(5)	FPOL	DISV	DISO	X(5)	08H
Brightness control	01H	81H	A17	A16	A15	A14	A13	A12	A11	A10	40H
Contrast control	02H	82H	A27	A26	A25	A24	A23	A22	A21	A20	FFH
OSD contrast control	03H	83H	X(5)	X(5)	X(5)	X(5)	A33	A32	A31	A30	0FH
Gain control channel 1	04H	84H	A47	A46	A45	A44	A43	A42	A41	A40	FFH
Gain control channel 2	05H	85H	A57	A56	A55	A54	A53	A52	A51	A50	FFH
Gain control channel 3	06H	86H	A67	A66	A65	A64	A63	A62	A61	A60	FFH
Black level reference channel 1	07H	87H	A77	A76	A75	A74	A73	A72	A71	A70	–
Black level reference channel 2	08H	88H	A87	A86	A85	A84	A83	A82	A81	A80	–
Black level reference channel 3	09H	89H	A97	A96	A95	A94	A93	A92	A91	A90	–
Black level for AC coupling	0AH	8AH	X(5)	X(5)	X(5)	X(5)	X(5)	AA2	AA1	AA0	–
Depth of pedestal blanking	0BH	8BH	X(5)	X(5)	X(5)	X(5)	X(5)	X(5)	AB1	AB0	00

Notes

1. See Table 3 (Subaddress byte format).
2. The least significant bit (LSB) of an analog alignment register is defined as AX0 (data bit D0).
3. Under certain conditions the nominal values lead to nominal colour signals, etc. (see notes 1 and 3 of Chapter “Characteristics” and Figs 4 to 6).

   After power-up and after internal Power-on reset of the I^2C-bus the registers are set to the following values:

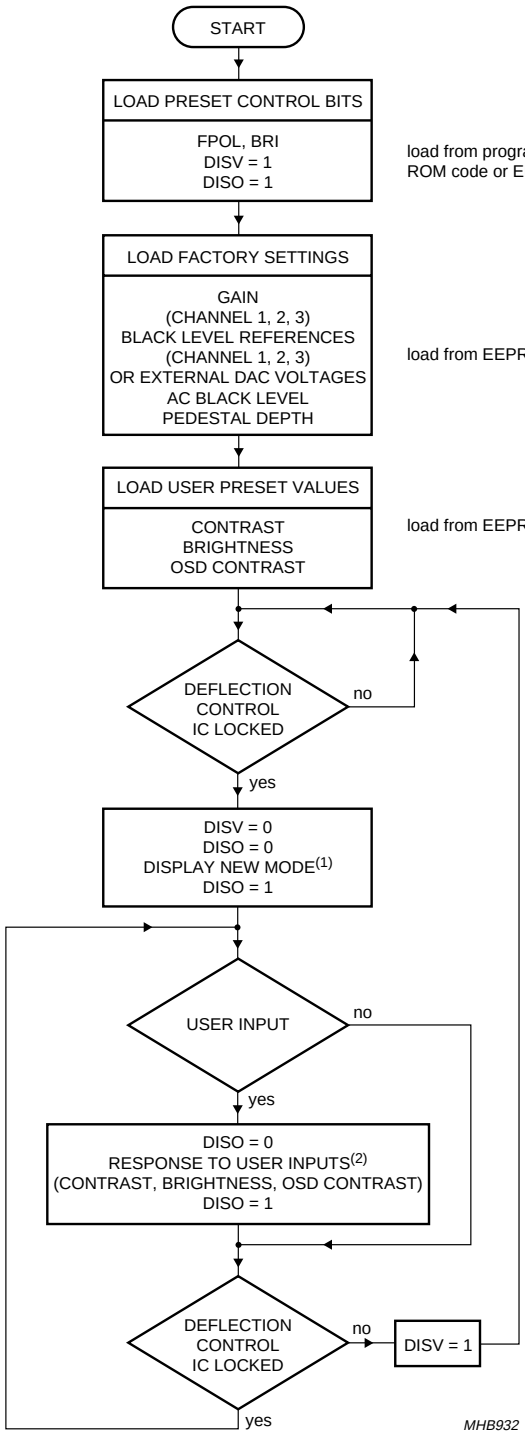
   a) Control bit FPOL to logic 1.

   b) Control bits DISV, DISO and BRI to logic 0.

   c) All other alignment registers to logic 0 (minimum value for control registers).
4. Data bit.
5. X means don’t care but the bits are preferably set to logic 0 for software compatibility with other video ICs that have the same slave address.

Table 5 Control register

BIT	FUNCTION
DISO = 0	OSD signals enabled
DISO = 1	OSD signals disabled
DISV = 0	video signals enabled
DISV = 1	video signals disabled
FPOL = 0	negative feedback polarity; pins 23, 20 and 17 as feedback inputs; no external DAC voltage outputs
FPOL = 1	positive feedback polarity; pins 23, 20 and 17 as external DAC voltage outputs; internal feedback of signal outputs
BRI = 0	internal brightness control with grey scale tracking
BRI = 1	Brightness control without grey scale tracking. With FPOL = 0 the brightness information is combined with the internal feedback reference voltages. With FPOL = 1 the brightness information is combined with the DAC output voltages for DC restoration at the cathodes.



(1) Only synchronized video should be displayed. Each new mode can be displayed by OSD.

(2) Data transmission should be synchronized with vertical blanking of the monitor.

Fig.15 I^2C-bus control flow chart.

12 TEST AND APPLICATION INFORMATION

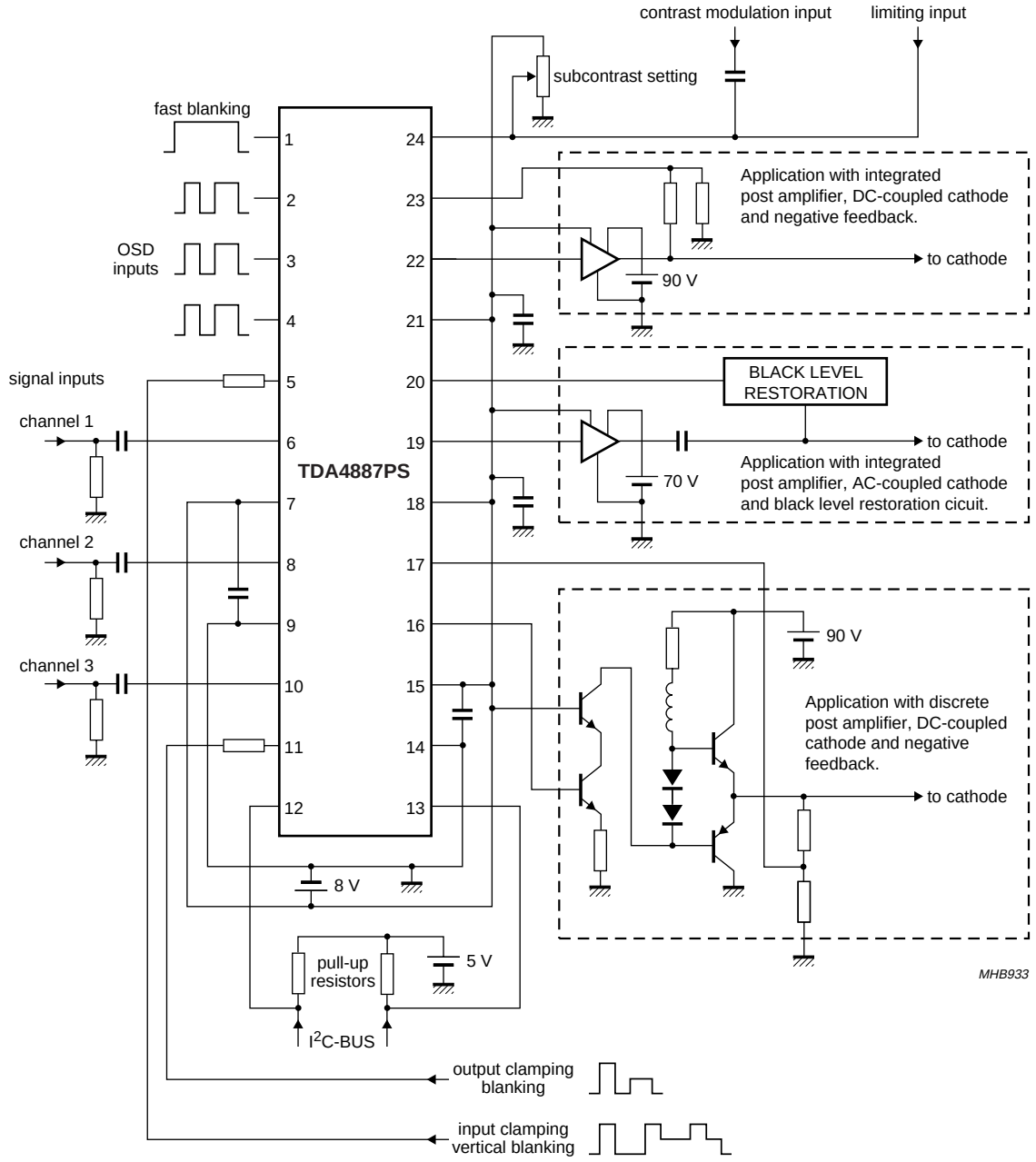


Fig.16 Basic applications for different kinds of post amplifiers with DC or AC coupling.

12.1 Test board

For high frequency measurements, a special test board with only a few external components can be built. It utilizes the internal positive feedback of the output signals during output clamping with control bit FPOL = 1. Figure 17 shows the test circuit and Figs 18 and 19 show the layout and mounting of the double-sided printed-circuit board. Most components are SMD-type. Short HF loops and minimum crosstalk between channels and between signal inputs and outputs are achieved by using properly shaped ground areas.

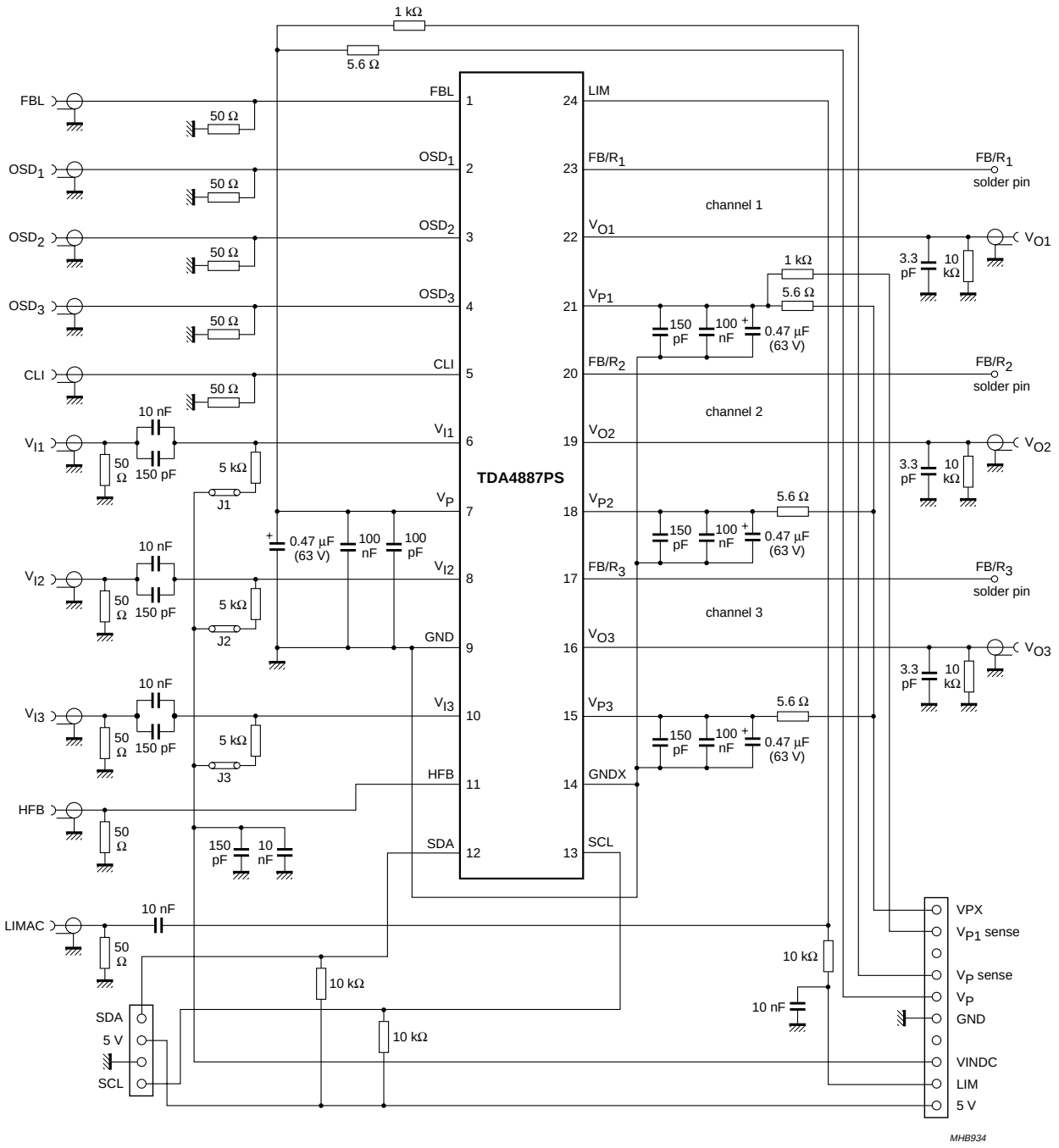
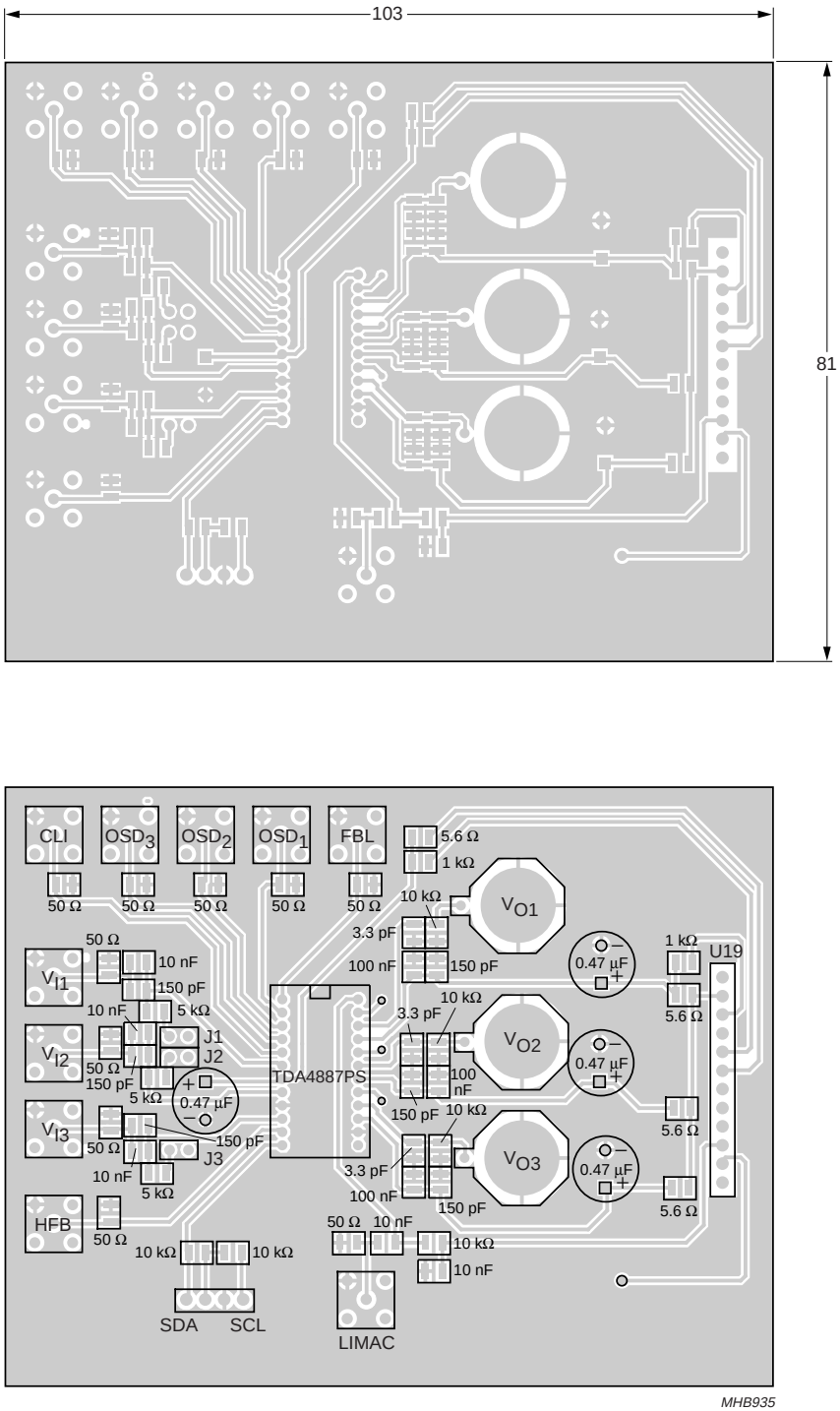
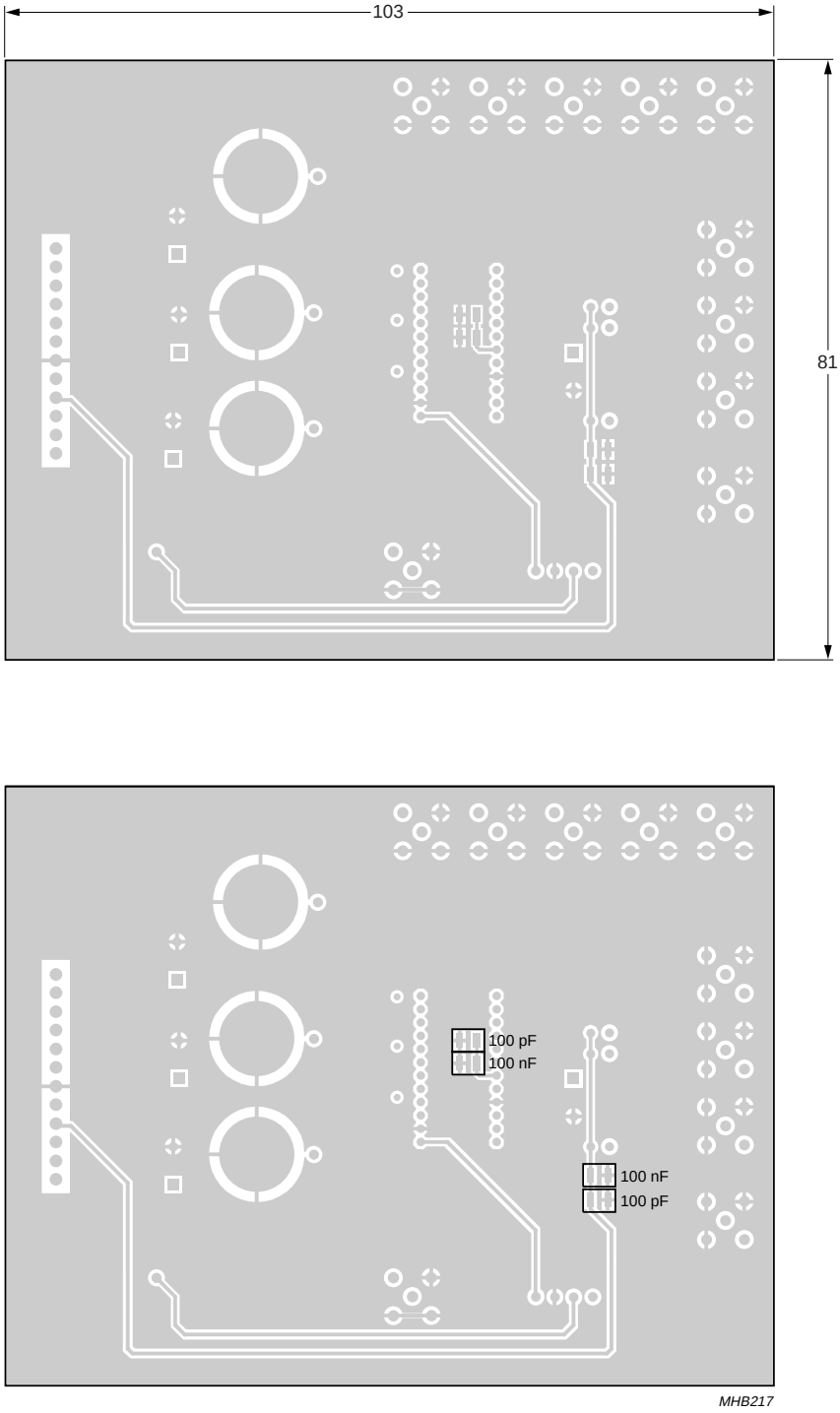


Fig.17 Test board utilizing internal positive feedback only (FPOL = 1).



Dimensions are in mm.

Fig.18 Printed-circuit top view shown with and without components mounted (for bottom view, see Fig.19).



Dimensions are in mm.

Fig.19 Printed-circuit bottom view shown with and without components mounted (for top view, see Fig.18).

12.2 Application board with monolithic post amplifier

Figure 20 shows the application circuit of TDA4887PS with a modern monolithic video post amplifier and AC-coupled CRT. The black level restoration circuit is designed for 80 V supply and use of I^2C-bus controlled external brightness setting. The 8 V supply voltage of the preamplifier is made from 12 V on this board. Connectors for video, sync, I^2C-bus, OSD, clamping pulses, beam current limiting and supply voltages are provided.

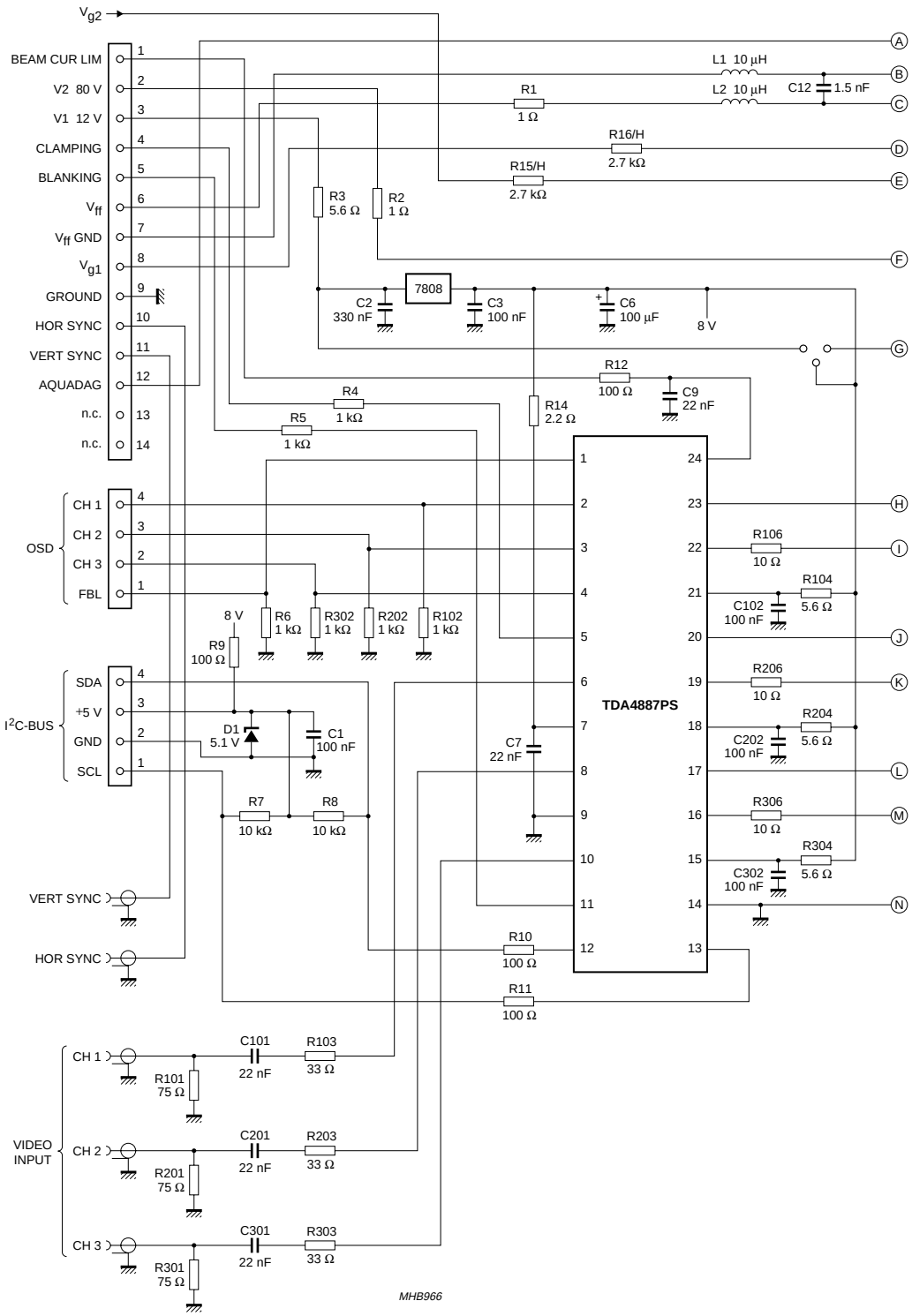


Fig.20 Application board with LM2435 (drawing is continued in Fig. 20).

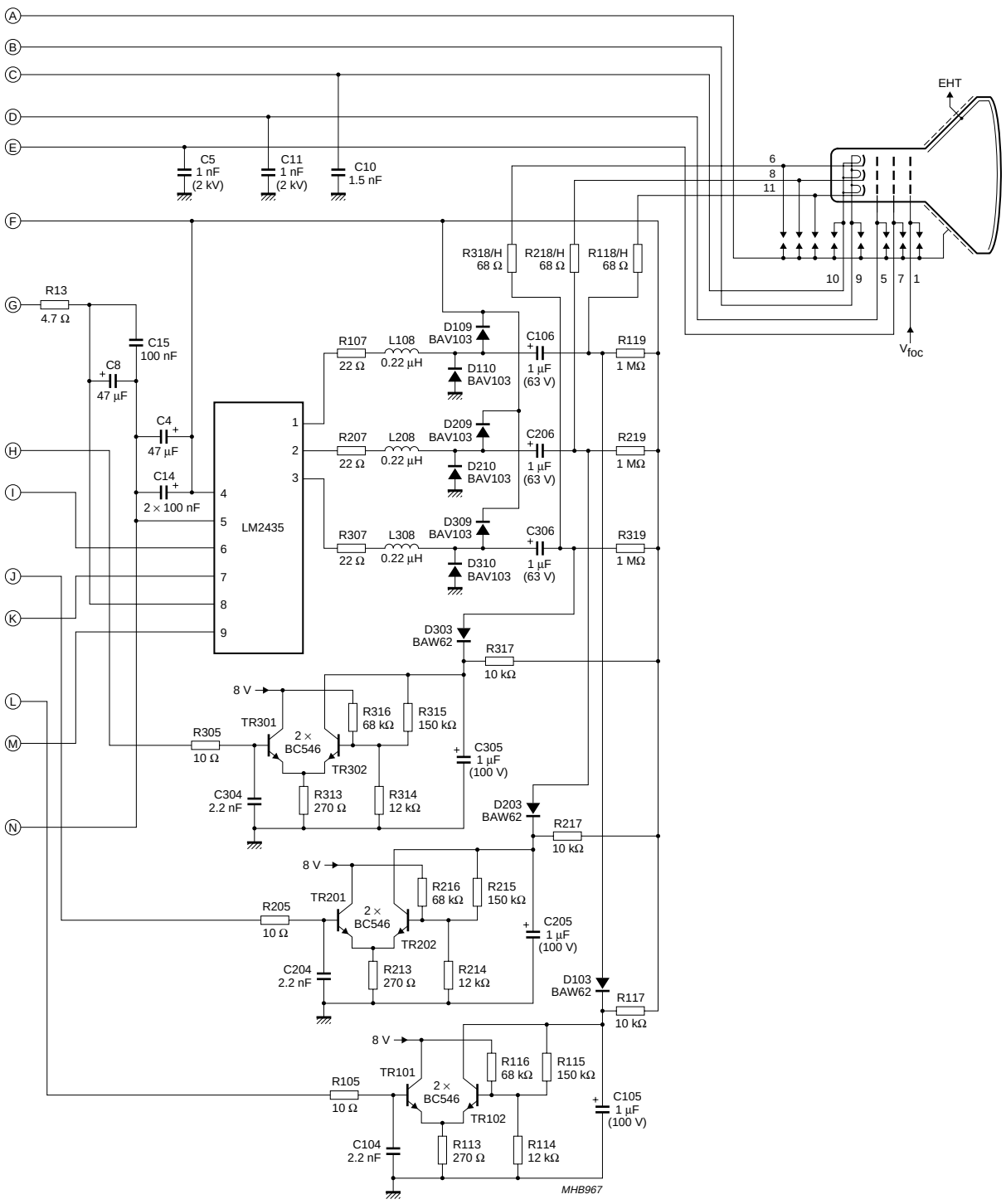


Fig.21 Application board with LM2435 (drawing continued from Fig. 20).

12.3 Building the application board

12.3.1 GENERAL

- Double-sided board
- Short HF loops by large ground plane on the rear
- SMD components with minimum parasitics.

12.3.2 VOLTAGE OUTPUTS

- Capacitive loads as small as possible
- Be aware of internal output resistance (typically 75 Ω).

12.3.3 SUPPLY VOLTAGES

- Capacitors as near as possible to the pins
- Use electrolytic capacitors with small serial resistance and inductance.

12.3.4 FLASHOVER

High electric field strength is present between the gun electrodes of picture tubes. In case of a flashover large transient currents and voltages may damage electronic components. It is therefore important to provide protective circuits with spark gaps, series resistors and protection diodes. Be aware that not only electronic components that are directly connected to the tube socket are endangered if interconnection lines on the application board are unfavourably routed.

12.4 Application hints

12.4.1 ALIGNMENT RECOMMENDATIONS USING BRIGHTNESS CONTROL WITH GREY SCALE TRACKING

12.4.1.1 Introduction (philosophy of TDA4887PS)

With the TDA4887PS the user may change contrast, brightness and even colour temperature (R, G, B gains) or any combination at will. The ‘x,y’ colour point will remain stable for the full grey scale. This feature is achieved in the following way:

A change of brightness will cause a change of black level which is proportional to the actual gain setting

Conversely, a change of gain setting will cause a change of black level that is proportional to the deviation of brightness from its nominal setting.

To benefit fully from this colour tracking feature, the reference black levels of the video amplifiers must match exactly to the cut-off points of the cathodes.
Re-adjustments of black level settings by the end user should be avoided, because this will upset the tracking feature.

12.4.1.2 Difficulty during monitor production

The factory cut-off alignment is done at a quite high level (e.g. 2.4 cd/m^2). As a consequence it is not certain that the reference black level will match the cut-off exactly after a first black level adjustment. If then the R, G, B gains are adjusted for the (x, y) white point at e.g. 102.8 cd/m^2, the white balance at 2.4 cd/m^2 will have changed. So two or more alignment cycles may be needed to achieve good results.

12.4.1.3 Considerations for a single-pass factory alignment

The nominal brightness setting is 40H. In this condition the black level equals reference black level and must match to the CRT cut-off.

For a better understanding, discrete values for luminance, video and feedback gain have been taken (these values should be regarded as examples). For special applications actual values have to be taken instead.

White point must be aligned at maximum luminance (e.g. at 102.8 cd/m^2) with maximum contrast and nominal brightness. It is recommended to use only a small white square for white point alignment, to prevent variations of the voltage at grid G1 (V_{g1}) and grid G2 (V_{g2}) and to prevent unwanted activation of the automatic beam limiter (ABL).

For practical reasons, alignment of the R, G, B reference black levels must be done with a small amount of drive for obtaining a luminance level of approximately 2.4 cd/m^2. This drive can be simulated by setting the brightness to a certain value. Assuming 102.8 cd/m^2 luminance with full white video (100% drive) and a cathode characteristic with gamma = 2.25, the drive for black level adjustment can be shown as:

$$\frac{2.4}{102.8^{1/2.25}} \times 100 = 18.8\% \text{ drive}$$

which corresponds to a brightness setting of B8H.

After black level adjustment for L = 2.4 cd/m^2, the cathode voltages are fixed and the cut-off voltages are set with equal gain condition in all channels. During white point adjustment the gains will be changed. In the factory procedure for single pass adjustment, the luminance level for black level alignment (2.4 cd/m^2) is kept constant while adjusting the gain settings. To achieve this, the black level references are compensated by software and an alignment computer (this compensation is for factory alignment only and is not needed for any user change of R, G, B gain).

Calculation of compensation (see Fig.22):

1. Gain adjustment is in 255 steps from 20 to 100% which equates to 4.6 V per step at maximum contrast.

   One step = $\frac{0.8 \times 4.6\ V}{255} = 14.4\ mV$ which is equal to 187 mV at the cathode with video gain = 13 for the white area.
2. For 18.8% drive (used for black level adjustment) the output changes only 2.7 mV (35 mV at the cathode) per gain step.
3. The black level adjustment range (at feedback inputs) is 1.9 V in 255 steps, which is 7.45 mV per step (Δ black level of 97 mV at the cathode with feedback gain = $^1/_{13}$). It follows that the optimum compensation is one step black level for $\frac{97}{35} = 2.8$ or approximately three steps of gain.

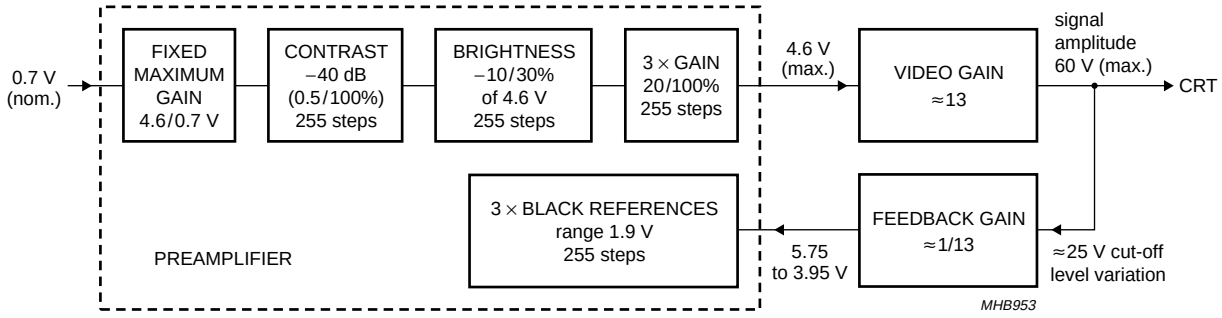


Fig.22 Signal amplification and feedback references.

12.4.1.4 Example of automatic factory alignment

This procedure shows a realization of the alignment description, it depends on disposable equipment.

Gamma = 2.25, maximum luminance = 102.8 cd/m^2, video gain = 13, feedback gain = $^1/_{13}$, white D; see Fig.23.

1. Initialization
   a) Set grid 2 voltage to minimum
   b) Set R, G, B gains to the centre values (80H, subaddresses 04H, 05H, 06H)
   c) Set R, G, B black references to centre values (80H, subaddresses 07H, 08H, 09H)
   d) Set contrast to maximum (FFH, subaddress 02H).
2. V_{g2} and black levels
   a) Set brightness to 18.8% drive (B8H, subaddress 01H, control bit BRI=0)
   b) Apply black video
   c) Increase V_{g2} manually until one colour appears
   d) Activate the alignment computer
   e) The computer will continuously adjust the R, G, B black levels to meet the following three conditions:
      x = 0.131
      y = 0.329
      the centre of the min/max setting remains at 80H (this will leave some margin for the compensation steps that follow)
   f) Fine tuning of V_{g2} (or V_{g1}) until Y = 2.4 cd/m^2 with the computer still active.

3. R, G, B gains (white point)
   a) Set brightness at nominal (40H)
   b) Apply full video white area (700 mV)
   c) Activate the computer
   d) The computer will adjust the R, G, B gains to meet the following three conditions:
      x = 0.313
      y = 0.329
      Y = 102.8 cd/m^2
      For each 3 (2.8) gain increments, the computer will decrement the black references by one step.

The effect on cathode voltages is demonstrated in Fig.23. After step 2 the voltages at 18.8% drive are correct but not those at 100% drive (white) and 0% (black). After step 3 the voltages at 18.8% drive have not changed but white as well as black voltages are correct now. Any brightness setting (−10 to +30%) relates to the individual maximum video amplitude (black-to-white).

This alignment procedure is adaptable to DC-coupled as well as AC-coupled cathodes.

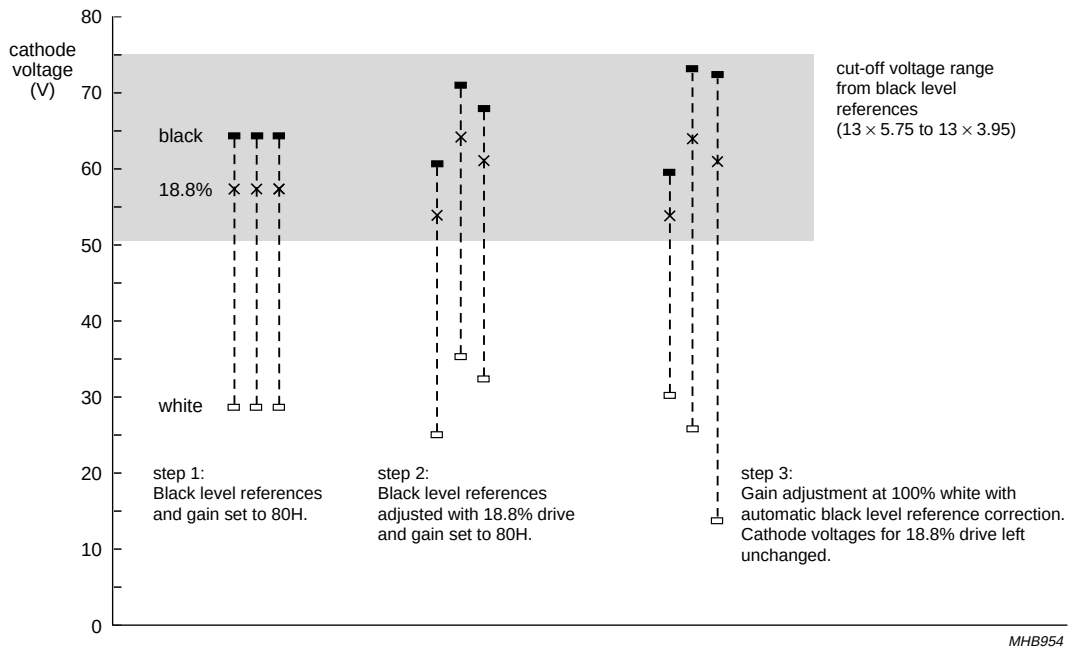


Fig.23 Automatic factory alignment.

12.4.2 BLACK LEVEL RESTORATION

Figure 24 shows two simple circuits for black level restoration for applications with AC-coupled cathodes. The output signal of the post amplifier is coupled via a 1 µF capacitor and a 68 Ω resistor to the cathode. The cathode voltage is clamped (peak responding) to the DC voltage $V_{cl} = V_b + V_{BE}$ via diode D1. The voltage V_b is derived from the bus controlled reference voltage V_{ref} (pin FB/$R_{(n)}$ of TDA4887PS) by resistor network R1 to R2.

$V_b = V_a \times \frac{R1 + R2}{R1}$ for the upper circuit.

$V_b = V_{p1} - (V_{a1} - V_{be}) \times \frac{R2}{R1}$ for the lower circuit.

The upper circuit has much less temperature dependence on clamp voltage and, in the event of an I²C-bus Power-on reset in TDA4887PS, all clamp voltages go to black.

For correct clamping, a well-defined top level of V_{sig} is necessary (pedestal black level has to be the most positive voltage).

When using internal brightness control, pedestal blanking (subaddress 0BH) has to be larger than minimum possible brightness setting (10% of maximum signal swing if the complete range is used). With 40 V maximum signal swing and 15% pedestal blanking, the clamping voltage V_{cl} has to be 6 V higher than the extended cut-off voltage.

Without using internal brightness control, at least 5% pedestal blanking is recommended.

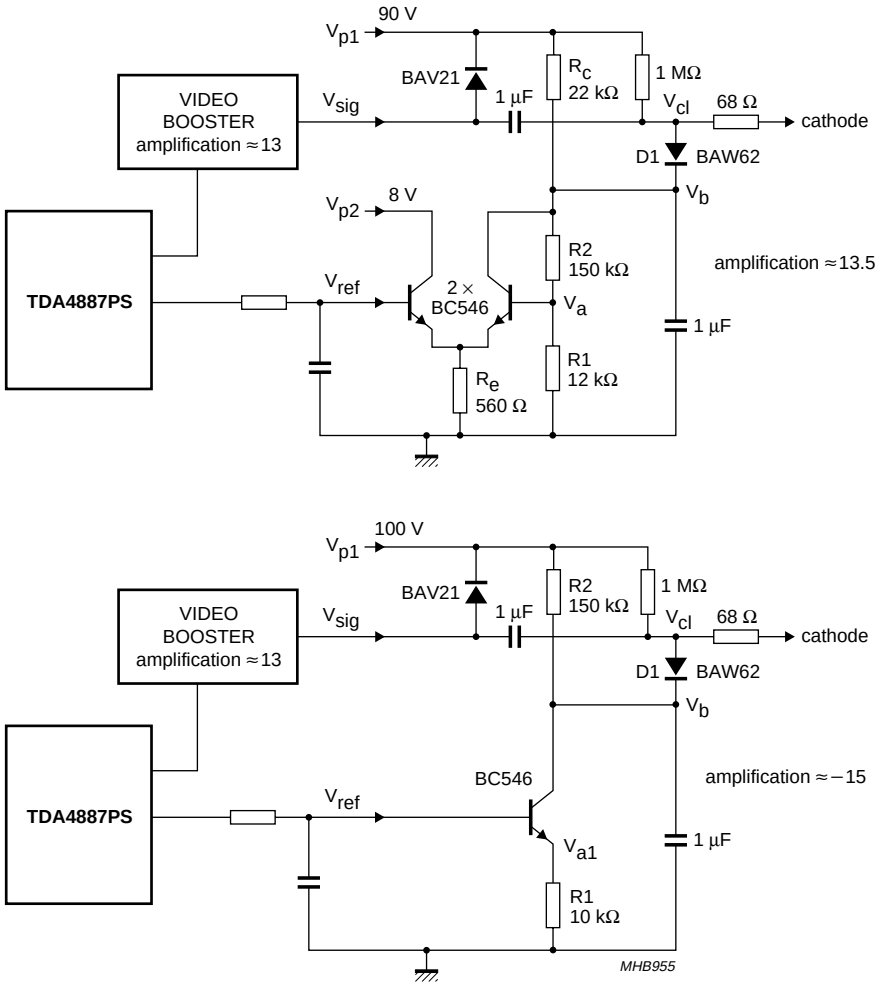


Fig.24 Black level restoration circuits.

12.4.3 Avoiding negative input voltages at blanking and clamping input pins

Negative voltages on any input pin causes ESD protection diodes and other internal junctions will become open-circuit resulting in substrate current injection. Substrate currents can generate parasitic effects that are not completely predictable. Signal inputs (pins 6 and 10) are neighbouring clamping inputs (pins 5 and 11) and can therefore suffer from larger leakage currents during negative clamping pulse glitches. An internal circuit in combination with an external resistor protects the pins from negative voltages (see Fig.25).

At pin voltages near to ground level, the voltage difference between the internal reference voltage V_{ref} and the base voltage of TR1, which is $2V_{BE}$ higher than the pin voltage, generates a current through R1 which is amplified to the output by transistor TR1. The voltage drop at the external resistor R_{ext} stabilizes voltage V_{pin} near ground. The recommended value for R_{ext} is 1 kΩ.

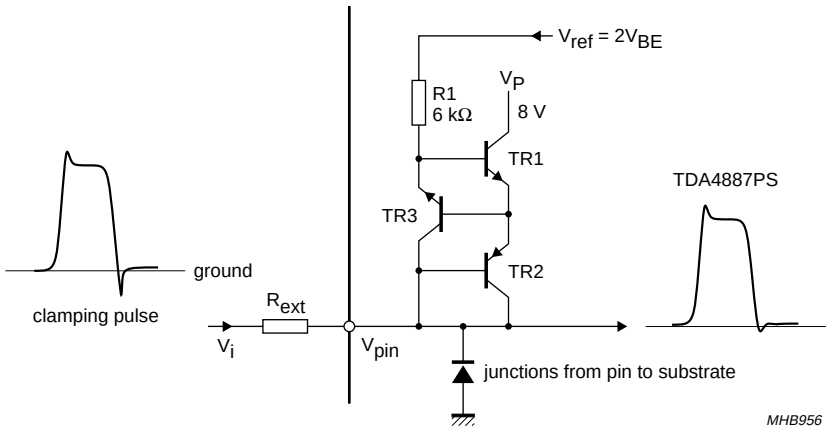
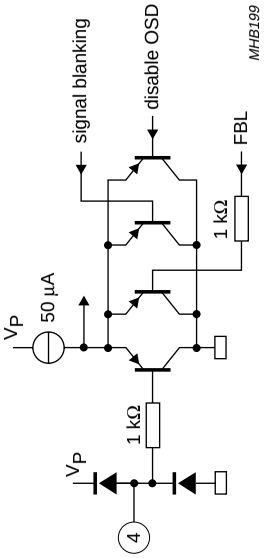
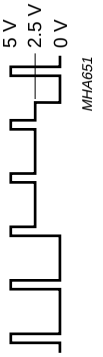
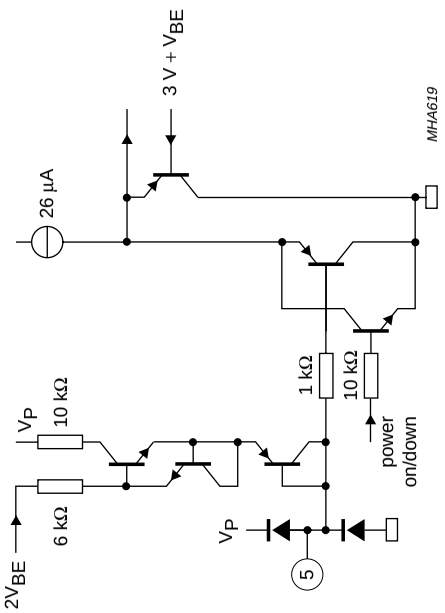


Fig.25 Protection circuit at pins CLI and HFB.

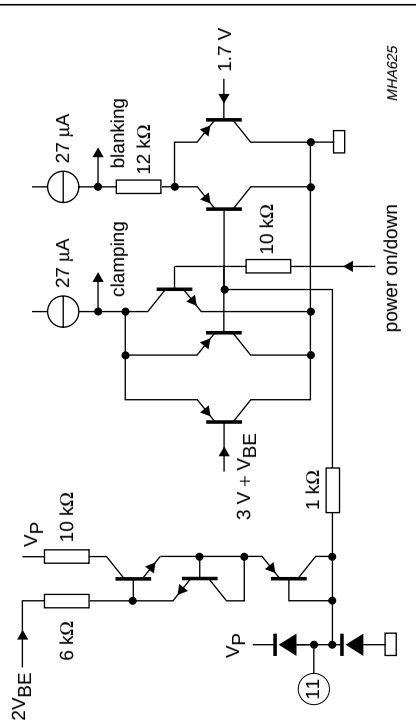
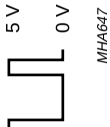
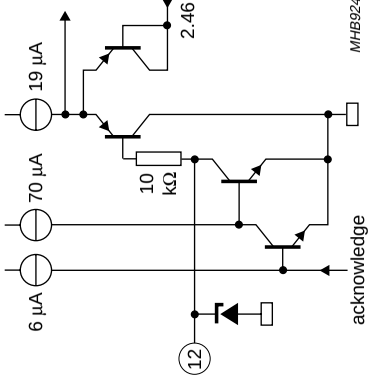
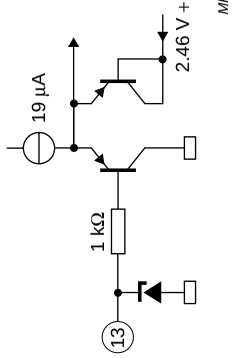
13 INTERNAL CIRCUITRY

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
1	FBL; fast blanking input for OSD insertion	open-circuit base		
2	OSD_1; OSD input channel 1	open-circuit base		
3	OSD_2; OSD input channel 2	open-circuit base		

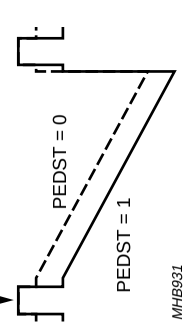
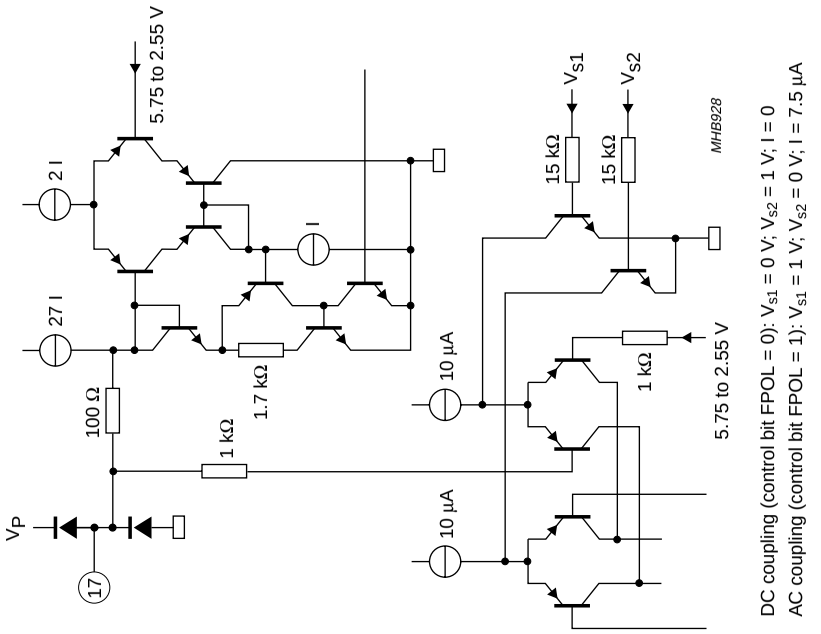
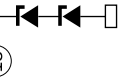
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
4	OSD_3; OSD input channel 3	open-circuit base		
5	CLI; vertical blanking input, input clamping input	V_{CLI} > 0.2 V: open-circuit base V_{CLI} ≤ 0.2 V: source current rising with decreasing voltage		

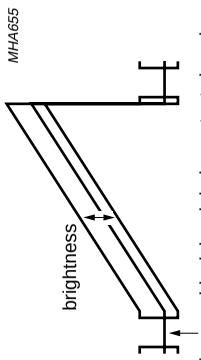
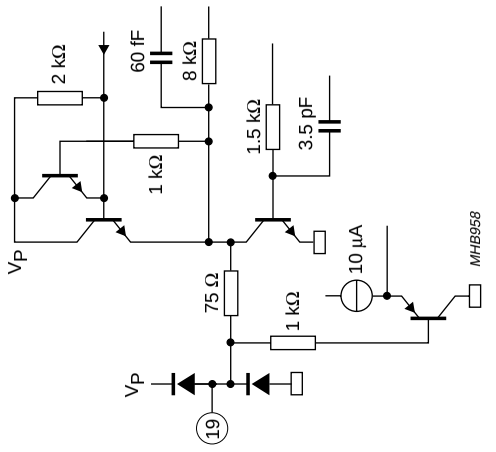
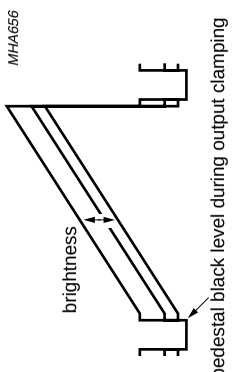
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
6	V_{I1}; signal input channel 1	outside clamping pulse: open-circuit base with base current compensation I_{I1} during clamping: −420 to +420 μA		
7	V_P; supply voltage	I_P = 25 mA (typical)		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
8	V_{I2}; signal input channel 2	outside clamping pulse: open-circuit base with base current compensation I_{I2} during clamping: −420 to +420 μA		
9	GND; ground			
10	V_{I3}; signal input channel 3	outside clamping pulse: open-circuit base with base current compensation I_{I3} during clamping: −420 to +420 μA		

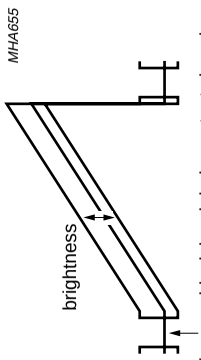
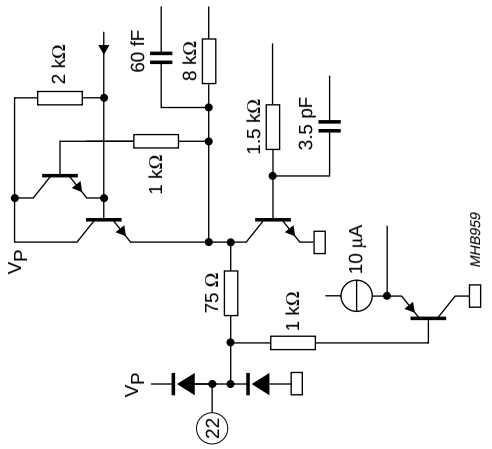
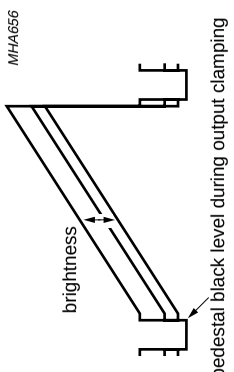
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
11	HFB; output clamping input, blanking input	V_{HFB} > 0.2 V: open-circuit base		
		V_{HFB} ≤ 0.2 V: source current rising with decreasing voltage		
12	SDA; I²C-bus serial data input/output	no acknowledge: open-circuit base		
		during acknowledge: I_{SDA} > 3 mA		
13	SCL; I²C-bus clock input	open-circuit base		

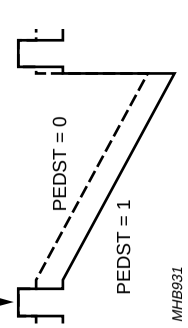
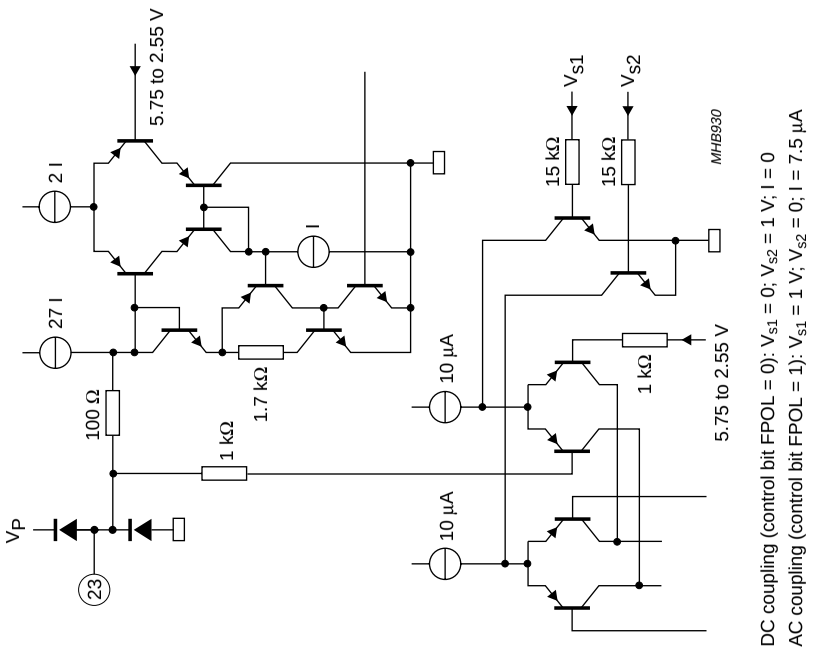
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
14	GNDX; ground signal channels 1, 2 and 3			
15	V_{P3}; supply voltage channel 3	I_{P3} = 20 mA (typical)		
16	V_{O3}; signal output channel 3	reference black level voltage 0.1 to 2.8 V	control bit PEDST = 0	
		pedestal black level voltage 0.1 to 2.8 V	control bit PEDST = 1	

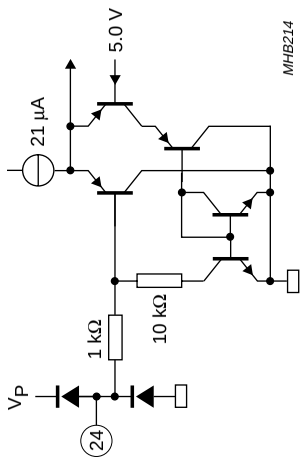
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
17	FB/R_3; feedback input/ reference voltage output channel 3	open-circuit base		
		control bit FPOL = 0		
		control bit FPOL = 1		
		$I_{FB/R3}$: −200 to +200 µA $V_{FB/R3}$: 5.75 to 2.55 V		
18	V_{P2}; supply voltage channel 2	I_{18} = 20 mA (typical)		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
19	V_{O2}; signal output channel 2	reference black level voltage 0.1 to 2.8 V	 control bit PEDST = 0	
		pedestal black level voltage 0.1 to 2.8 V	 control bit PEDST = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
20	FB/R_2; feedback input/reference voltage output channel 2	open-circuit base	 control bit FPOL = 0	 DC coupling (control bit FPOL = 0): V_{s1} = 0; V_{s2} = 1 V; I = 0 AC coupling (control bit FPOL = 1): V_{s1} = 1 V; V_{s2} = 0; I = 7.5 µA
		$I_{FB/R2}$: –200 to +200 µA $V_{FB/R2}$: 5.75 to 2.55 V	control bit FPOL = 1	
21	V_{P1}; supply voltage channel 1	I_{P1} = 20 mA (typical)		

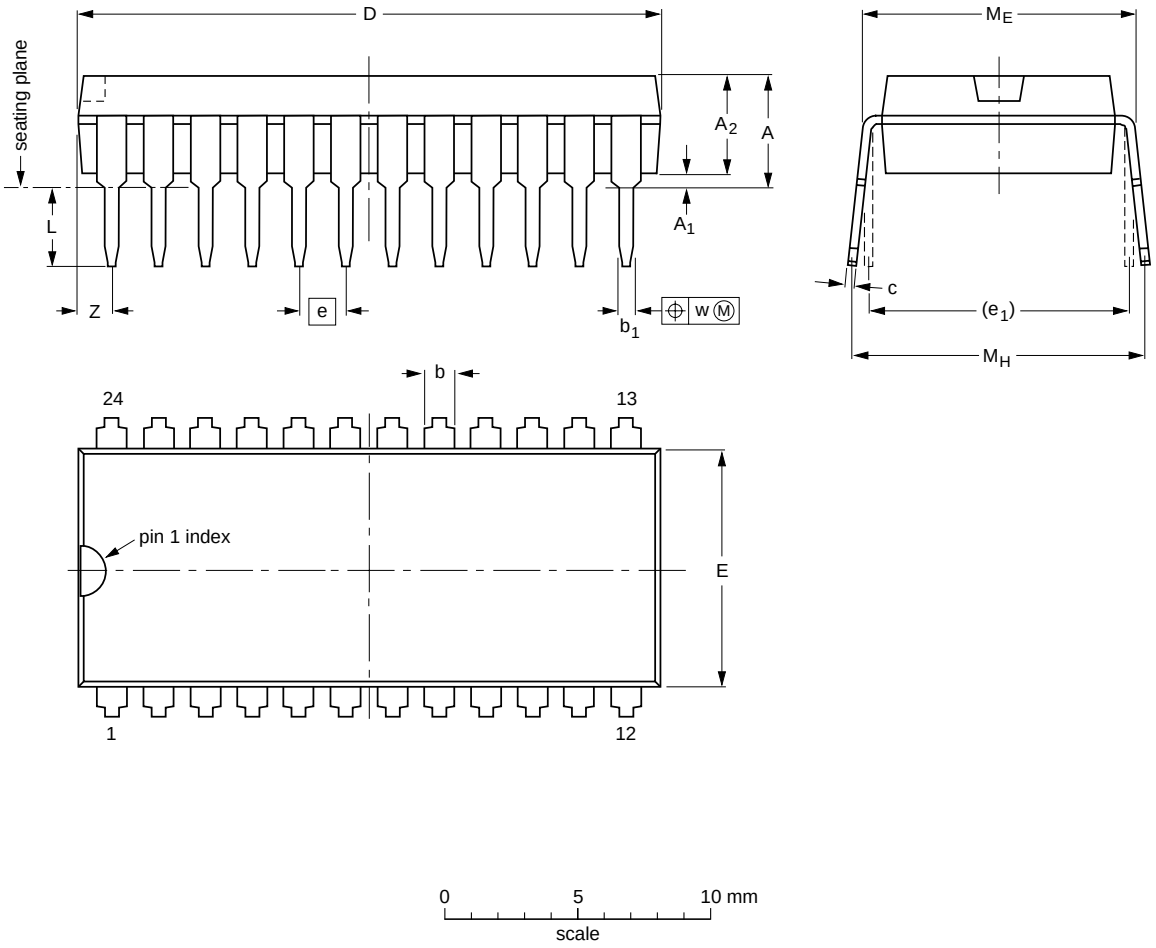
PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
22	V_{O1}; signal output channel 1	reference black level voltage 0.1 to 2.8 V	 control bit PEDST = 0	
		pedestal black level voltage 0.1 to 2.8 V	 control bit PEDST = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	WAVEFORM	EQUIVALENT CIRCUIT
23	FB/R_1; feedback input/reference voltage output channel 1	open-circuit base	 control bit FPOL = 0	
		$I_{FB/R1}$: −200 to +200 µA $V_{FB/R1}$: 5.75 to 2.55 V	control bit FPOL = 1	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC		WAVEFORM	EQUIVALENT CIRCUIT
24	LIM; subcontrast adjustment, contrast modulation, beam current limiting input	open-circuit voltage V_{LIM} = 5 V	V_{LIM} < 4.4 V: open-circuit base		

14 PACKAGE OUTLINE

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

15 SOLDERING

15.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

15.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

16 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective specification	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product specification	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18 DISCLAIMERS

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19 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Printed in The Netherlands 753504/01/pp68 Date of release: 2001 Oct 19 Document order number: 9397 750 08393

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