

# DATA SHEET

## **TDA8714** 8-bit high-speed analog-to-digital converter

Product specification  
Supersedes data of 1996 Jan 31  
File under Integrated Circuits, IC02

1997 Oct 29

## 8-bit high-speed analog-to-digital converter

## TDA8714

## FEATURES

- 8-bit resolution
- Sampling rate up to 80 MHz
- No missing codes guaranteed
- High signal-to-noise ratio over a large analog input frequency range (7.7 effective bits at 4.43 MHz full-scale input at  $f_{\text{clk}} = 80$  MHz)
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 340 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

## APPLICATIONS

High-speed analog-to-digital conversion for:

- video data digitizing
- radar pulse analysis
- transient signal analysis
- high energy physics research
- $\Sigma\Delta$  modulators
- medical imaging.

## GENERAL DESCRIPTION

The TDA8714 is an 8-bit high-speed Analog-to-Digital Converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CCA}}$	analog supply voltage		4.75	5.0	5.25	V
$V_{\text{CCD}}$	digital supply voltage		4.75	5.0	5.25	V
$V_{\text{CCO}}$	output stages supply voltage		4.75	5.0	5.25	V
$I_{\text{CCA}}$	analog supply current		–	25	30	mA
$I_{\text{CCD}}$	digital supply current		–	27	33	mA
$I_{\text{CCO}}$	output stages supply current		–	16	20	mA
INL	DC integral non-linearity		–	$\pm 0.4$	$\pm 0.5$	LSB
DNL	DC differential non-linearity		–	$\pm 0.2$	$\pm 0.35$	LSB
AINL	AC integral non-linearity	note 1	–	$\pm 0.5$	$\pm 1.0$	LSB
$f_{\text{clk(max)}}$	maximum clock frequency					
	TDA8714/7		80	–	–	MHz
	TDA8714/6		60	–	–	MHz
	TDA8714/4		40	–	–	MHz
$P_{\text{tot}}$	total power dissipation		–	340	435	mW

## Note

1. Full-scale sine wave ( $f_i = 4.43$  MHz;  $f_{\text{clk}} = 80$  MHz).

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## ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8714T/4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	40
TDA8714T/6	SO24		SOT137-1	60
TDA8714T/7	SO24		SOT137-1	80
TDA8714M/4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	40
TDA8714M/6	SSOP24		SOT340-1	60
TDA8714M/7	SSOP24		SOT340-1	80

## BLOCK DIAGRAM

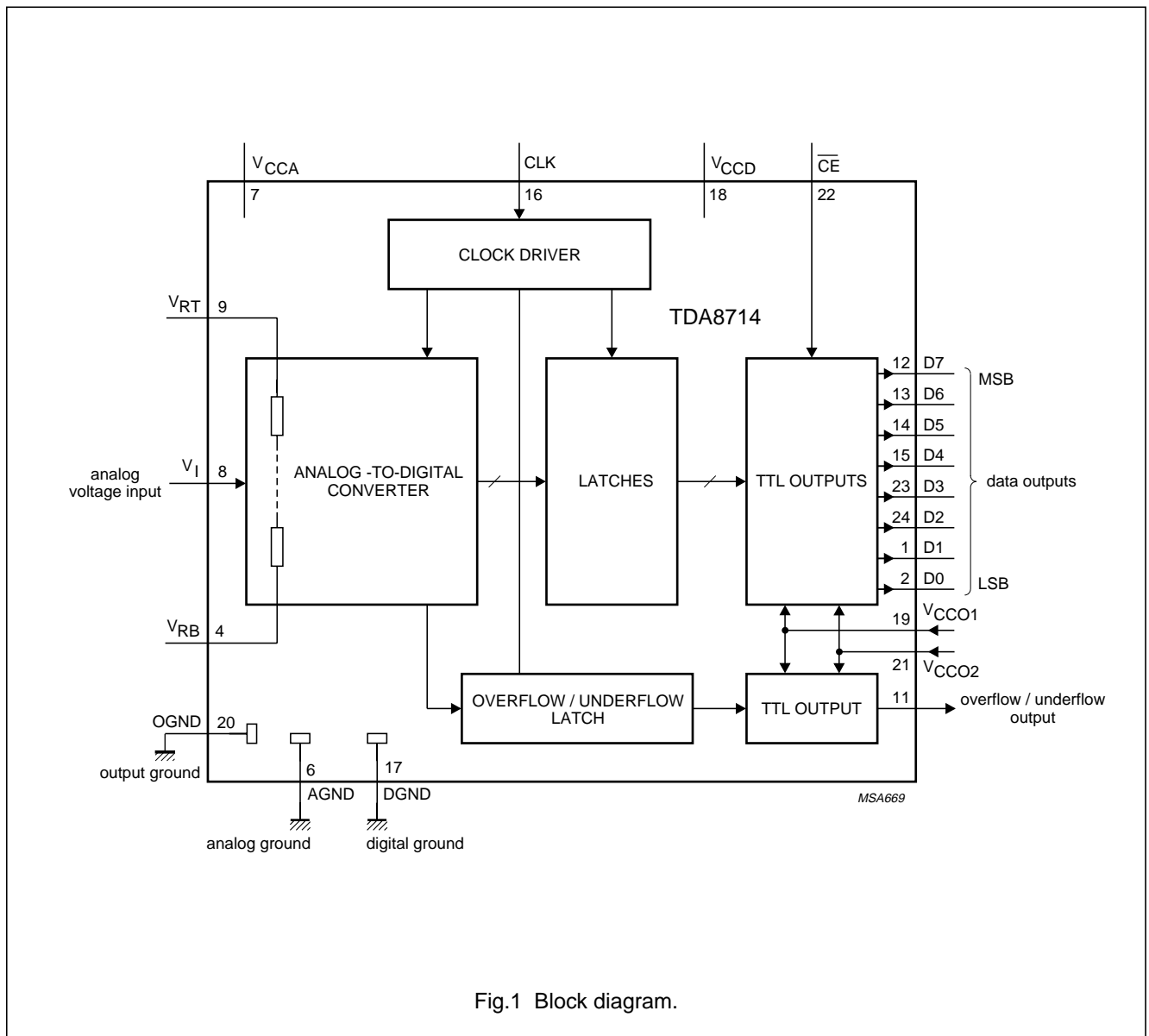


Fig.1 Block diagram.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V <sub>RB</sub>	4	reference voltage BOTTOM input
n.c.	5	not connected
AGND	6	analog ground
V <sub>CCA</sub>	7	analog supply voltage (+5 V)
V <sub>I</sub>	8	analog input voltage
V <sub>RT</sub>	9	reference voltage TOP input
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V <sub>CCD</sub>	18	digital supply voltage (+5 V)
V <sub>CCO1</sub>	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V <sub>CCO2</sub>	21	supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

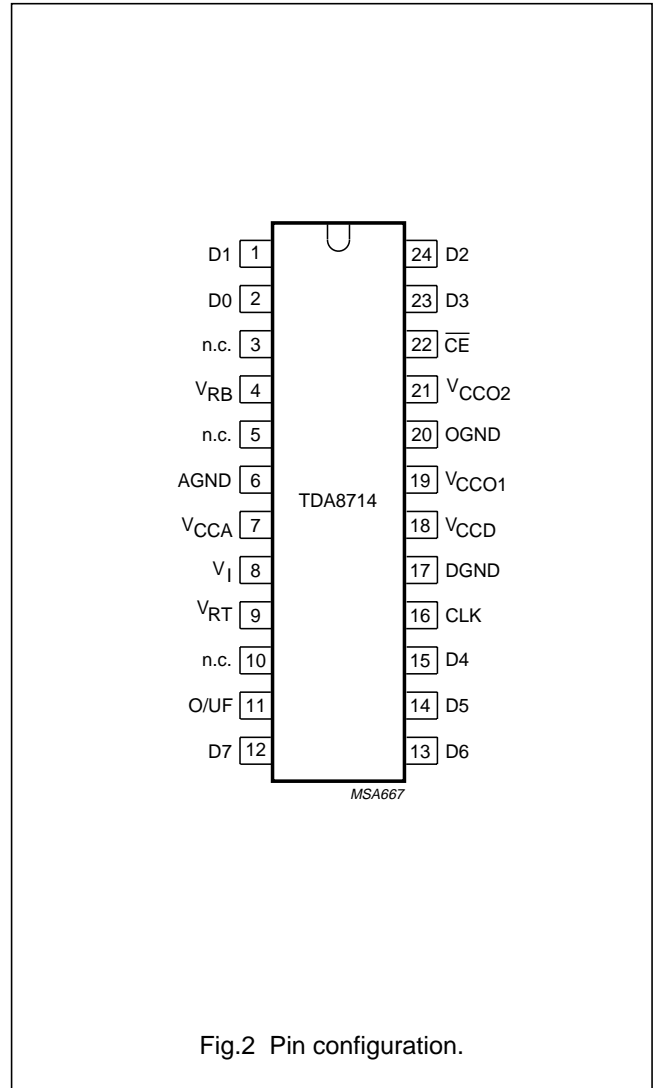


Fig.2 Pin configuration.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	note 1	-0.3	+7.0	V
$V_{CCD}$	digital supply voltage	note 1	-0.3	+7.0	V
$V_{CCO}$	output stages supply voltage	note 1	-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCA}$ and $V_{CCD}$		-1.0	+1.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCO}$ and $V_{CCD}$		-1.0	+1.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCA}$ and $V_{CCO}$		-1.0	+1.0	V
$V_I$	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	$V_{CCD}$	V
$I_O$	output current		-	10	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		0	+70	°C
$T_j$	junction temperature		-	+150	°C

**Note**

- The supply voltages  $V_{CCA}$  and  $V_{CCD}$  may have any value between -0.3 V and +7.0 V provided the difference between  $V_{CCA}$  and  $V_{CCD}$  is between -1 V and +1 V.

**HANDLING**

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT137-1	75	K/W
	SOT340-1	119	K/W

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**CHARACTERISTICS**

$V_{CCA} = V_7$  to  $V_6 = 4.75$  to  $5.25$  V;  $V_{CCD} = V_{18}$  to  $V_{17} = 4.75$  to  $5.25$  V;  $V_{CCO} = V_{19}$  and  $V_{21}$  to  $V_{20} = 4.75$  to  $5.25$  V; AGND and DGND shorted together;  $V_{CCA}$  to  $V_{CCD} = -0.25$  to  $+0.25$  V;  $V_{CCO}$  to  $V_{CCD} = -0.25$  to  $+0.25$  V;  $V_{CCA}$  to  $V_{CCO} = -0.25$  to  $+0.25$  V;  $V_{i(p-p)} = 1.75$  V;  $T_{amb} = 0$  to  $+70$  °C; typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 5$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CCA}$	analog supply voltage		4.75	5.0	5.25	V
$V_{CCD}$	digital supply voltage		4.75	5.0	5.25	V
$V_{CCO}$	output stages supply voltage		4.75	5.0	5.25	V
$I_{CCA}$	analog supply current		–	25	30	mA
$I_{CCD}$	digital supply current		–	27	33	mA
$I_{CCO}$	output stages supply current		–	16	20	mA
<b>Inputs</b>						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{clk} = 0.4$ V	–400	–	–	µA
$I_{IH}$	HIGH level input current	$V_{clk} = 2.7$ V	–	–	300	µA
$Z_I$	input impedance	$f_{clk} = 80$ MHz	–	18	–	kΩ
$C_I$	input capacitance	$f_{clk} = 80$ MHz	–	1	–	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND); see Table 2						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
$I_{IH}$	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
$V_I$ (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
$I_{IL}$	LOW level input current	$V_I = 1.2$ V	–	0	–	µA
$I_{IH}$	HIGH level input current	$V_I = 3.5$ V	60	130	280	µA
$Z_I$	input impedance	$f_i = 4.43$ MHz	–	10	–	kΩ
$C_I$	input capacitance	$f_i = 4.43$ MHz	–	14	–	pF
<b>Reference voltages for the resistor ladder; see Table 1</b>						
$V_{RB}$	reference voltage BOTTOM		1.2	1.3	1.6	V
$V_{RT}$	reference voltage TOP		3.5	3.6	3.9	V
$V_{diff}$	differential reference voltage $V_{RT} - V_{RB}$		1.9	2.3	2.7	V
$I_{ref}$	reference current		–	11.5	–	mA
$R_{LAD}$	resistor ladder		–	200	–	Ω
$TC_{RLAD}$	temperature coefficient of the resistor ladder		–	0.24	–	ppm
$V_{osB}$	offset voltage BOTTOM	note 2	275	285	295	mV
$V_{osT}$	offset voltage TOP	note 2	305	315	325	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)		1.45	1.75	2.15	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Outputs</b>						
DIGITAL OUTPUTS D7 to D0 (REFERENCED TO DGND)						
$V_{OL}$	LOW level output voltage	$I_O = 1 \text{ mA}$	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_O = -0.4 \text{ mA}$	2.7	–	$V_{CCD}$	V
		$I_O = -1 \text{ mA}$	2.4	–	$V_{CCD}$	V
$I_{OZ}$	output current in 3-state mode	$0.4 \text{ V} < V_O < V_{CCD}$	–20	–	+20	$\mu\text{A}$
<b>Switching characteristics</b>						
CLOCK INPUT CLK (note 1; see Fig.3)						
$f_{clk(max)}$	maximum clock frequency					
	TDA8714/4		40	–	–	MHz
	TDA8714/6		60	–	–	MHz
	TDA8714/7		80	–	–	MHz
$t_{CPH}$	clock pulse width HIGH		6	–	–	ns
$t_{CPL}$	clock pulse width LOW		6	–	–	ns
<b>Analog signal processing</b>						
LINEARITY						
INL	DC integral non-linearity		–	$\pm 0.4$	$\pm 0.5$	LSB
DNL	DC differential non-linearity		–	$\pm 0.2$	$\pm 0.35$	LSB
AINL	AC integral non-linearity	note 3	–	$\pm 0.5$	$\pm 1.0$	LSB
BANDWIDTH ( $f_{clk} = 40 \text{ MHz}$ ); note 4						
B	analog bandwidth	full-scale sine wave	–	13	–	MHz
		75% full-scale sine wave; small signal at $V_i = \pm 5 \text{ LSB}$ , code 128	–	20	–	MHz
$t_{STLH}$	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.6; note 5	–	2.5	3.5	ns
$t_{STHL}$	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.6; note 5	–	3.0	4.0	ns
HARMONICS ( $f_{clk} = 40 \text{ MHz}$ )						
$h_1$	fundamental harmonics (full scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB
$h_{all}$	harmonics (full scale); all components	$f_i = 4.43 \text{ MHz}$				
	second harmonics		–	–64	–60	dB
	third harmonics		–	–58	–55	dB
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–56	–	dB
SIGNAL-TO-NOISE RATIO (note 6; see Figs 7 and 13)						
S/N	signal-to-noise ratio (full scale)	without harmonics; $f_{clk} = 40 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	46	48	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
EFFECTIVE BITS (note 6; see Figs 7 and 13)							
EB	effective bits TDA8714/4	$f_{\text{clk}} = 40 \text{ MHz}$					
		$f_i = 4.43 \text{ MHz}$	–	7.75	–	bits	
		$f_i = 7.5 \text{ MHz}$	–	7.6	–	bits	
	effective bits TDA8714/6	$f_{\text{clk}} = 60 \text{ MHz}$					
		$f_i = 4.43 \text{ MHz}$	–	7.7	–	bits	
		$f_i = 7.5 \text{ MHz}$	–	7.55	–	bits	
		$f_i = 10 \text{ MHz}$	–	7.4	–	bits	
	effective bits TDA8714/7	$f_{\text{clk}} = 80 \text{ MHz}$					
		$f_i = 4.43 \text{ MHz}$	–	7.7	–	bits	
$f_i = 7.5 \text{ MHz}$		–	7.5	–	bits		
$f_i = 10 \text{ MHz}$		–	7.2	–	bits		
	$f_i = 15 \text{ MHz}$	–	6.3	–	bits		
TWO-TONE (note 7)							
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 40 \text{ MHz}$	–	–56	–	dB	
BIT ERROR RATE							
BER	bit error rate	$f_{\text{clk}} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz};$ $V_I = \pm 16 \text{ LSB at}$ code 128	–	$10^{-11}$	–	times/ samples	
DIFFERENTIAL GAIN (note 8)							
$G_{\text{diff}}$	differential gain	$f_{\text{clk}} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz}$	–	0.6	–	%	
DIFFERENTIAL PHASE (note 8)							
$\varphi_{\text{diff}}$	differential phase	$f_{\text{clk}} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz}$	–	0.8	–	deg	
<b>Timing</b> (note 9; see Figs 3 and 5; $f_{\text{clk}} = 80 \text{ MHz}$ )							
$t_{\text{ds}}$	sampling delay time		–	–	2	ns	
$t_{\text{h}}$	output hold time		5	–	–	ns	
$t_{\text{d}}$	output delay time		–	10	11	ns	
<b>3-state output delay times</b> (see Fig.4)							
$t_{\text{dZH}}$	enable HIGH		–	40	44	ns	
$t_{\text{dZL}}$	enable LOW		–	12	16	ns	
$t_{\text{dHZ}}$	disable HIGH		–	50	54	ns	
$t_{\text{dLZ}}$	disable LOW		–	10	14	ns	



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### Notes to the characteristics

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including FF:
  - a)  $V_{osB}$  (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM ( $V_{RB}$ ) at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
  - b)  $V_{osT}$  (voltage offset TOP) is the difference between  $V_{RT}$  (reference voltage TOP) and the analog input which produces data outputs equal to FF at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
3. Full-scale sine wave ( $f_i = 4.43\text{ MHz}$ ;  $f_{clk} = 80\text{ MHz}$ ).
4. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio:  $S/N = EB \times 6.02 + 1.76\text{ dB}$ .
7. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
8. Measurement carried out using video analyser VM700A where the video analog signal is reconstructed through a digital-to-analog converter.
9. Output data acquisition: the output data is available after the maximum delay time of  $t_d$ ; in the event of 80 MHz clock operation, the hardware design must take into account the  $t_d$  and  $t_h$  limits with respect to the input characteristics of the acquisition circuit.

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**Table 1** Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{I(p-p)}$	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.585	1	0	0	0	0	0	0	0	0
0	1.585	0	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	3.28	0	1	1	1	1	1	1	1	1
Overflow	>3.28	1	1	1	1	1	1	1	1	1

**Table 2** Mode selection

$\overline{CE}$	D7 to D0	O/UF
1	high impedance	high impedance
0	active; binary	active

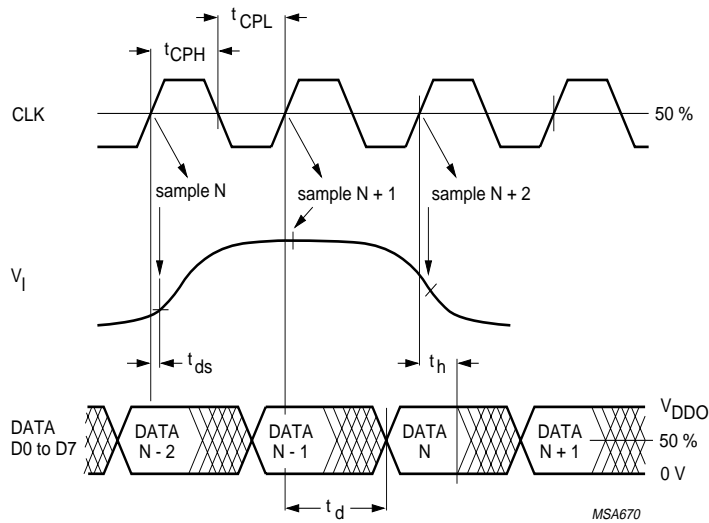


Fig.3 Timing diagram.

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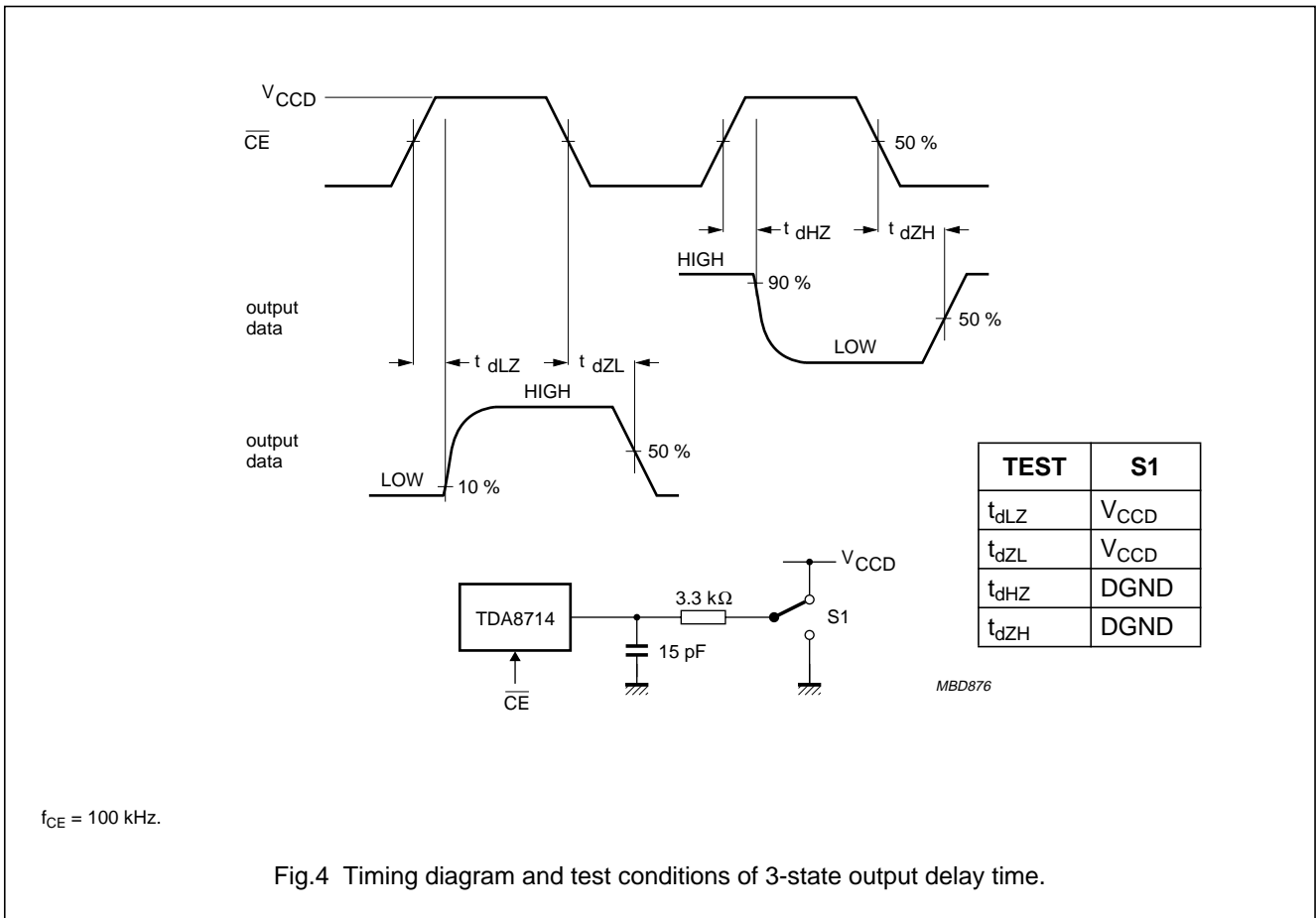


Fig.4 Timing diagram and test conditions of 3-state output delay time.

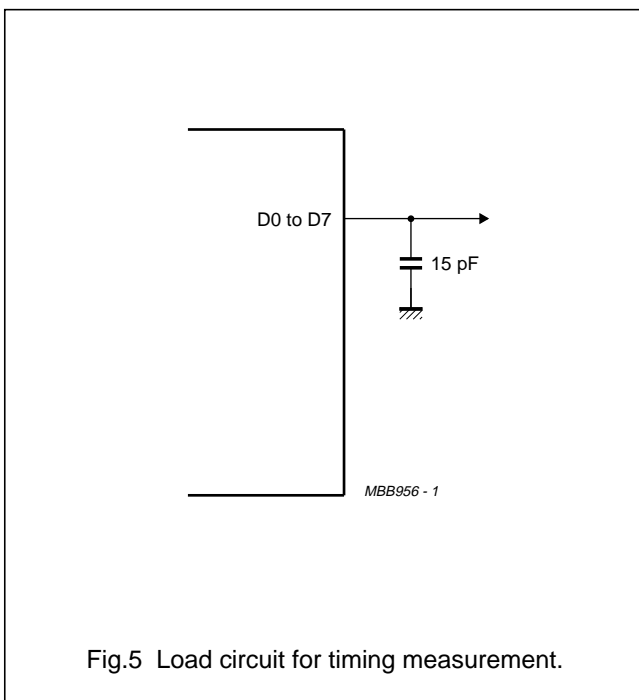


Fig.5 Load circuit for timing measurement.

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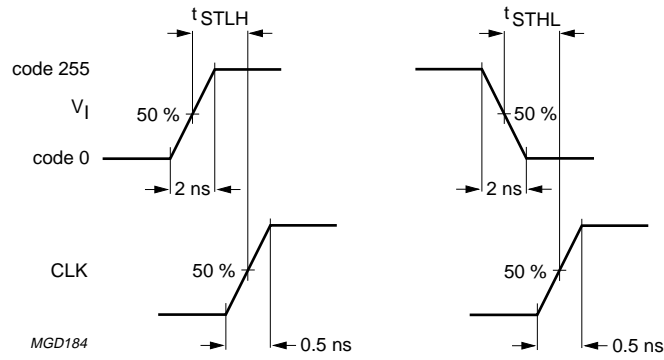
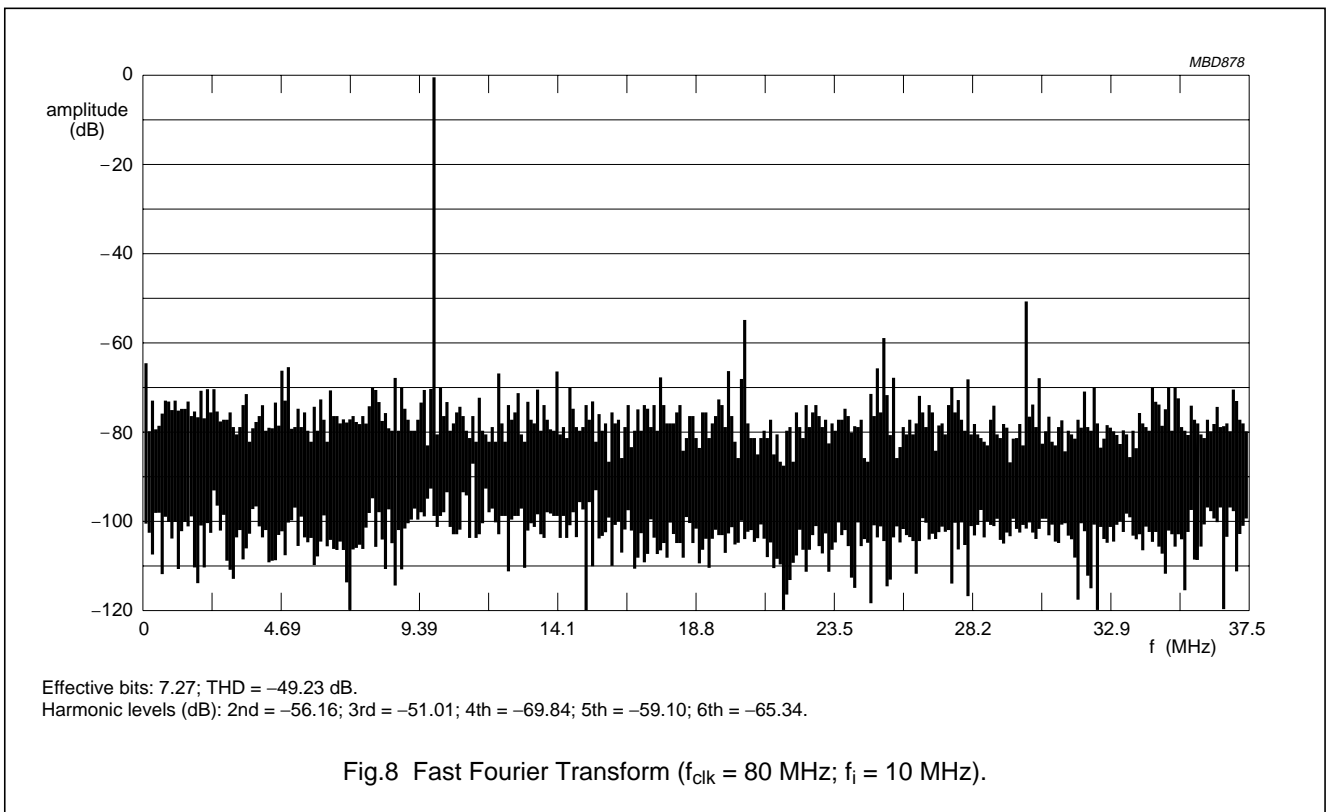
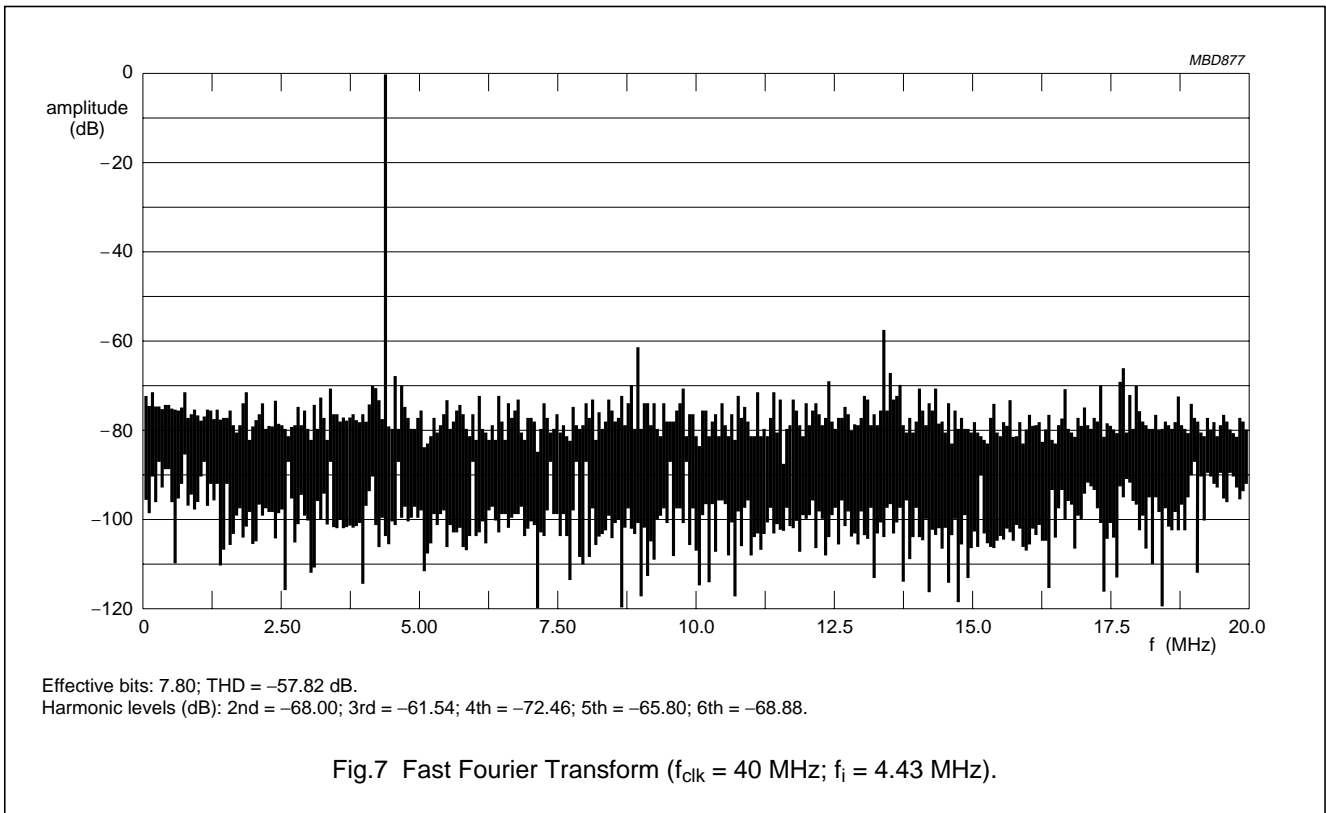


Fig.6 Analog input settling-time diagram.

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INTERNAL PIN CONFIGURATIONS

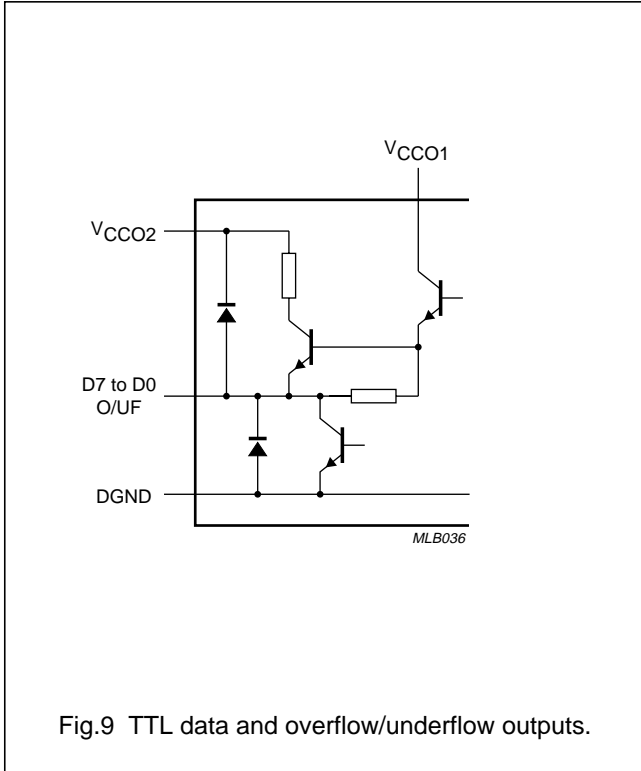


Fig.9 TTL data and overflow/underflow outputs.

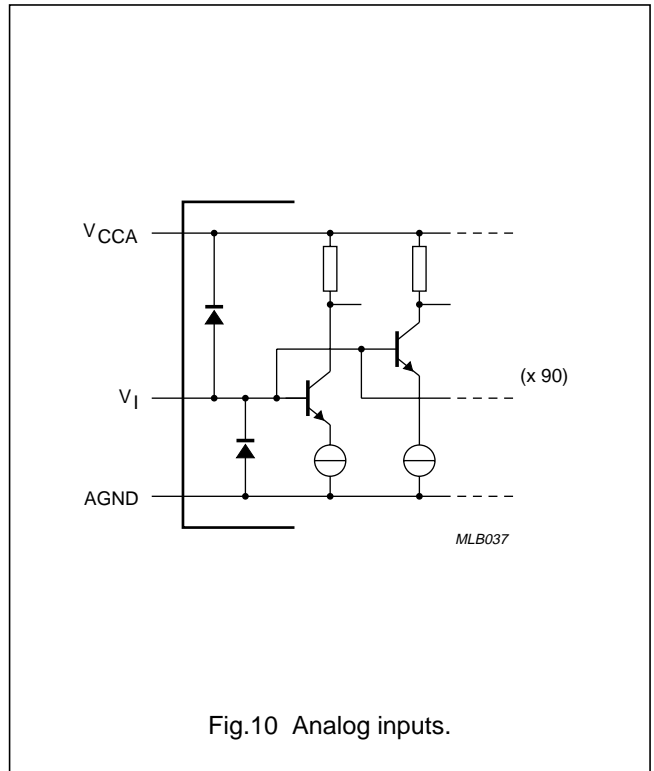


Fig.10 Analog inputs.

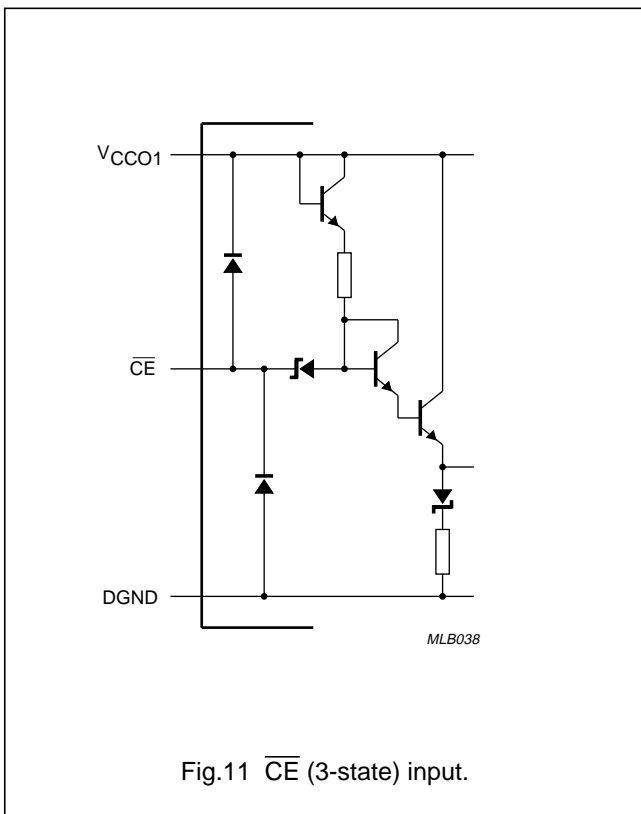


Fig.11  $\overline{CE}$  (3-state) input.

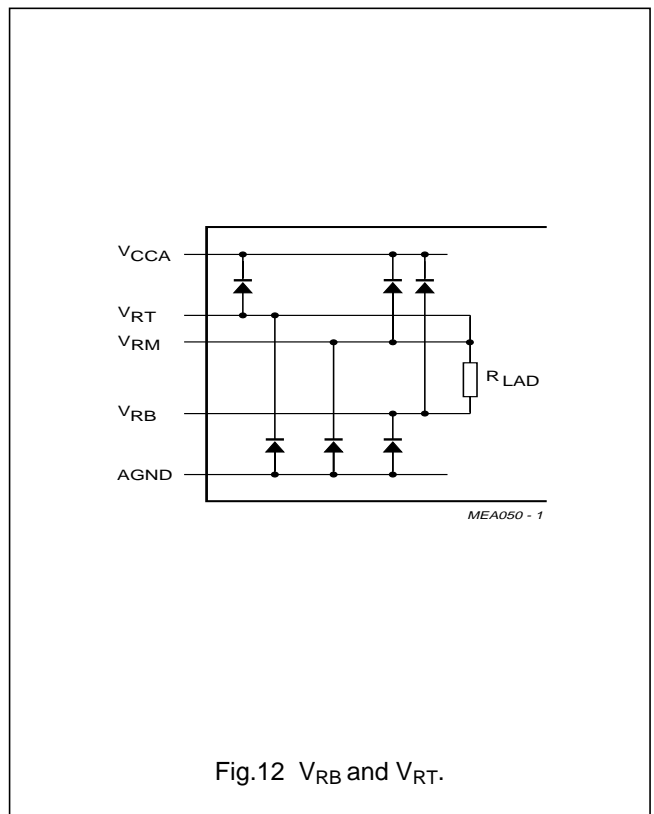
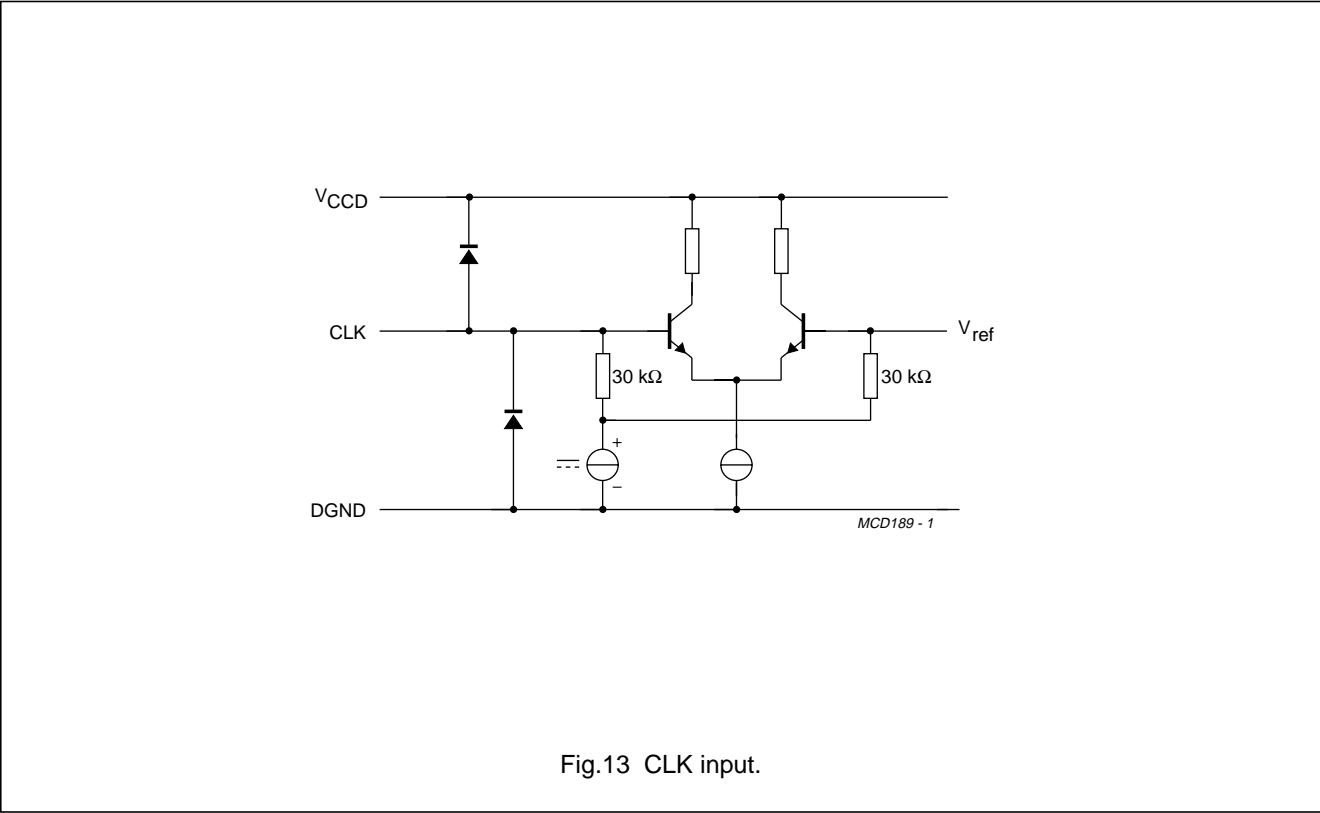


Fig.12 V<sub>RB</sub> and V<sub>RT</sub>.

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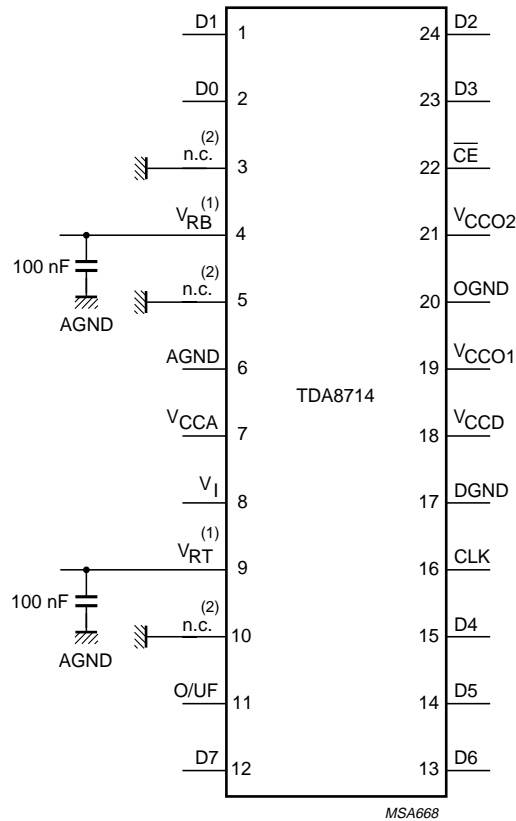
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APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value.

(1)  $V_{RB}$  and  $V_{RT}$  are decoupled to AGND.

(2) Pin 5 should be connected to AGND; pins 3 and 10 to DGND in order to prevent noise influence.

Fig.14 Application diagram.



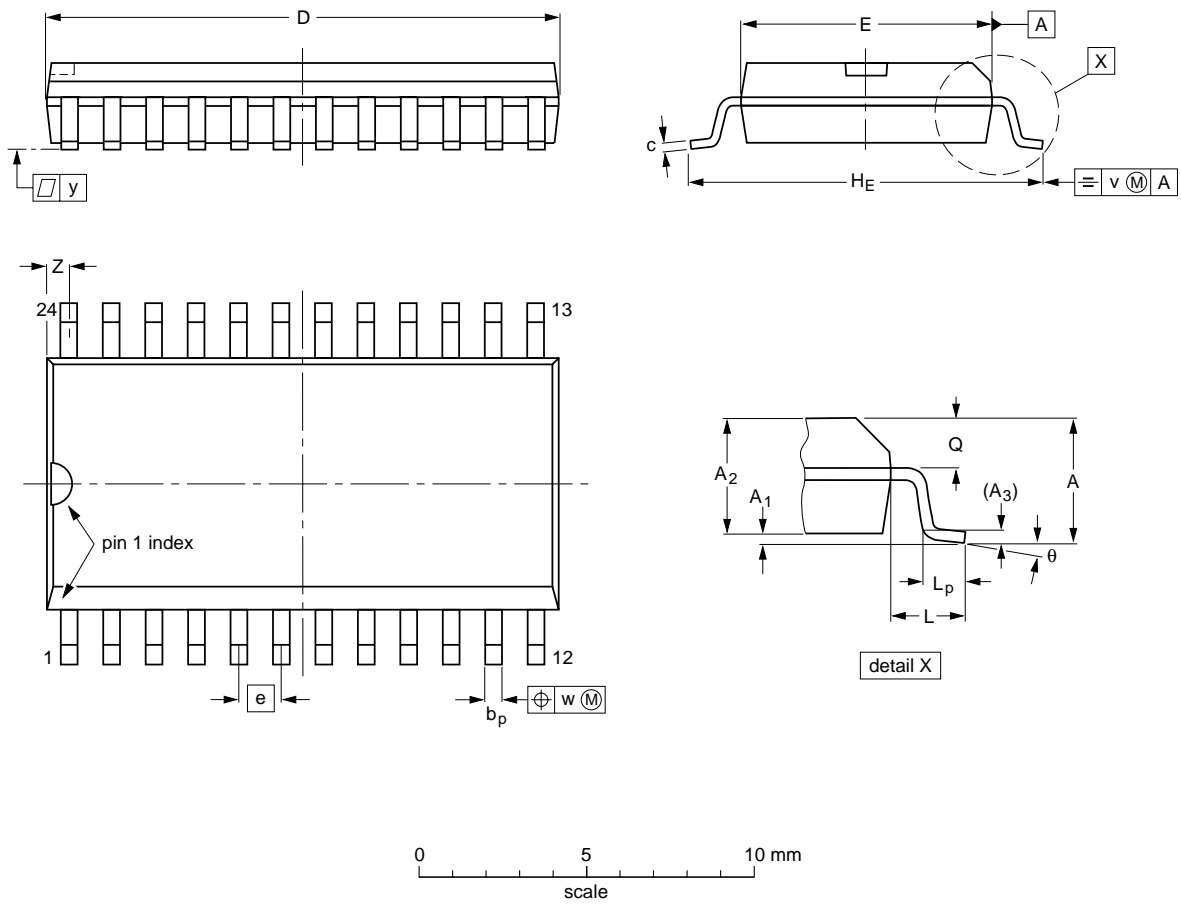
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PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

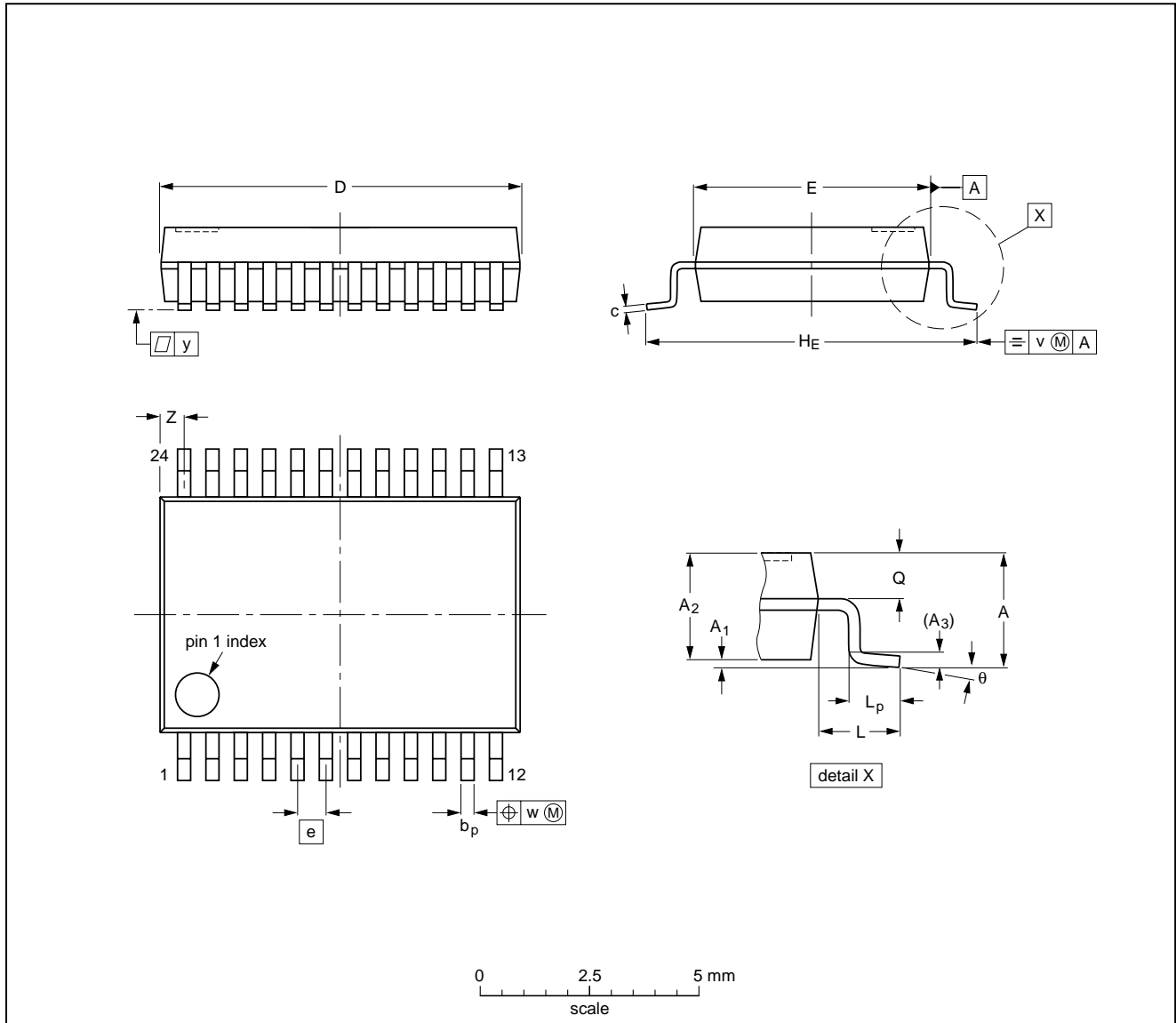
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

8-bit high-speed analog-to-digital converter

TDA8714

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT340-1		MO-150AG			93-09-08 95-02-04

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

##### SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

##### SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

#### METHOD (SO AND SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
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**NOTES**

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**NOTES**

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