

THC63LVD103

135MHz 30Bits COLOR LVDS Transmitter

General Description

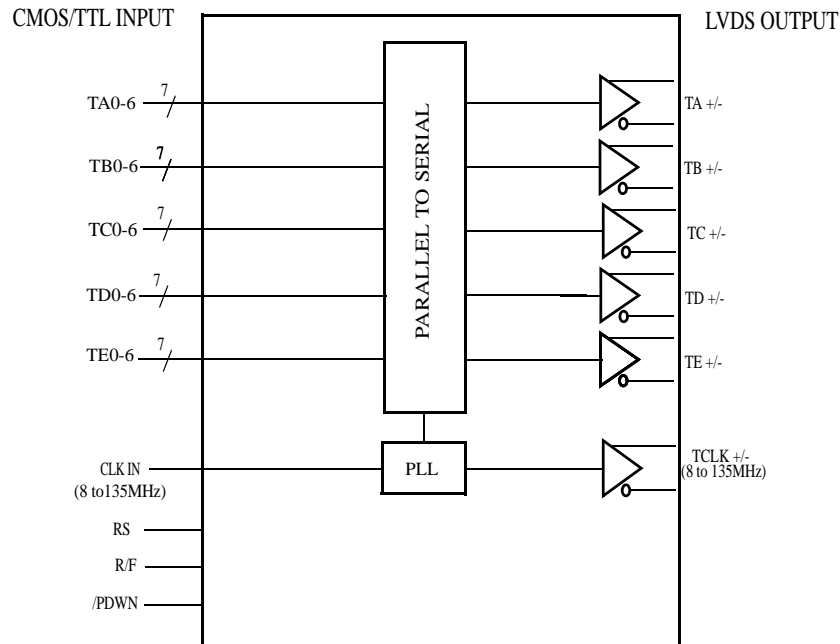
The THC63LVD103 transmitter is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA+ resolutions.

The THC63LVD103 converts 35bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 135MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted at an effective rate of 945Mbps per LVDS channel.

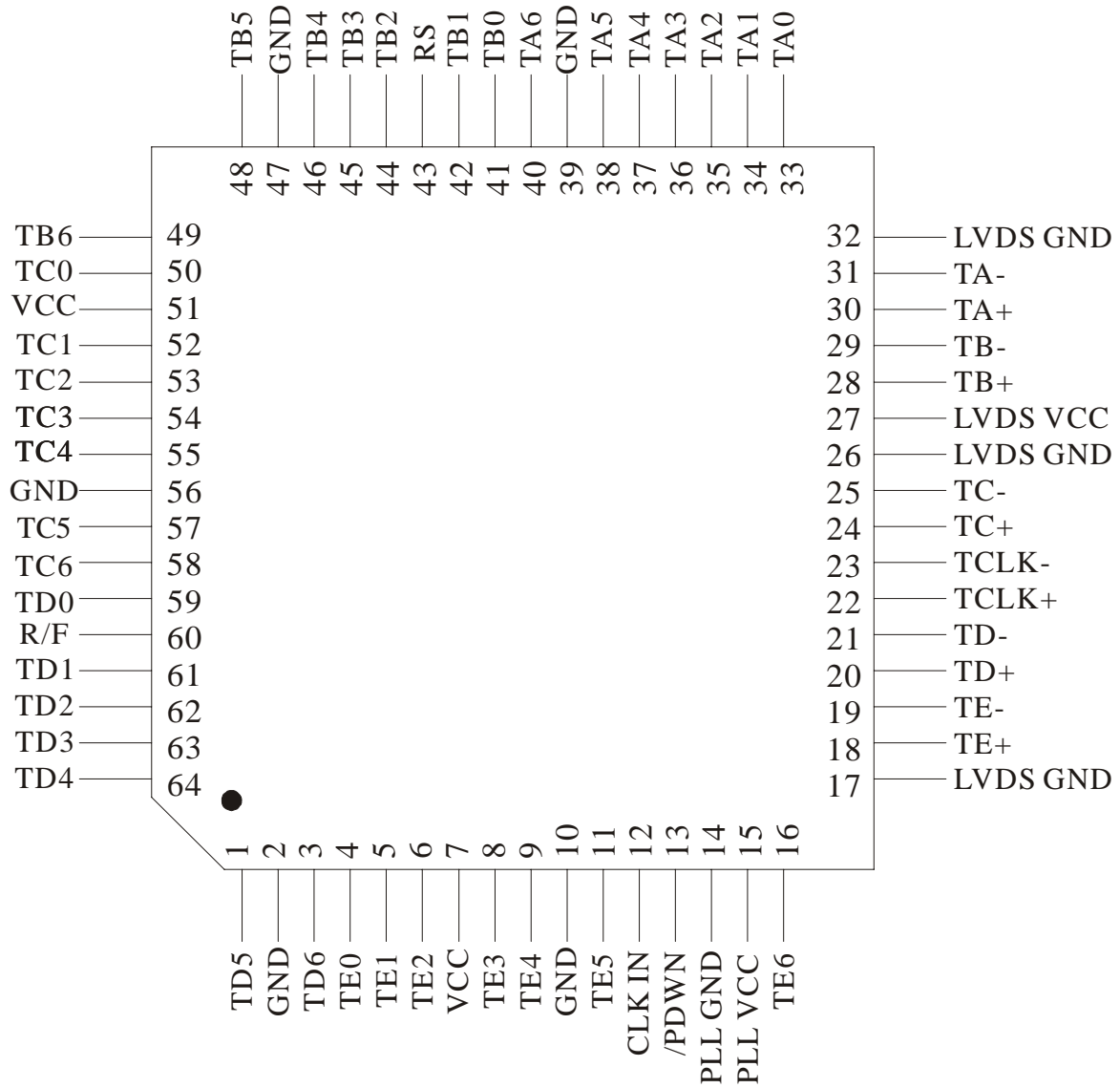
Features

- Wide dot clock range: 8-135MHz suited for NTSC, VGA, SVGA, XGA, SXGA and SXGA+
- PLL requires no external components
- Supports spread spectrum clock generator
- On chip jitter filtering
- Clock edge selectable
- Supports reduced swing LVDS for low EMI
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Backward compatible with
THC63LVDM63R(18bits) / M83R(24bits)

Block Diagram



Pin Out



Pin Description

| Pin Name | Pin # | Type | Description | | | | | | | | | | | | |
|--------------|----------------------|---------------------------|--|----|------------|---------------------------|-----|-------|-----|------------|-------|----------------------|-----|-------|-----|
| TA+, TA- | 30, 31 | LVDS OUT | LVDS Data Out. | | | | | | | | | | | | |
| TB+, TB- | 28, 29 | LVDS OUT | | | | | | | | | | | | | |
| TC+, TC- | 24, 25 | LVDS OUT | | | | | | | | | | | | | |
| TD+, TD- | 20, 21 | LVDS OUT | | | | | | | | | | | | | |
| TE+, TE- | 18, 19 | LVDS OUT | | | | | | | | | | | | | |
| TCLK+, TCLK- | 22, 23 | LVDS OUT | LVDS Clock Out. | | | | | | | | | | | | |
| TA0 ~ TA6 | 33,34,35,36,37,38,40 | IN | Pixel Data Inputs. | | | | | | | | | | | | |
| TB0 ~ TB6 | 41,42,44,45,46,48,49 | IN | | | | | | | | | | | | | |
| TC0 ~ TC6 | 50,52,53,54,55,57,58 | IN | | | | | | | | | | | | | |
| TD0 ~ TD6 | 59,61,62,63,64,1,3 | IN | | | | | | | | | | | | | |
| TE0 ~ TE6 | 4,5,6,8,9,11,16 | IN | | | | | | | | | | | | | |
| /PDWN | 13 | IN | H: Normal operation, L: Power down (all outputs are Hi-Z) | | | | | | | | | | | | |
| RS | 43 | IN | LVDS swing mode, VREF select. <table border="1" data-bbox="954 891 1374 1070"> <thead> <tr> <th>RS</th> <th>LVDS Swing</th> <th>Small Swing Input Support</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>350mV</td> <td>N/A</td> </tr> <tr> <td>0.6 ~ 1.4V</td> <td>350mV</td> <td>RS=VREF^a</td> </tr> <tr> <td>GND</td> <td>200mV</td> <td>N/A</td> </tr> </tbody> </table> a. VREF is Input Reference Voltage. | RS | LVDS Swing | Small Swing Input Support | VCC | 350mV | N/A | 0.6 ~ 1.4V | 350mV | RS=VREF ^a | GND | 200mV | N/A |
| RS | LVDS Swing | Small Swing Input Support | | | | | | | | | | | | | |
| VCC | 350mV | N/A | | | | | | | | | | | | | |
| 0.6 ~ 1.4V | 350mV | RS=VREF ^a | | | | | | | | | | | | | |
| GND | 200mV | N/A | | | | | | | | | | | | | |
| R/F | 60 | IN | Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge | | | | | | | | | | | | |
| VCC | 51, 7 | Power | Power Supply Pins for TTL inputs and digital circuitry. | | | | | | | | | | | | |
| CLKIN | 12 | IN | Clock in. | | | | | | | | | | | | |
| GND | 2, 10, 39, 47, 56 | Ground | Ground Pins for TTL inputs and digital circuitry. | | | | | | | | | | | | |
| LVDS VCC | 27 | Power | Power Supply Pins for LVDS Outputs. | | | | | | | | | | | | |
| LVDS GND | 17, 26, 32 | Ground | Ground Pins for LVDS Outputs. | | | | | | | | | | | | |
| PLL VCC | 15 | Power | Power Supply Pin for PLL circuitry. | | | | | | | | | | | | |
| PLL GND | 14 | Ground | Ground Pins for PLL circuitry. | | | | | | | | | | | | |

Absolute Maximum Ratings ¹

| | |
|----------------------------------|-----------------------------|
| Supply Voltage (V_{CC}) | -0.3V ~ +4.0V |
| CMOS/TTL Input Voltage | -0.3V ~ ($V_{CC} + 0.3V$) |
| CMOS/TTL Output Voltage | -0.3V ~ ($V_{CC} + 0.3V$) |
| LVDS Driver Output Voltage | -0.3V ~ ($V_{CC} + 0.3V$) |
| Junction Temperature | +125°C |
| Storage Temperature Range | -55°C ~ +150°C |
| Resistance to soldering heat | +260°C /10sec |
| Maximum Power Dissipation @+25°C | 1.0W |

1. “Absolute Maximum Ratings” are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Electrical Characteristics

CMOS/TTL DC Specifications

 $V_{CC} = 3.0V \sim 3.6V, T_a = 0^{\circ}C \sim +70^{\circ}C$

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------|--------------------------------------|--------------------------------|---------------------|-------------|---------------------|---------|
| V_{IH} | High Level Input Voltage | RS=VCC or GND | 2.0 | | V_{CC} | V |
| V_{IL} | Low Level Input Voltage | RS=VCC or GND | GND | | 0.8 | V |
| V_{DDQ}^1 | Small Swing Voltage | | 1.2 | | 2.8 | V |
| V_{REF} | Input Reference Voltage | Small Swing (RS= $V_{DDQ}/2$) | | $V_{DDQ}/2$ | | |
| V_{SH}^2 | Small Swing High Level Input Voltage | $V_{REF} = V_{DDQ}/2$ | $V_{DDQ}/2 + 100mV$ | | | V |
| V_{SL}^2 | Small Swing Low Level Input Voltage | $V_{REF} = V_{DDQ}/2$ | | | $V_{DDQ}/2 - 100mV$ | V |
| I_{INC} | Input Current | $0V \leq V_{IN} \leq V_{CC}$ | | | ± 10 | μA |

Notes: ¹ V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.

² Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0], TE[6:0] and CLKIN.

LVDS Transmitter DC Specifications

 $V_{CC} = 3.0V \sim 3.6V, T_a = 0^{\circ}C \sim +70^{\circ}C$

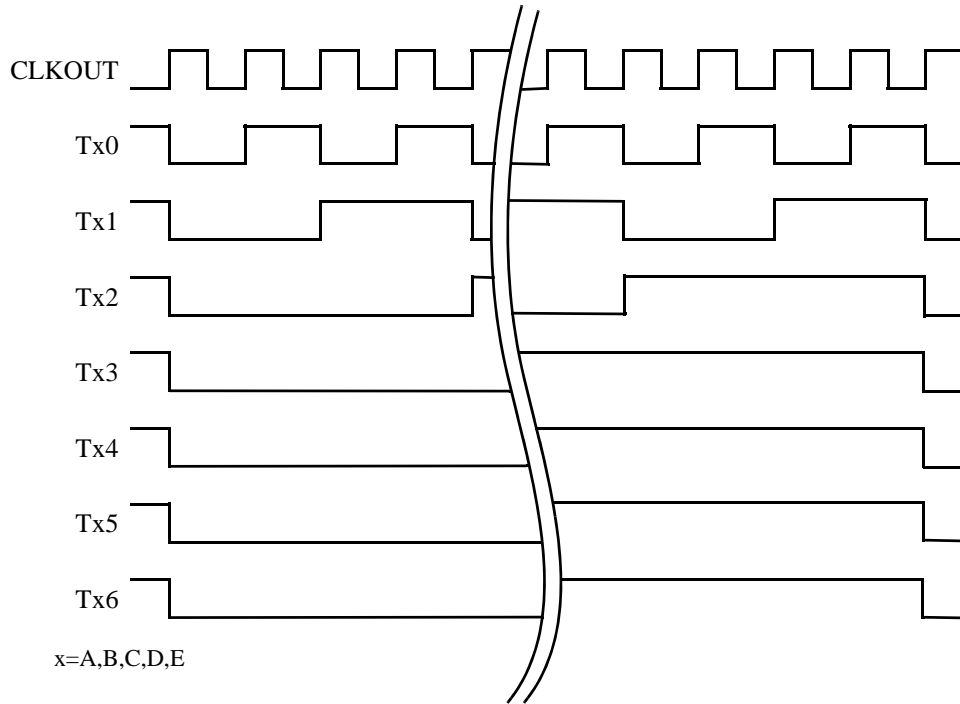
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------|---|--|-------|------|----------|---------|
| VOD | Differential Output Voltage | Normal swing RS=VCC RL=100 Ω | 250 | 350 | 450 | mV |
| | | Reduced swing RS=GND RL=100 Ω | 100 | 200 | 300 | mV |
| ΔVOD | Change in VOD between complementary output states | RL=100 Ω | | | 35 | mV |
| VOC | Common Mode Voltage | | 1.125 | 1.25 | 1.375 | V |
| ΔVOC | Change in VOC between complementary output states | | | | 35 | mV |
| I_{OS} | Output Short Circuit Current | VOUT=0V, RL=100 Ω | | | -24 | mA |
| I_{OZ} | Output TRI-STATE Current | /PDWN=0V, V _{OUT} =0V to VCC | | | ± 10 | μA |

Supply Current

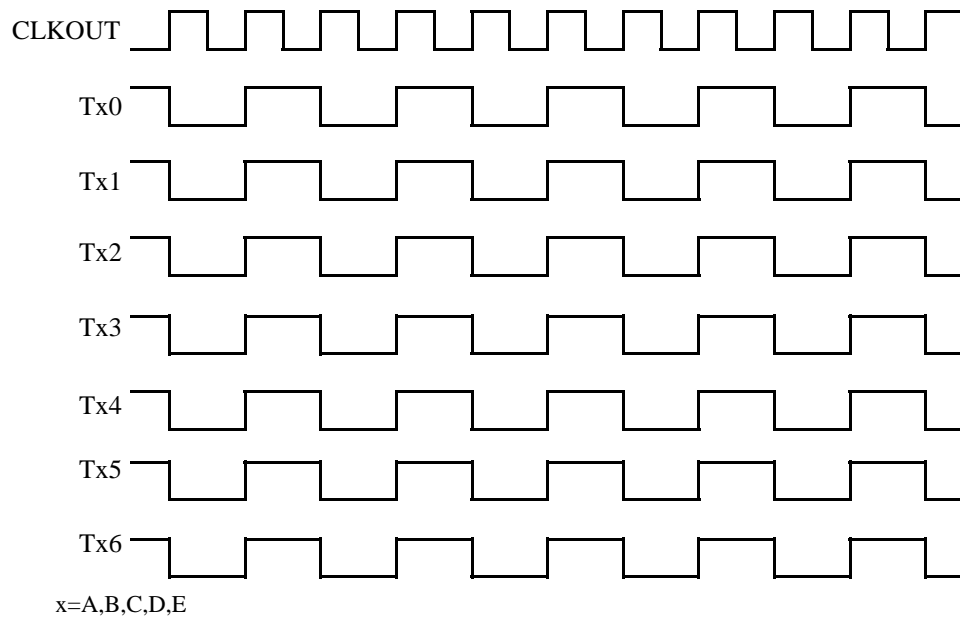
 $V_{CC} = 3.0V \sim 3.6V, T_a = 0^{\circ}C \sim +70^{\circ}C$

| Symbol | Parameter | Conditions | Typ. | Max. | Units |
|------------|----------------------------|--|------|------|-------|
| I_{TCCG} | Transmitter Supply Current | RL=100 Ω , CL=5pF f=85MHz V _{CC} =3.3V, RS=V _{CC} Gray Scale Pattern | 58 | 64 | mA |
| | | f=135MHz | 70 | 76 | mA |
| | | RL=100 Ω , CL=5pF f=85MHz V _{CC} =3.3V, RS=GND Gray Scale Pattern | 44 | 50 | mA |
| | | f=135MHz | 56 | 62 | mA |

Gray Scale Pattern



Worst Case Pattern



| Symbol | Parameter | Conditions | Typ. | Max. | Units | |
|-------------------|---------------------------------------|---|----------|------|-------|----|
| I _{TCCW} | Transmitter Supply Current | RL=100Ω, CL=5pF | f=85MHz | 69 | 75 | mA |
| | | V _{CC} =3.3V, RS=V _{CC} | f=135MHz | 87 | 93 | mA |
| | | Worst Case Pattern | | | | |
| | | RL=100Ω, CL=5pF | f=85MHz | 55 | 61 | mA |
| | | V _{CC} =3.3V, RS=GND | f=135MHz | 73 | 79 | mA |
| | | Worst Case Pattern | | | | |
| I _{TCCS} | Transmitter Power Down Supply Current | /PDWN = L | | 10 | μA | |

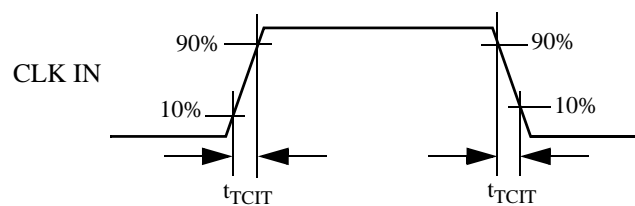
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

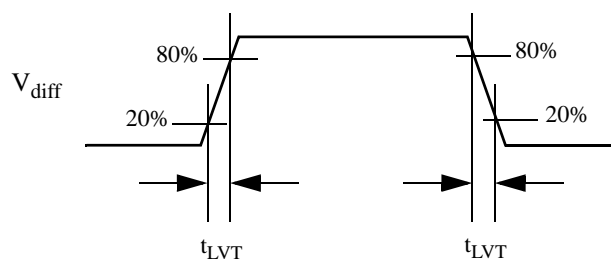
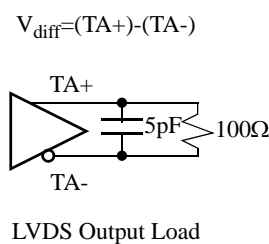
| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-------------------|---------------------------|----------------------------|----------------------|----------------------------|-------|
| t _{TCIT} | CLK IN Transition time | | | 5.0 | ns |
| t _{TCP} | CLK IN Period | 7.4 | | 125.0 | ns |
| t _{TCH} | CLK IN High Time | 0.35t _{TCP} | 0.5t _{TCP} | 0.65t _{TCP} | ns |
| t _{TCL} | CLK IN Low Time | 0.35t _{TCP} | 0.5t _{TCP} | 0.65t _{TCP} | ns |
| t _{TCD} | CLK IN to TCLK+/- Delay | | 3t _{TCP} | | ns |
| t _{TS} | TTL Data Setup to CLK IN | 2.5 | | | ns |
| t _{TH} | TTL Data Hold from CKL IN | 0 | | | ns |
| t _{LVT} | LVDS Transition Time | | 0.6 | 1.5 | ns |
| t _{TOP1} | Output Data Position0 | -0.2 | 0.0 | +0.2 | ns |
| t _{TOP0} | Output Data Position1 | $\frac{t_{TCP}}{7} - 0.2$ | $\frac{t_{TCP}}{7}$ | $\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TOP6} | Output Data Position2 | $2\frac{t_{TCP}}{7} - 0.2$ | $2\frac{t_{TCP}}{7}$ | $2\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TOP5} | Output Data Position3 | $3\frac{t_{TCP}}{7} - 0.2$ | $3\frac{t_{TCP}}{7}$ | $3\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TOP4} | Output Data Position4 | $4\frac{t_{TCP}}{7} - 0.2$ | $4\frac{t_{TCP}}{7}$ | $4\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TOP3} | Output Data Position5 | $5\frac{t_{TCP}}{7} - 0.2$ | $5\frac{t_{TCP}}{7}$ | $5\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TOP2} | Output Data Position6 | $6\frac{t_{TCP}}{7} - 0.2$ | $6\frac{t_{TCP}}{7}$ | $6\frac{t_{TCP}}{7} + 0.2$ | ns |
| t _{TPLL} | Phase Lock Loop Set | | | 10.0 | ms |

AC Timing Diagrams

TTL Input

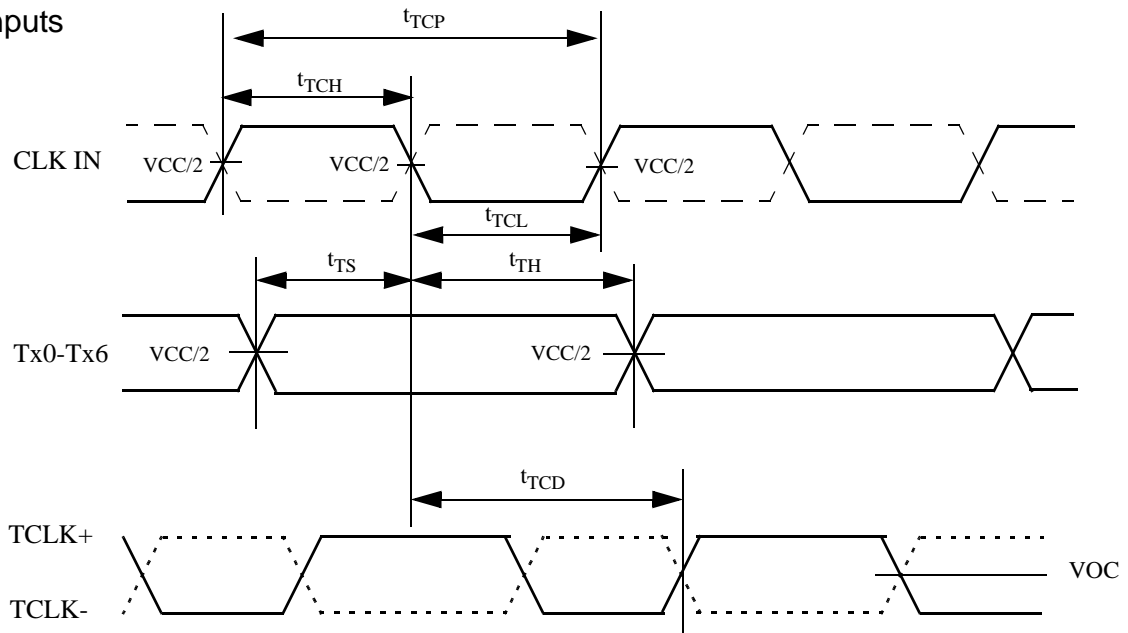


LVDS Output



AC Timing Diagrams

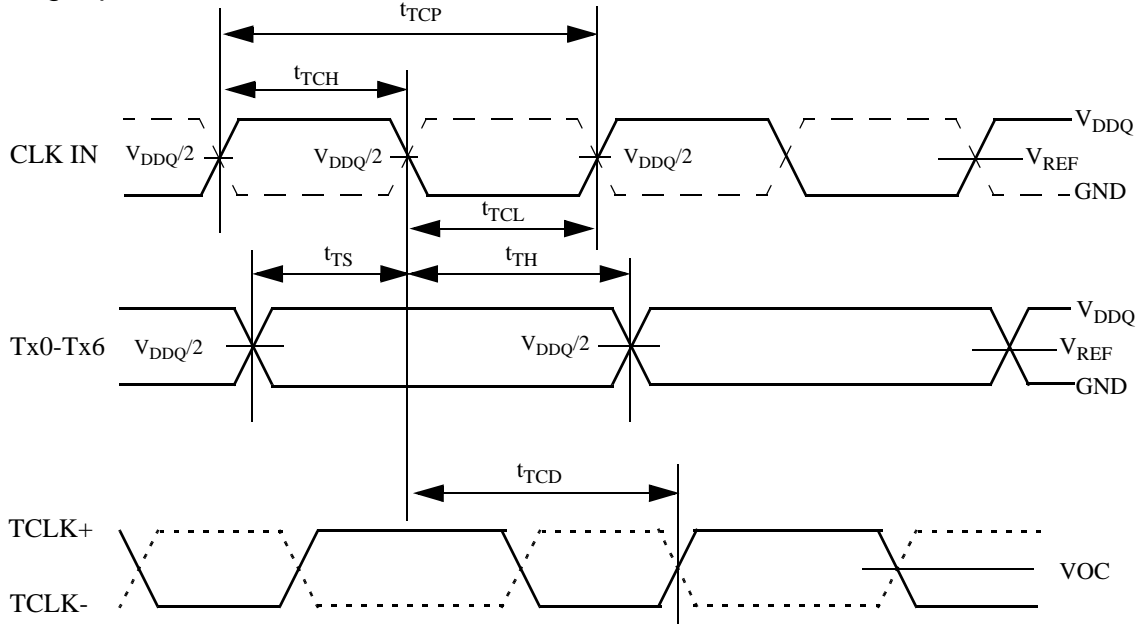
TTL Inputs



Note:

CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

Small Swing Inputs

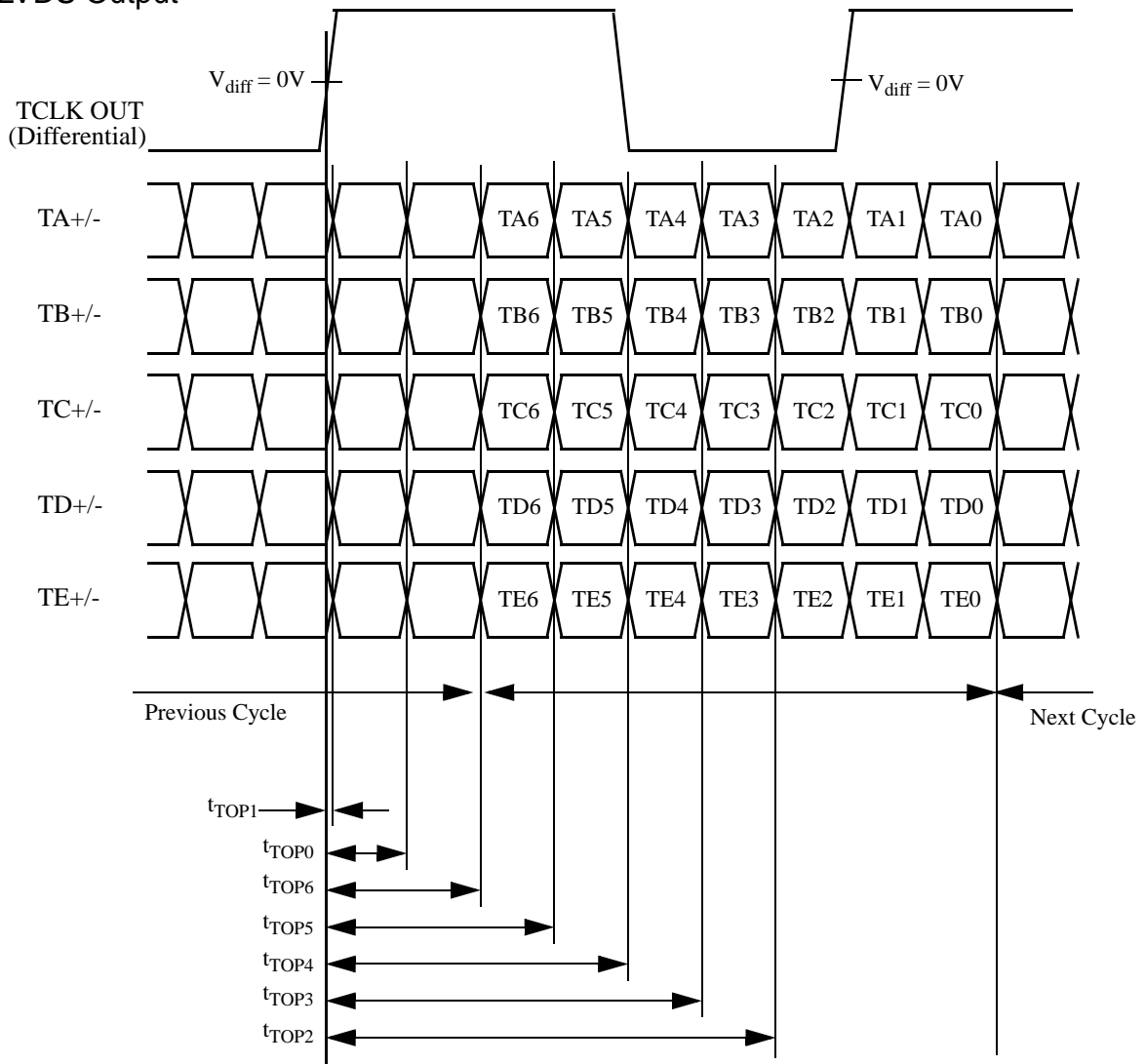


Note:

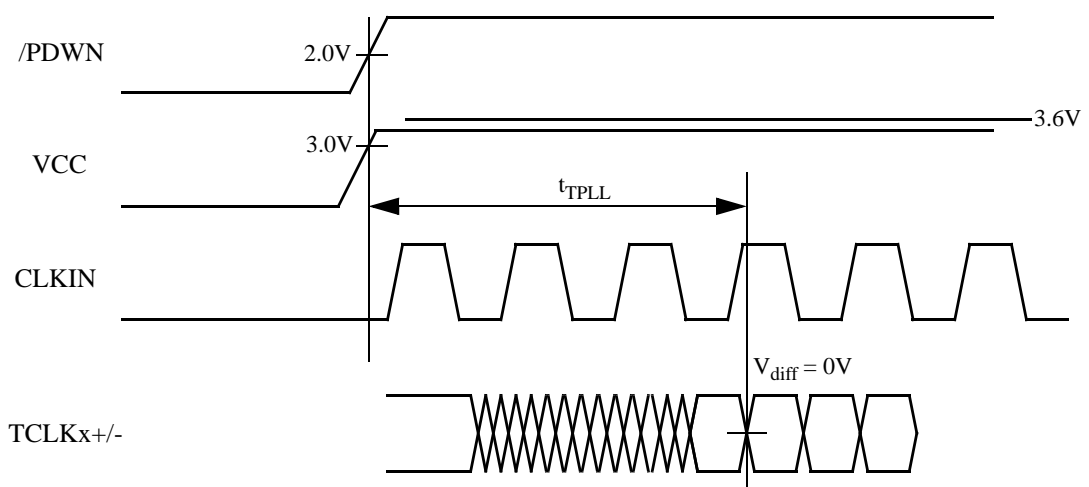
CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

AC Timing Diagrams

LVDS Output

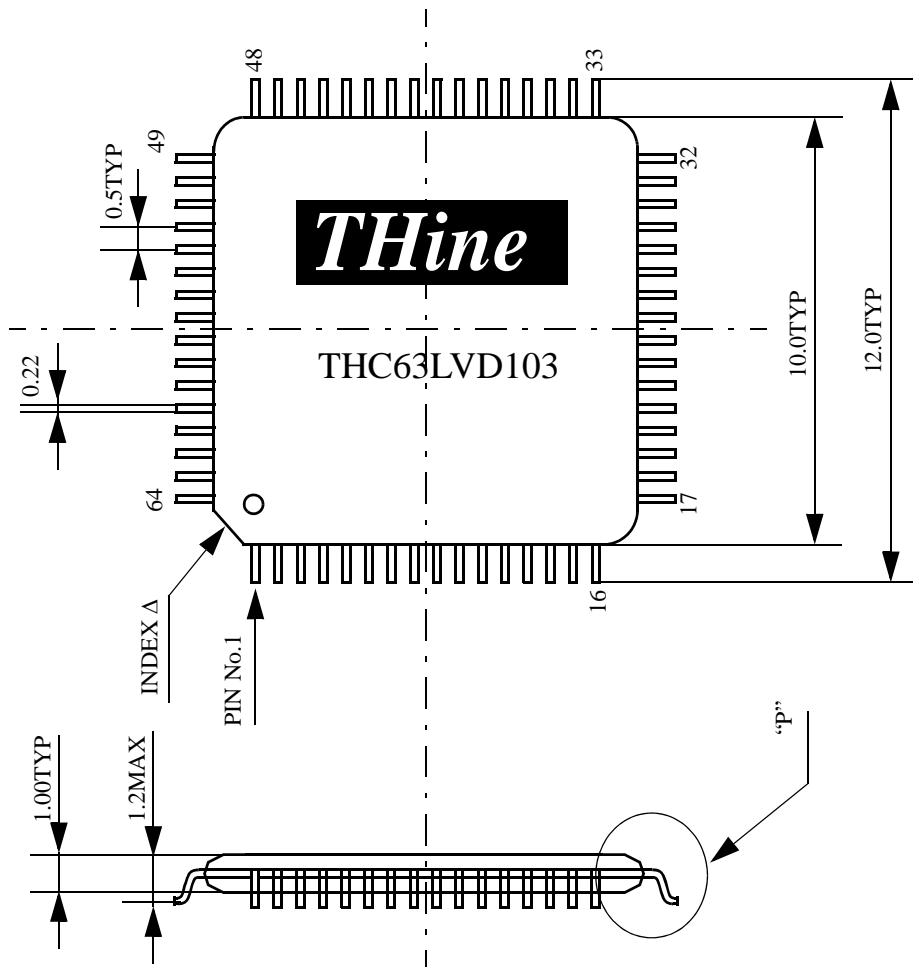


Phase Lock Loop Set Time



Package

64 Pin TQFP ,JEDEC



UNITS: mm

Notes to Users:

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