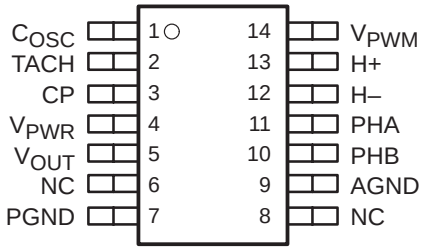
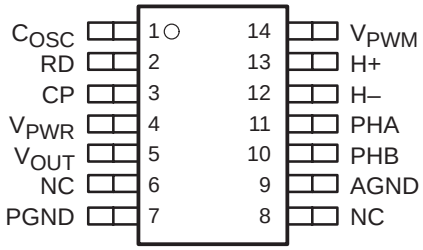
- **DC Fan Drive Speed Control With No External Power Drive Stage Required**
- **11% to 100% PWM Range Adjustable Via 0–2.5 V DC Control Voltage – Suited for Cooling Fan Applications Requiring Variable RPM to Reduce Noise and/or Increase MTBF**
- **Speed Control Capability With Either DC or PWM Input Signal for Greater System-Level Flexibility**
- **Sleep-State Mode to Eliminate External Fan ON/OFF Power Device – Suited for Cooling Fans in *Instantly Available* PCs**
- **Thermal Shutdown Protection**
- **High Impedance V_{PWM} Input for Speed Control of Multiple Fans With a Single Signal**
- **Locked Rotor Protection (THMC40, THMC41) With Open-Drain Output Indication (THMC41)**
- **Open-Drain Tachometer Signal Valid Over Entire RPM Range (THMC40)**
- **Noise Immune Signal Conditioning to Allow Use of Low-Cost Hall Effect Position Sensor**
- **Patented High Efficiency Drive Topology With Integrated Low $R_{DS(ON)}$ LDMOS Output Drivers**

THMC40 . . . TACH OUTPUT
14-Pin SOP D Package
(TOP VIEW)



THMC41 . . . RD OUTPUT
14-Pin SOP D Package
(TOP VIEW)



description

The THMC40 and THMC41 are 2-phase, dc brushless motor (BLM) drive and control devices intended for use with 12-Vdc cooling fans. Both devices include a high-efficiency PWM drive topology using integrated 0.5-Ω (typical) LDMOS drivers, plus a speed control input stage to provide the industry's first solution for efficient speed control *inside* dc cooling fans. This patented solution eliminates the need for power drive components on the main system board, thus reducing printed-circuit board (PCB) component count, PCB space, and assembly time. This solution also offers other advantages over the two commonly used fan speed control methods, adjustable external dc supply voltage, and adjustable external PWM drive duty cycle.

Unlike other methods which control speed external to the cooling fan, the THMC40 and THMC41 high-efficiency PWM drive stage adjusts only the level of motor phase winding power. All other circuitry inside the fan obtains power from the fixed dc voltage fan supply. This method eliminates the typical problem associated with an external dc voltage regulation method causing loss of headroom to internal control circuitry at low fan supply voltage and the resulting limitation of low-speed operation to ≈40%. The PWM drive method employed by the THMC40 and THMC41 also reduces fan supply power consumption over the external linear regulation method, which has V×I power loss due to the voltage drop across the regulator.

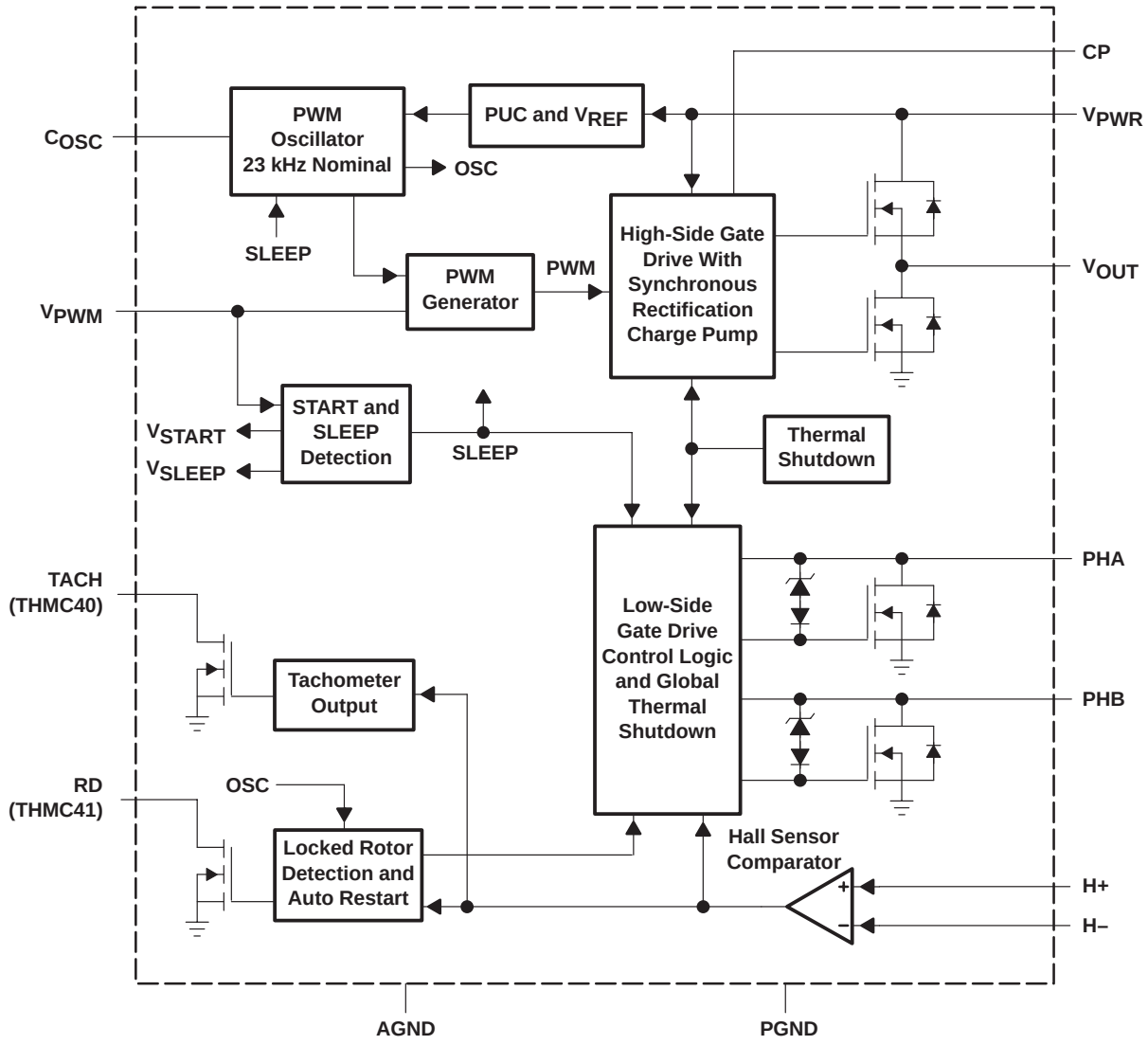
An external PWM drive method disrupts power to the motor and also to all internal fan circuitry. The THM40 and THMC41 solution maintains all signal integrity with phase drive commutation and tachometer, while providing reliable low speed fan operation down to 11% PWM. This method allows fan health monitoring over the full fan speed range.

description (continued)

The V_{OUT} duty cycle, and thus the motor speed, is proportional to the voltage present at the V_{PWM} input terminal. This terminal allows controlling the fan speed via a DAC output from an external control IC or an RC-filtered PWM output from a PC Super I/O chip.

The THMC40 and THMC41 have an internal Hall sensor amplifier and signal conditioner, global thermal shutdown, locked rotor protection, and automatic restart after a locked rotor condition. The THMC40 provides an open-drain tachometer output signal, while the THMC41 provides an open-drain locked rotor detection output signal. These devices also provide a sleep-state mode to eliminate the need for an external power component to disconnect the fan from the supply during a system sleep state or *instantly available* power down. The THMC40 and THMC41 are primarily intended for cooling fan applications that require RPM speed control and the availability of a tachometer or locked rotor detection signal.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	9	I	IC analog ground and substrate connection
CP	3	I	External charge pump capacitor
C_{OSC}	1	I/O	External oscillator capacitor
H–	12	I	Hall sensor negative input
H+	13	I	Hall sensor positive input
NC	6, 8	–	No connection
PGND	7	I	Power ground for high-side charge pump
PHA	11	O	Low-side driver for phase A motor winding
PHB	10	O	Low-side driver for phase B motor winding
RD	2	O	Open-drain locked rotor detection output—THMC41 only
TACH	2	O	Open-drain tachometer output signal—THMC40 only
V_{OUT}	5	O	High-side PWM driver output for motor windings
V_{PWR}	4	I	Supply voltage input
V_{PWM}	14	I	PWM duty cycle control voltage input

absolute maximum ratings over operating case temperature range (unless otherwise noted)† (see Note 1)

Supply voltage input, V_{PWR} . . . . . 18 V
High-side driver, PWM output voltage, V_{OUT} . . . . . 18 V
Low-side drivers, phase A and B output, V_{PHA}, V_{PHB} . . . . . 40 V
Hall sensor amplifier input voltage, V_{H+}, $V_{H–}$ . . . . . 7 V
PWM duty cycle control input voltage, V_{PWM} . . . . . 7 V
Open-drain tachometer output voltage (THMC40), V_{TACH}, or open-drain RD output voltage (THMC41), V_{RD} . . . . . 7 V
Oscillator capacitor voltage, V_{COSC} . . . . . 7 V
Charge pump capacitor voltage, V_{CP} . . . . . 30 V
Continuous high-side PWM output source/sink current, I_{OUT} . . . . . 1.5 A
Continuous low-side PWM output sink current, I_{PHA}, I_{PHB} . . . . . 1.5 A
Junction-to-case thermal resistance, $R_{\theta JC}$ . . . . . 26.9°C/W
Junction-to-ambient thermal resistance , $R_{\theta JA}$ (see Note 2) . . . . . 122.3°C/W
Continuous power dissipation at 25°C , P_D (see Note 3) . . . . . 1022 mW
Power derating factor above 25°C ambient , $P_{DERATING}$ (see Note 4) . . . . . 8.18 mW/°C
Operating case temperature range, T_C . . . . . –30°C to 80°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (soldering, 10 sec), T_{LEAD} . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. JEDEC low-K board with 0 LFM airflow
3. 150°C maximum junction temperature, JEDEC low-K board with 0 LFM airflow
4. 80°C maximum ambient and 150°C maximum junction temperature

dc electrical characteristics, V_{PWR} = 12 V, T_A = – 30°C to 80°C (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{PWR}	Supply voltage range		11	12	13	V
I_{VPWR}	V_{PWR} supply current	Idle condition in locked rotor detect		2.5	5	mA
		I_{LOAD} = –1 A, V_{OUT} low, T_A = 25°C		5		mA
I_{SLEEP}	Sleep-state current	$V_{PWM} \le 0.4$ V		300	400	µA

PHA, PHB low-side phase winding driver outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{LEAK}	PHA,PHB output leakage current	Output = OFF, V_{PHx} = 12 V		0.1	10	µA
V_{OL}	PHA, PHB low-level output voltage	Output = ON, I_{PHx} = 1 A, T_A = 25°C		0.5	0.6	V
$R_{DS(ON)}$	PHA, PHB output ON resistance	Output = ON, I_{PHx} = 1A, T_A = 25°C		0.5	0.6	Ω
V_{CLAMP}	PHA, PHB output active clamp voltage	Output = OFF, I_{PHx} = 200 mA	32	38		V

Hall sensor signal conditioning

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{IB(HL)}$	Hall input bias current			±0.1	±1	µA
$V_{ICR(HL)}$	ICR(HL) common-mode input voltage range		1		3.5	V
V_{IO}	Hall comparator input offset voltage	Over $V_{ICR(HL)}$ = 1 V to 3.5 V	–7	0	7	mV

V_{OUT} high-side phase winding driver output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{LEAK}	V_{OUT} output sleep-state leakage current	Sleep state engaged, V_{VOUT} = 0 V to V_{PWR}		±0.1	±10	µA
V_{OH}	V_{OUT} high-level output voltage	Run state, Output high I_{VOUT} = –1 A, T_A = 25°C		V_{PWR} – 0.4	V_{PWR} – 0.6	V
$R_{DS(ON)}$	V_{OUT} output high-side resistance to V_{PWR}			0.4	0.6	Ω
V_{RECIR}	V_{OUT} output recirculation voltage	Run state, Output low I_{VOUT} = –1 A, T_A = 25°C		– 0.3	– 0.5	V
$R_{DS(ON)(SYNC)}$	V_{OUT} synchronous switch resistance to PGND			0.3	0.5	Ω
I_{LIMIT}	Pulsed V_{OUT} synchronous rectification current limit	Run state, V_{OUT}=V_{PWR}=12V, V_{COSC} > V_{PWM}, t_{PULSE} = 100 µs, See Note 5	2	2.6		A

CP high-side gate drive charge pump capacitor input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CP}	Charge pump voltage	I_{VCP} = –60 µA, V_{PWM} = 2.5 V	22	26		V
$V_{CP(UVLO)}$	V_{CP} undervoltage lock-out		6.5	7.6	8.5	V

C_{OSC} external oscillator capacitor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CHARGE}	C_{OSC} charge source current	V_{COSC} = 1.4 V, Charge mode	–130	–180	–230	µA
$I_{DISCHARGE}$	C_{OSC} discharge sink current	V_{COSC} = 1.4 V, Discharge mode	130	180	230	µA
$V_{DISCHARGE}$	C_{OSC} upper threshold for switching to current sink		2	2.3	2.6	V
V_{CHARGE}	C_{OSC} lower threshold for switching to current source		0.43	0.5	0.57	V

NOTE 5: V_{OUT} current limit, in conjunction with thermal shutdown function, provides device survivability under V_{OUT}-to-V_{PWR} short condition.

dc electrical characteristics, V_{PWR} = 12 V, T_A = –30°C to 80°C (unless otherwise noted) (continued)

V_{PWM} high-side PWM duty cycle adjust input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{IB(PWM)}$	V_{PWM} input bias current	V_{PWM} = 0 V to 3 V			±1	µA
V_{PWM} (100%)	V_{PWM} voltage equivalent to 100% duty cycle			2.3		V
V_{SLEEP}	V_{PWM} voltage threshold to engage sleep mode		0.6	0.7		V
V_{START}	V_{PWM} voltage threshold to disengage sleep mode			0.8	0.9	V

thermal shutdown characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{TSD}	V_{OUT}, PHA, PHB global thermal shutdown thresholds	Temperature increasing until outputs are off, See Note 6	150		185	°C
T_{HYST}	Thermal shutdown hysteresis	After T_{TSD}, temperature decreasing until outputs return to normal operation, See Note 6		15		°C

TACH Tachometer open-drain output (THMC40)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{TACHLEAK}$	TACH high-level output leakage current	V_{TACH} = 5 V		0.1	1	µA
V_{OL}	TACH low-level output voltage	I_{TACH} = 5 mA		0.1	0.3	V

RD locked rotor detection open-drain output (THMC41)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{RDLEAK}	RD high-level output leakage current	V_{RD} = 5 V, Locked rotor condition		0.1	1	µA
V_{OL}	RD low-level output voltage	I_{RD} = 5 mA, No locked rotor		0.1	0.3	V

ac electrical characteristics, V_{PWR} = 12 V, T_A = –30°C to 80°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{PWM}	High-side gate drive PWM frequency	C_{OSC} = 2200 pF		22.7		kHz
t_{RD}	Locked rotor detect delay time	C_{OSC} = 2200 pF, See Figure 9		1		s
t_{RETRY}	Auto-restart delay time			8		s
t_{HALL}	Hall zero-crossing deglitch time	See Figure 2		25		µs
$t_{DEAD(PHx)}$	Dead time between phase commutations			5		µs
$t_{f(OUT)}$	V_{OUT} output fall time	R_L = 20 Ω , L_L = 5 mH, See Note 6		25		ns
$t_{r(OUT)}$	V_{OUT} output rise time			25		ns
$t_{f(PHx)}$	PHA or PHB fall time			1		µs
$t_{r(PHx)}$	PHA or PHB rise time			1		µs

NOTE 6: Design targets only. Not tested in production.

PRINCIPLES OF OPERATION

general overview

The THMC40 and THMC41 are 2-phase dc brushless fan motor drivers with PWM speed control intended primarily for applications requiring a wide speed control range and an open-drain tachometer output signal (THMC40), or a locked rotor detection output (THMC41). The V_{OUT} drive duty cycle, and thus fan speed, is proportional to the voltage level at the V_{PWM} input terminal. Each device has an internal Hall sensor comparator/signal conditioner, a low power sleep-state mode, locked rotor protection with automatic restart after a locked rotor condition, and over-temperature protection. The tachometer signal (THMC40) can be used to monitor the *health* of the fan or to close an external loop based on fan RPM. The THMC40 and THMC41 provide a more efficient drive solution to fan RPM control than external linear voltage control. This solution is also considerably more efficient than controlling dc brushless fan RPM using external PWM drive.

low-side motor phase winding driver outputs (PHA, PHB)

The PHA and PHB outputs provide low-side drive of the motor's two stator phase windings (see block diagram and Figure 1). These outputs have a typical $R_{DS(ON)}$ of 400 mΩ at 25°C and a 1-A continuous current rating. The PHA and PHB outputs have an active flyback clamp (V_{ZCLAMP} in Figure 1) of 38 V (typical) to snub inductive energy when a phase drive switches off. The outputs also have global thermal shutdown to prevent device failure.

Drive commutation of PHA and PHB outputs is controlled according to rotor position monitored by a Hall-effect position sensor. Discussion of this function is found in the following section, and the relationship between PHA and PHB outputs to Hall input signal is shown in Figure 2.

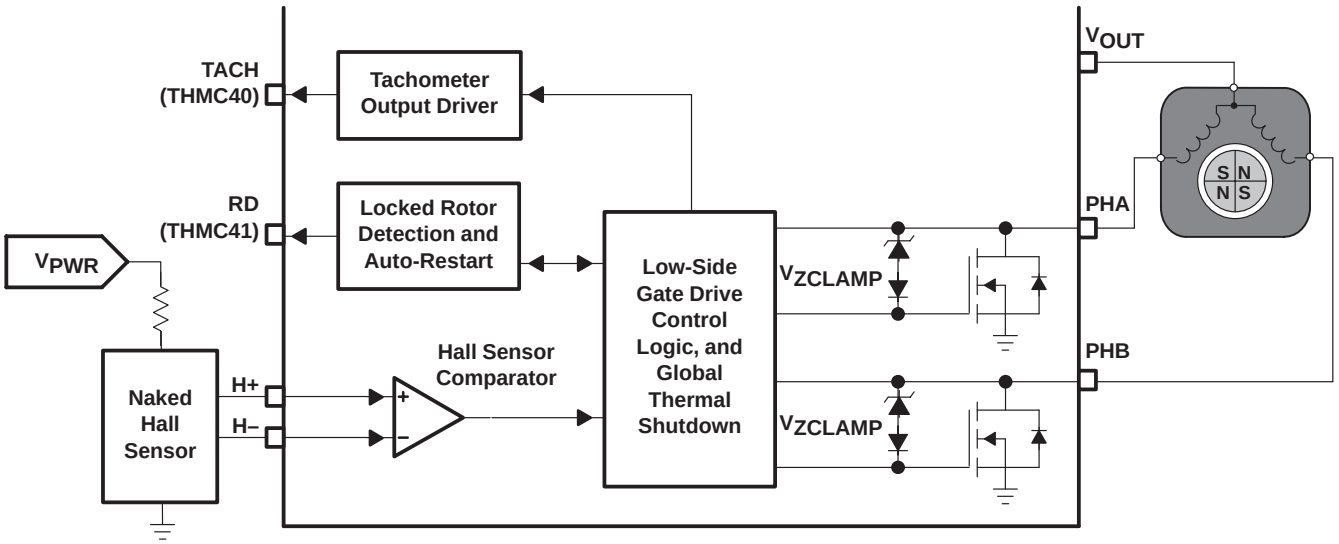


Figure 1. Low-Side Gate Drive Block Diagram

Hall sensor comparator and signal conditioning inputs (H+, H–)

Referring to Figure 1, the THMC40 and THMC41 have an internal Hall sensor comparator allowing the use of low-cost naked Hall sense elements. The Hall signal conditioning block receives a low-level differential voltage from the naked Hall position sensor element. The comparator then implements a zero differential voltage crossing detection with a deglitch time of 25 μs (typical) to reject noise on the Hall signal inputs. Referring to Figure 2, the PHx drive that was on (low) turns off after the 25-μs deglitch time is reached. Then the opposite PHx drive turns on after another delay time. This 5-μs (typical) *dead time* is implemented to prevent both phases from conducting simultaneously and to allow time for the inductive energy to be snubbed from the phase that was just turned off. The Hall comparator circuit has an input offset voltage (V_{IO}) which is not greater than ±7 mV. The common-mode input voltage range is 1 V to 3.5 V (see Figure 2).

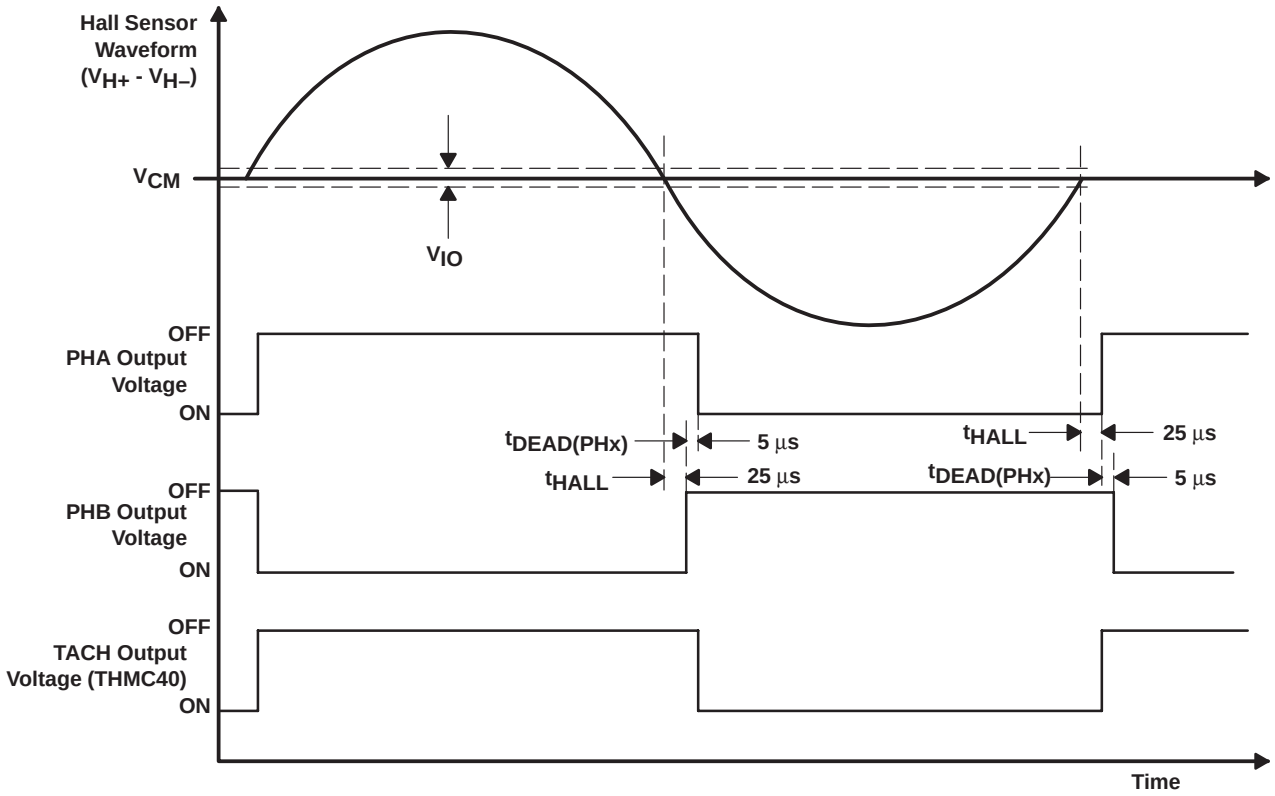


Figure 2. Hall Sensor Signal Conditioning Waveforms

Table 1 shows PHA and PHB commutation, and TACH output (THMC40) functionality:

Table 1. PHA and PHB Low-Side Drive Commutation and TACH Functionality

H+	H–	PHA	PHB	TACH (THMC40)
+	–	High (OFF)	Low (ON)	High (OFF)
–	+	Low (ON)	High (OFF)	Low (ON)

high-side PWM output driver (V_{OUT})

Referring to Figure 3, V_{OUT} is a drive output to provide PWM controlled power to the common node of the motor phase windings using an internally generated PWM signal. The PWM duty cycle controls the effective drive power to the motor, and thus motor speed. The high-side V_{OUT} DMOS output transistor has a typical $R_{DS(ON)}$ of 400 mΩ at 25°C and a 1-A continuous current.

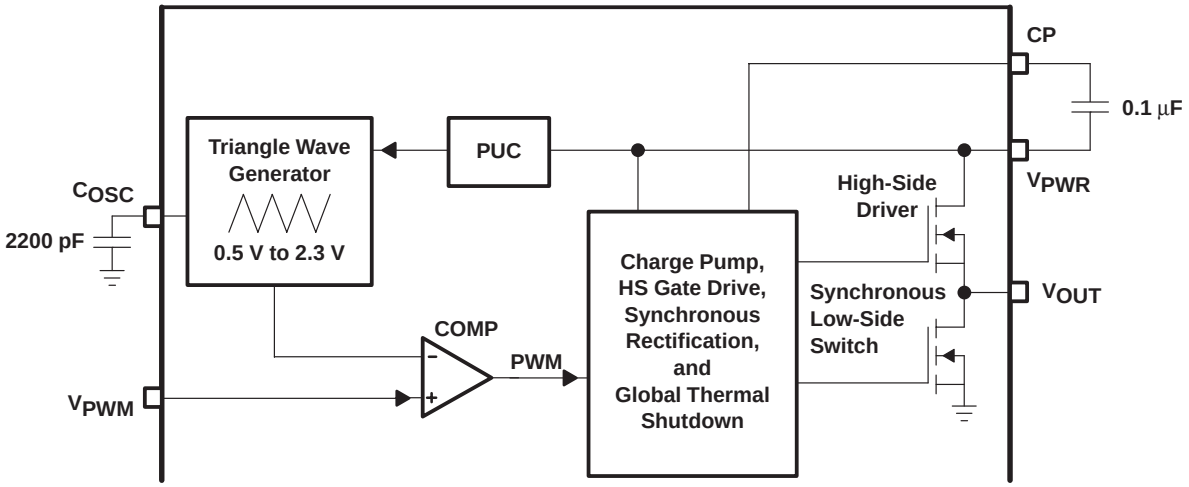


Figure 3. High-Side PWM Drive

The frequency of the PWM drive (typically 23 kHz) is such that the L/R time constant of the motor phase winding filters the current. Referring to Figure 4, during the on-time (t_{ON}) of a PWM period, V_{OUT} is driven high forcing voltage across a phase winding and increasing the current. During t_{OFF}, PWM off-time, the V_{OUT} high-side DMOS is switched off, the phase winding inductive energy is recirculated, and the current decreases. To minimize the voltage drop and the resulting energy loss during recirculation, a low-side DMOS synchronous switch is provided, as shown in Figure 3. This low-side DMOS device has a 2-A minimum current limit to prevent device failures should a solder bridge occur between the adjacent V_{PWR} and V_{OUT} terminals.

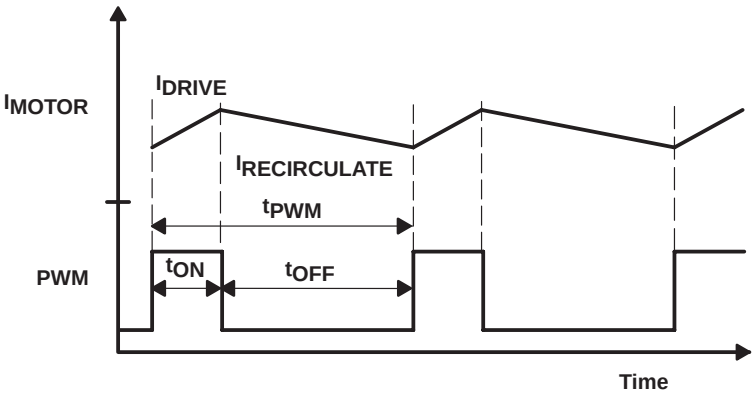


Figure 4. Motor Current Waveform

The V_{OUT} circuit is protected by the global thermal shutdown of the THMC40 and THMC41 by turning off both the high-side and low-side DMOS drivers when an over-temperature condition is detected. V_{OUT} is also held off when the charge-pump voltage (V_{CP}) is lower than its undervoltage lock-out threshold, $V_{CP(UVLO)}$.

charge pump (CP)

THMC40 and THMC41 have an internal charge pump which utilizes an external reservoir capacitor (CP) to generate the gate-drive voltage for the V_{OUT} output high-side DMOS transistor (see Figure 3). The recommended value for CP is 0.1 μF, with a minimum rating of 35 WVdc. The charge pump is disabled during the sleep state (see the sleep/run state section) to minimize current consumption into V_{PWR}. The charge pump also incorporates internal undervoltage lockout detection used to disable V_{OUT} when the charge pump voltage does not have an adequate level above V_{PWR} to fully drive the high-side DMOS gate. Thus, the V_{CP} (UVLO), in conjunction with the charge pump start-up time, delays the V_{OUT} drive for a short time after the device has transitioned from sleep to run state, until the charge pump voltage reaches the UVLO threshold.

PWM oscillator/triangle waveform generator (C_{OSC})

The PWM oscillator uses source and sink currents switched into an external capacitor (C_{OSC}) to set the PWM frequency and generate a triangle waveform. A PWM oscillator cycle consists of charging C_{OSC} with a constant current source (–180 μA typical) until the C_{OSC} voltage ramps up to an upper threshold (2.3 V typical), and then discharging C_{OSC} with a constant current sink (180 μA typical) until the C_{OSC} voltage ramps down to a lower threshold (0.5 V typical). The charge/discharge cycle is repeated each time the 2.3-V or 0.5-V threshold is reached (see Figure 5).

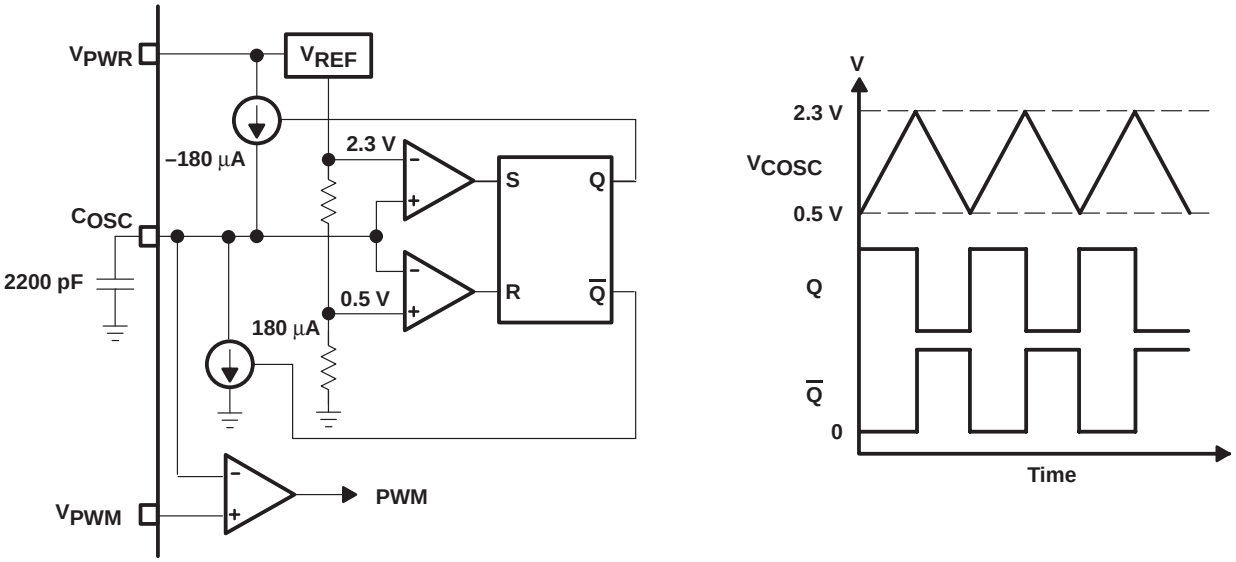


Figure 5. PWM Triangle Waveform Generator

The following equation can be used to calculate the value of C_{OSC} needed for a desired PWM frequency, f_{PWM}:

$$C_{OSC(max)} = \frac{I_{CHARGE(min)}}{2 \times f_{PWM(min)} \times \left(V_{DISCHARGE} - V_{CHARGE}\right)}$$

PWM duty cycle control voltage (V_{PWM}) – dc control voltage input

The voltage at the V_{PWM} terminal determines the PWM duty cycle of the output (V_{OUT}) to control drive power to the fan motor, and thus control fan speed (see Figures 3 and 6). The V_{PWM} voltage is internally compared against the 0.5-V to 2.3-V triangle waveform generated on the C_{OSC} terminal. The PWM signal output from this comparator has a duty cycle proportional to the voltage at V_{PWM}, as shown in Figure 6. The output of this comparator is used as the PWM input to the V_{OUT} drive stage.

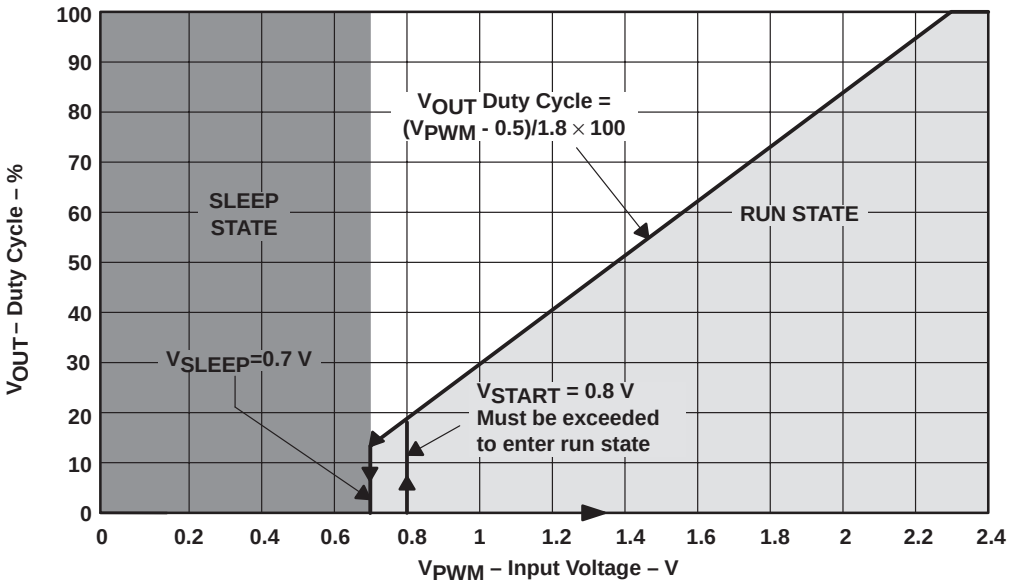
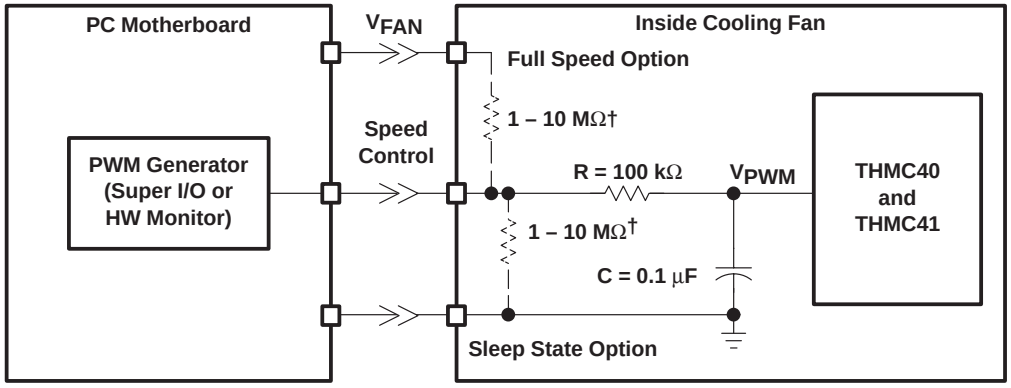


Figure 6. Relationship of V_{OUT} Duty Cycle, V_{START}, and V_{SLEEP} vs V_{PWM} Input Voltage

PWM duty cycle control voltage (V_{PWM}) – digital PWM control input

To allow control of the THMC40 and THMC41 by either a PWM or a dc input control signal, it is recommended that the fan manufacturer includes a 100-kΩ, 0.1-μF RC filter between the speed control wire and the V_{PWM} terminal (see Figure 7). This method allows the end user to control the fan speed with either a PWM signal or a dc control voltage. Many PC Super I/O ICs and hardware monitoring ICs provide one of the two fan speed control outputs. Therefore, fans with THMC40 and THMC41 ICs can be used with a wide variety of control schemes to provide variable fan speed without an external fan drive power stage.



† Optional resistors control fan operation with open speed control input.

Figure 7. PWM Input Control With RC Filter Inside the Cooling Fan

PWM duty cycle control voltage (V_{PWM}) – digital PWM control input (continued)

Figure 8 illustrates the relationship between V_{OUT} output duty-cycle and a 0–3.3-V digital PWM input control signal.

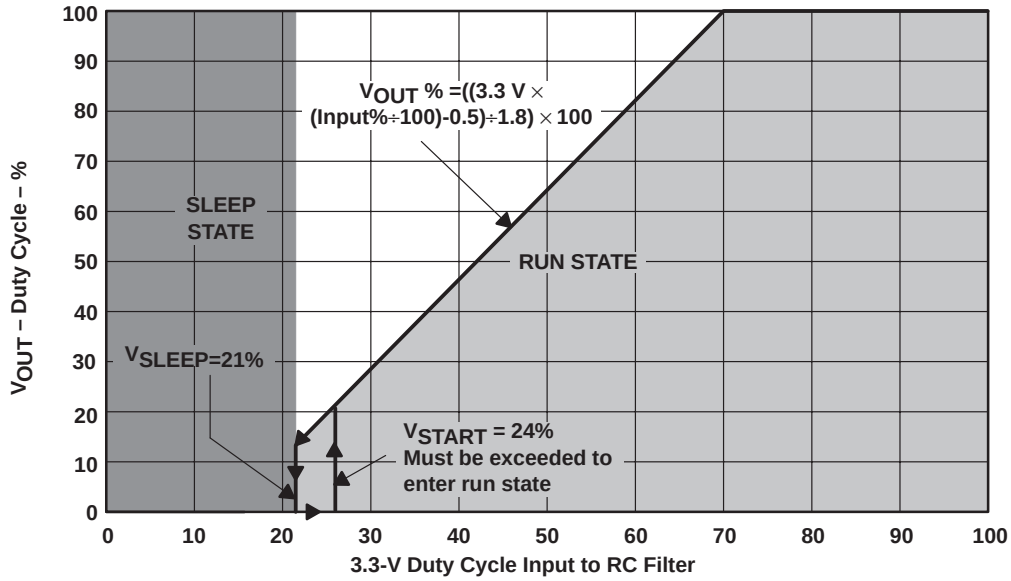


Figure 8. Relationship of V_{OUT} Duty Cycle, V_{SLEEP}, V_{START} vs 0–3.3 V PWM Input Duty Cycle

sleep/run state

Sleep-state and run-state modes are provided, as illustrated in Figures 6 and 8. The sleep state is intended to minimize V_{PWR} (fan) supply current requirements (300 μA typical) when cooling fan operation is not required. This feature is especially beneficial for PC OEMs needing to meet the *instantly available* PC requirements without the use of additional external circuitry.

The sleep state is engaged when the V_{PWM} input voltage is below the V_{SLEEP} threshold (0.7 V typical, 11.1% duty cycle). During the sleep state, all output drivers are turned off and any unused circuits are powered down to minimize current drain. Once sleep state is engaged, V_{PWM} must exceed the V_{START} threshold (0.8 V typical, 17% duty cycle) to disable the sleep state and enter the run state, allowing the motor to be driven. Once the run state is engaged, outputs V_{OUT}, PHA, and PHB are active and the V_{PWM} voltage can be decreased to obtain minimum fan speed down to the V_{SLEEP} threshold. This procedure allows the user to overcome initial motor stiction with a PWM duty cycle of 17% to avoid the possibility of false locked rotor detection during initial start-up. See Figure 6 for the V_{PWM} input voltage relationship to sleep mode and V_{OUT} duty cycle.

A control device with a voltage range of 0 V to 2.5 V is recommended to provide the adjustable V_{PWM} reference voltage to the THMC40 and THMC41. A 2.5-V DAC is an optimal choice as the controlling circuitry, whether as a stand-alone device, or as an integrated function in a multiple-function device. Using a control device without a minimum 0.5-V to 2.3-V range reduces the RPM control range of the fan motor and may not allow duty-cycle settings of 0% and/or 100%.

thermal shutdown

The THMC40 and THMC41 provide protection against excessive device temperature with a thermal sensor that monitors the die temperature. Should some operating or abnormal condition cause the die temperature to exceed T_{TSD}, the thermal shutdown threshold (165°C typical), all output drivers are turned off. Once T_{TSD} has been exceeded, the die temperature must fall below a hysteresis temperature (typical T_{TSD} –15°C) before the output drivers are re-enabled.

locked rotor protection

An internal digital timer monitors the output of the Hall sensor amplifier. When a change in commutation state is not observed within one second (typical with 2200 pF C_{OSC}), the V_{OUT}, PHA, and PHB outputs are disabled for eight seconds (typical with 2200 pF C_{OSC}). After the outputs have been disabled for eight seconds (typical with 2200 pF C_{OSC}), the THMC40 and THMC41 re-enable the V_{OUT}, PHA, and PHB outputs to automatically restart the motor after a locked rotor condition. If the locked rotor condition still exists, the above process repeats itself until the condition is removed, or the THMC40 and THMC41 are powered down (see Figure 9).

NOTE:

The locked rotor detection time and auto-retry time are proportional to the PWM frequency, and therefore to the value of C_{OSC}. With a C_{OSC} value of 2200 pF, the PWM frequency is typically 22.7 kHz, locked rotor detection time is typically one second, and auto-retry time is typically eight seconds.

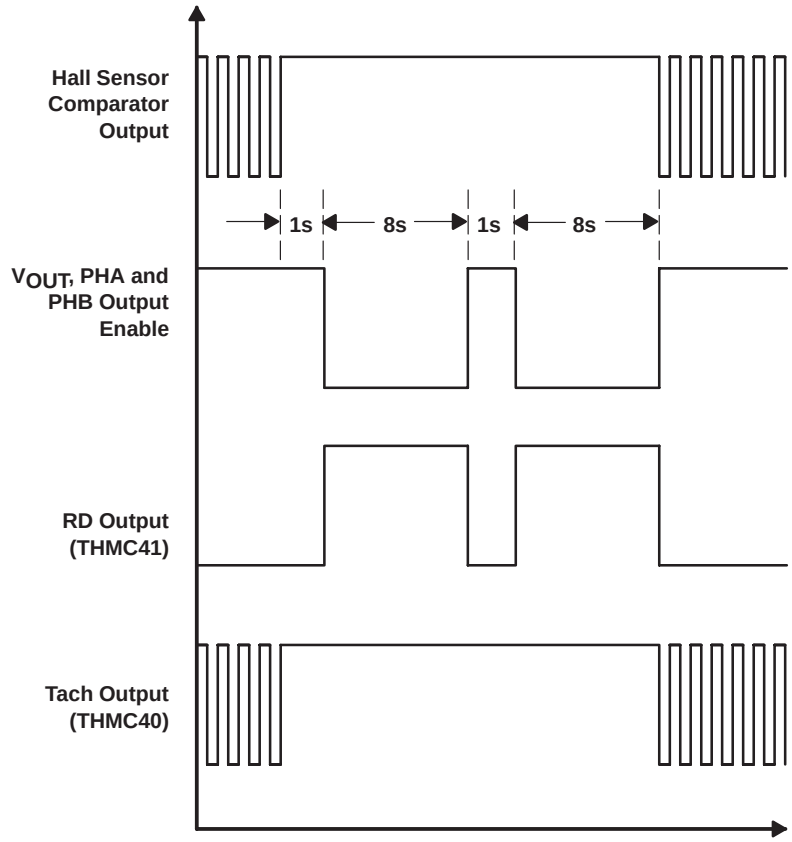


Figure 9. Typical Locked Rotor Protection Timing Waveforms

open-drain tachometer output (TACH)—THMC40 Only

The THMC40 TACH output is an open-drain output activated by the Hall sensor comparator output (see Figure 9). When the Hall sensor comparator output is high, the TACH output floats high. When the Hall sensor amplifier output is low, the TACH output is pulled low. The resulting output signal has two pulses per revolution on a four-pole motor.

The TACH output can be used to monitor and measure actual fan speed. This output can also be used as part of a closed-loop speed control system.

NOTE:

It is recommended that the fan manufacturer not place a pullup resistor for this terminal on the fan circuit board. Leaving the output as open-drain allows the end user to pull up this terminal with an external resistor to the supply voltage of their choice (that is, 3.3 V or 5 V).

open-drain locked rotor detection output—THMC41 only

The THMC41 RD output is an open-drain output pulled low during normal fan operation and allowed to float during a locked rotor condition (see Figure 9). This signal can be used to alert the system of a locked rotor condition.

The RD output can also be used as a *fan present* or *fan OK* signal by using a general-purpose input terminal on a PC Super I/O chip to detect the logic state of this terminal. When this input is high, the signal indicates that the fan has been disconnected or is in a locked rotor condition.

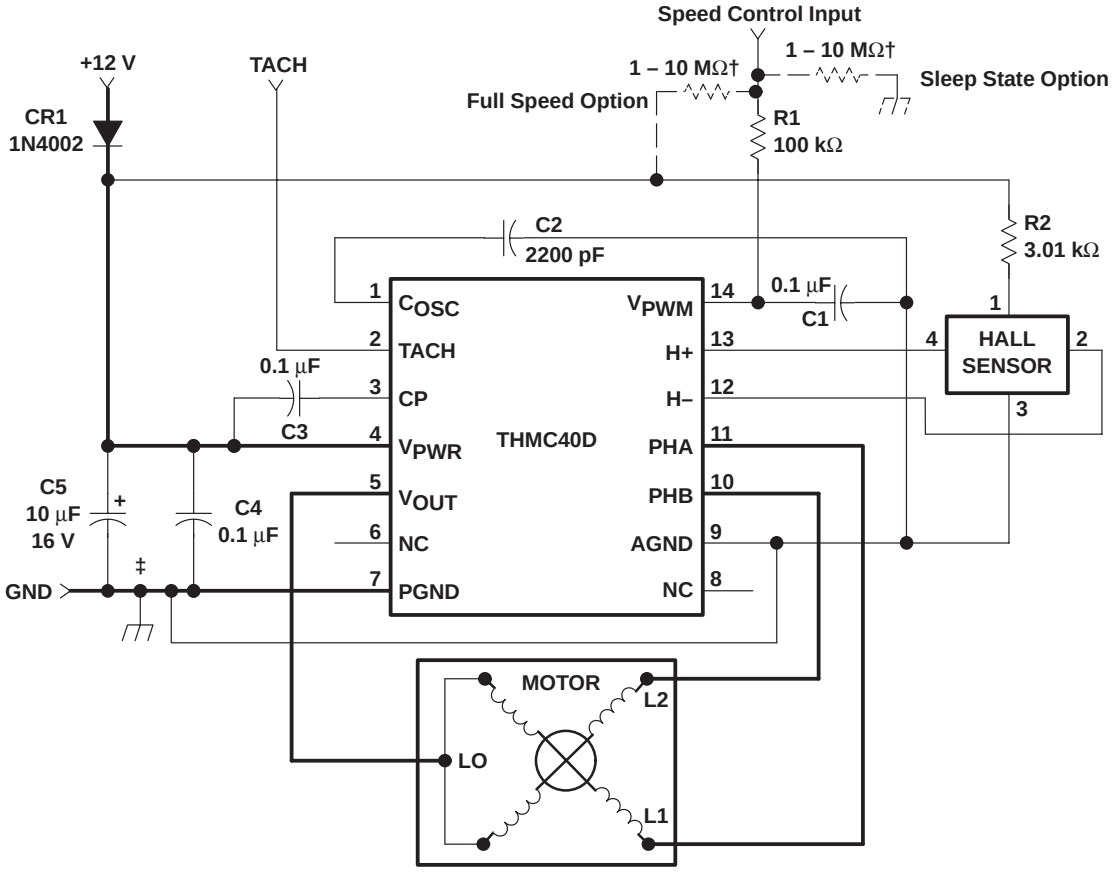
NOTE:

It is recommended that the fan manufacturer not place a pullup resistor for this terminal on the fan circuit board. Leaving the output as open-drain allows the end user to pull up this terminal with an external resistor to the supply voltage of their choice (that is, 3.3V or 5V).

supply voltage input (V_{PWR})

The V_{PWR} terminal serves as the voltage supply input to the THMC40 and THMC41. A 0.1-μF bypass capacitor should be placed as close to this terminal as the layout permits. Additional bulk capacitance of 2.2 μF to 10 μF on this terminal is highly recommended to reduce current spikes on the supply line during motor commutation, thus reducing radiated emissions from the fan. See Application Information for further details.

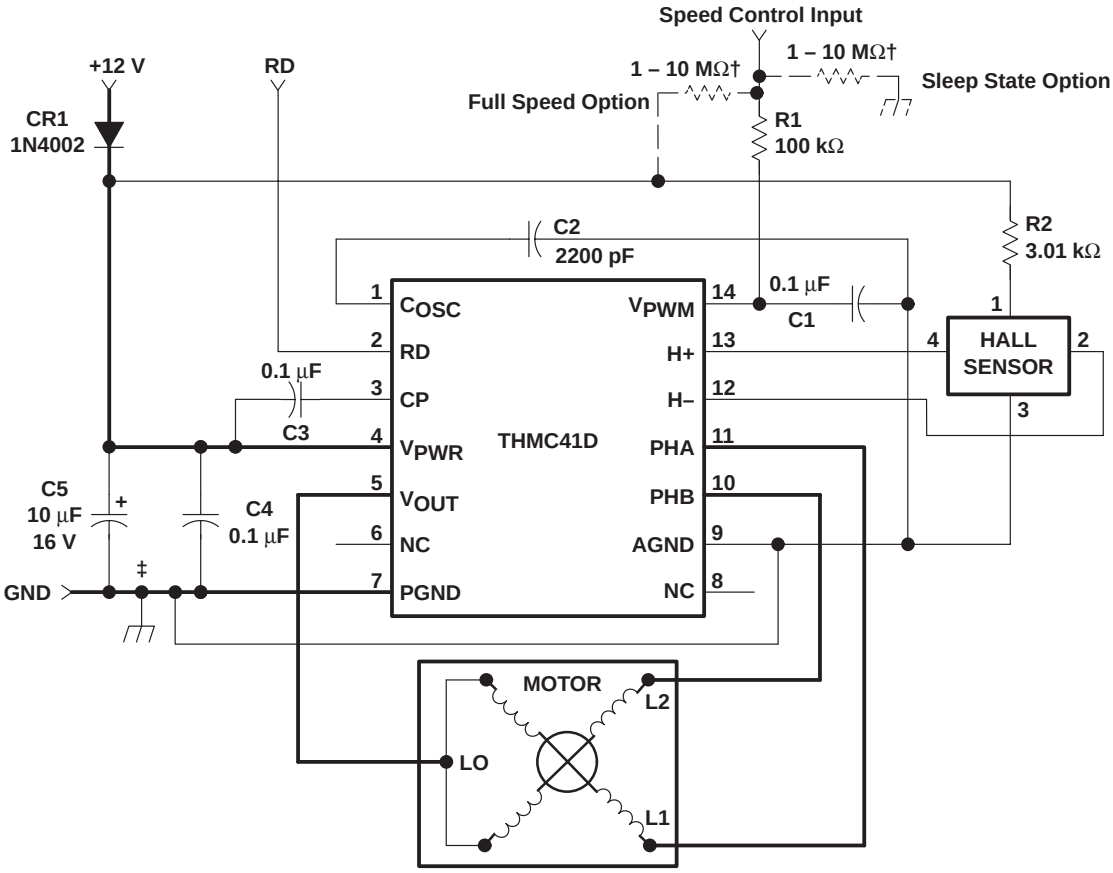
APPLICATION INFORMATION



† Optional resistors control fan operation with open speed control input.
‡ An analog ground trace should be connected close to the ground connection of C4 and C5.
NOTE: Traces in bold handle highest current.

Figure 10. THMC40 Application Schematic

APPLICATION INFORMATION



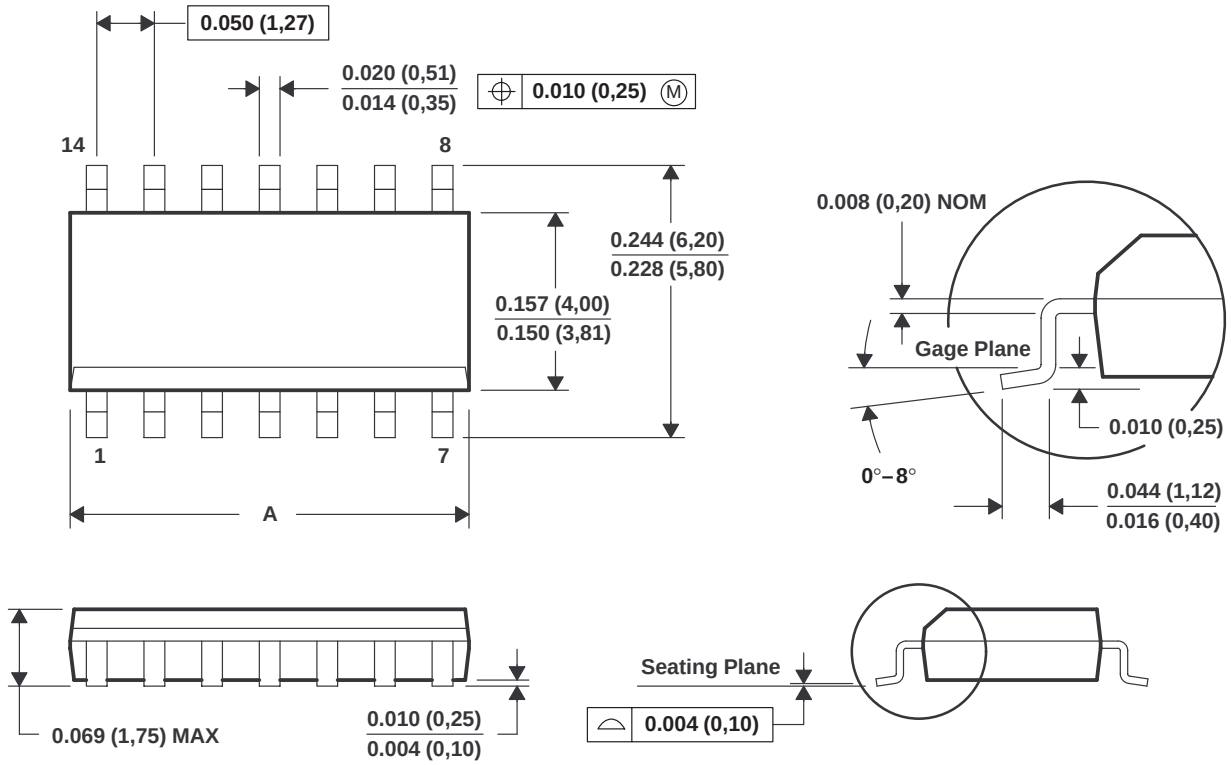
† Optional resistors control fan operation with open speed control input.
‡ An analog ground trace should be connected close to the ground connection of C4 and C5.
NOTE: Traces in bold handle highest current.

Figure 11. THMC41 Application Schematic

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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