

ADVANCED INFORMATION

VOLTAGE DETECTOR

FEATURES

- Very Low Quiescent Current (1 μ A)
- No External Components
- Built In Hysteresis (5% typ.)
- ± 2 % Voltage Detection Accuracy
- Miniature Package (SOT23-5)

APPLICATIONS

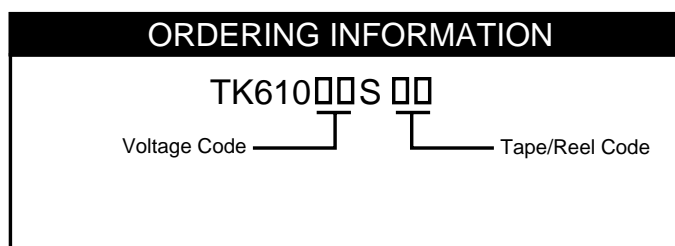
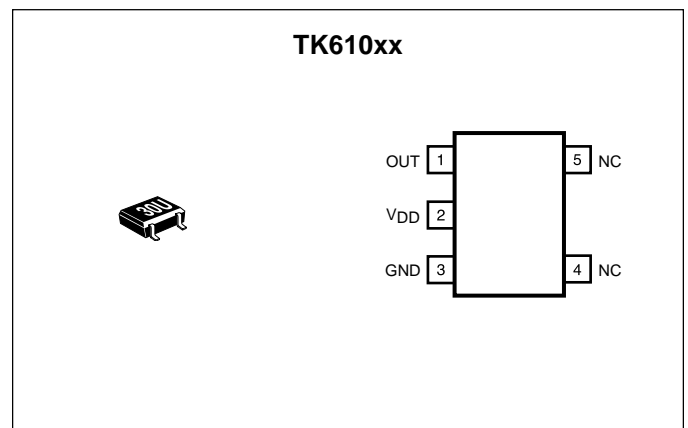
- Battery Powered Systems
- Wireless Telephones
- Pagers
- Personal Communications Equipment
- Personal Digital Assistants

DESCRIPTION

The TK610xx family of voltage detectors is designed to provide accurate monitoring of the battery voltage. These low powered CMOS devices require no external components and are available in 0.1 V steps from 2.0 V to 5.0 V.

When the input voltage reaches the detection voltage, the output goes low. This detection voltage has a ± 2 % accuracy and is set at the factory. When the input voltage goes high, the output will stay low until the voltage reaches the detection voltage plus hysteresis (+3 to +7 %).

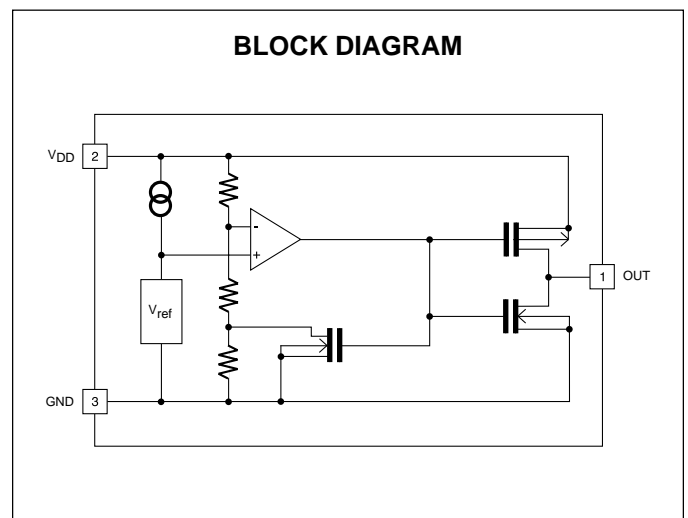
The TK610xx is available in a miniature SOT23-5 surface mount package.



VOLTAGE CODE *	
23 = 2.3 V	36 = 3.6 V
25 = 2.5 V	40 = 4.0 V
27 = 2.7 V	41 = 4.1 V
30 = 3.0 V	42 = 4.2 V
33 = 3.3 V	45 = 4.5 V

TAPE/REEL CODE
TL: Tape Left

* Consult factory for availability of other voltages



TK610xx

ABSOLUTE MAXIMUM RATINGS

All Pins Except GND 11 V
 Power Dissipation (Note 4) 400 mW
 Storage Temperature Range -40 to +125 °C

Operating Temperature Range -30 to +80 °C
 Junction Temperature 150 °C

TK610xx ELECTRICAL CHARACTERISTICS

T_A = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V _{ERR}	Voltage Accuracy	Note 1	-2		+2	%
HYS	Hysteresis	Note 2	3	5	7	%
V _{DDH}	Maximum Operating Voltage		9			V
V _{DDL}	Lowest Operating Voltage				0.8	V
$\frac{\Delta V_{DET}}{V_{DET} * \Delta T}$	Detection Voltage Temperature Coefficient	-30 °C ≤ top ≤ 80 °C		±100		ppm/°C
t _{DR}	Rise Propagation Delay Time	Note 3		100		µsec
I _{SSL}	Supply Current (L)	V _{DD} = 1.0 V			1.0	µA
I _{SSM}	Supply Current (M)	V _{DD} = 5.0 V, 2.0 V ≤ Setting Voltage ≤ 5.0 V		1.0	2.0	µA
I _{SSH}	Supply Current (H)	V _{DD} = 7.0 V, 4.2 V ≤ Setting Voltage ≤ 5.0 V		1.5	3.0	µA
I _{ON1}	Output Current (N1) (Note 5)	V _{DS} = 0.05 V, V _{DD} = 0.8 V	0.01	0.05		mA
I _{ON2}	Output Current (N2) (Note 5)	V _{DS} = 0.5 V, V _{DD} = 1.5 V	2.0	4.0		mA
I _{OP1}	Output Current (P1) (Note 6)	V _{DS} = 2.1 V, V _{DD} = 4.5 V, 2.0 V ≤ Setting Voltage ≤ 4.1 V	2.0	4.0		mA
I _{OP1}	Output Current (P1) (Note 6)	V _{DS} = 2.1 V, V _{DD} = 7.0 V, 4.2 V ≤ Setting Voltage ≤ 5.0 V	6.0	8.0		mA

Note 1: V_{ERR} = 100 * (V_{DET} - Setting Voltage) / Setting Voltage expressed in %

Note 2: HYS = 100 * (V_{HYS} - V_{DET}) / V_{DET} expressed in %

Note 3: The applied voltage is a pulse of V_{LOW} = 0.8 V, V_{HIGH} = V_{DET} + 2 V

Note 4: Power dissipation is 400 mW when mounted as recommended. Derate at 3.2 mW/°C for operation above 25 °C.
 Power dissipation is 200 mW in Free Air. Derate at 1.6 mW/°C for operation above 25 °C.

Note 5: Output sink current.

Note 6: Output source current.

TEST CIRCUIT

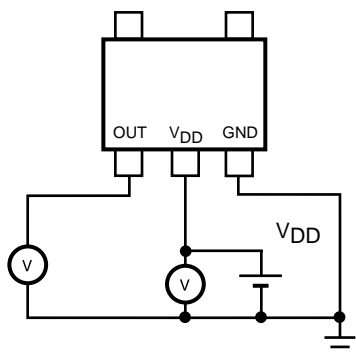


FIGURE 1: TEST CIRCUIT FOR V_{DET} , V_{HYS} , V_{DDH} ,
 V_{DDL} , t_{DR}

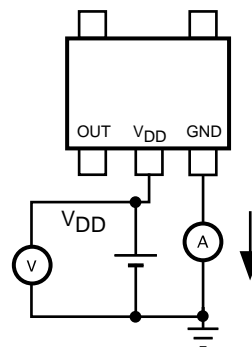


FIGURE 3: TEST CIRCUIT FOR I_{SS}

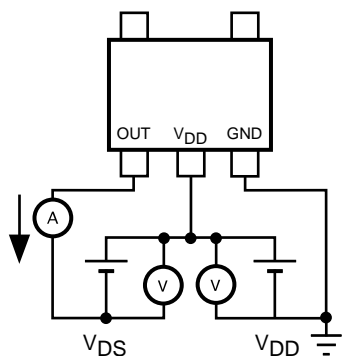


FIGURE 2: TEST CIRCUIT FOR I_{OP}

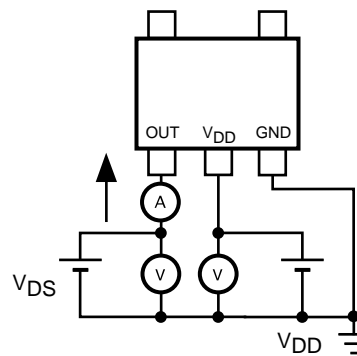
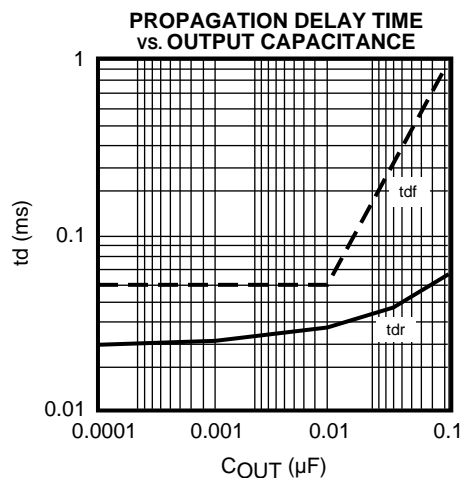
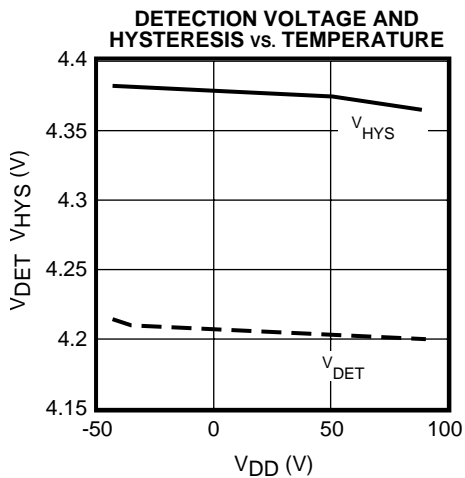
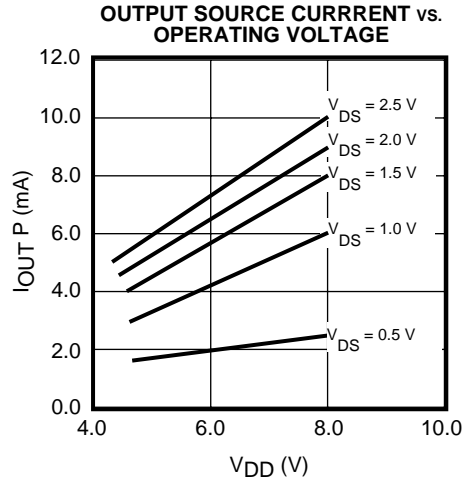
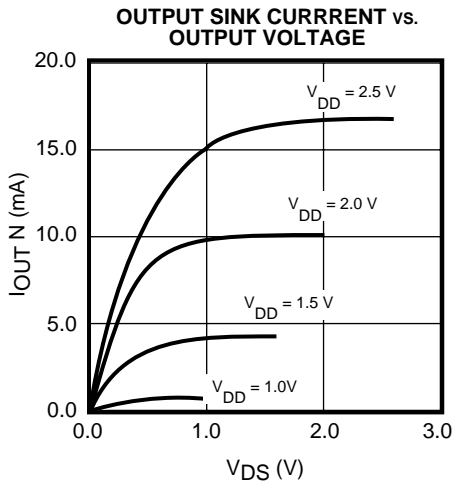
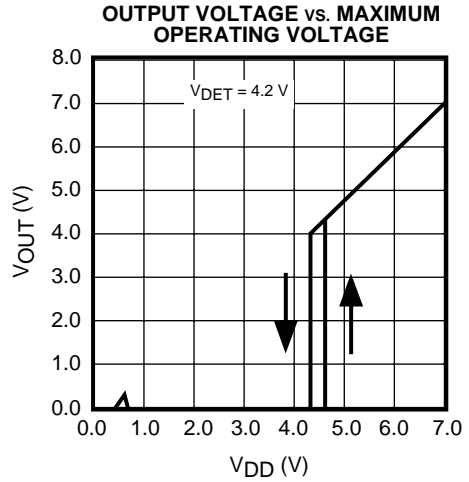
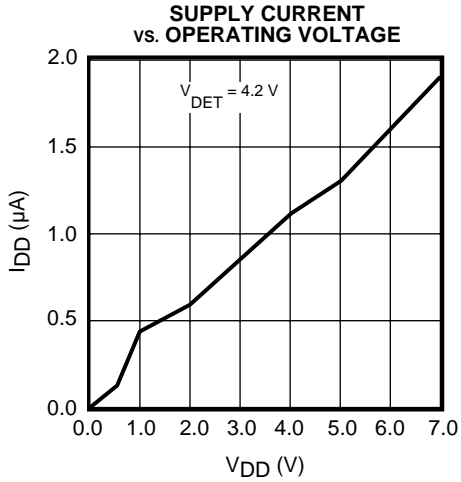


FIGURE 4: TEST CIRCUIT FOR I_{ON}

TYPICAL PERFORMANCE CHARACTERISTICS



DEFINITION AND EXPLANATION OF TECHNICAL TERMS

DETECTION VOLTAGE (V_{DET})

When V_{DD} goes below the detection voltage, the output goes low.

HYSTERESIS VOLTAGE (V_{HYS})

When V_{DD} goes above the sum of the detection voltage and the hysteresis voltage, the output goes high.

SUPPLY CURRENT (I_{SSL})

Supply current ($V_{DD} = 1\text{ V}$)

SUPPLY CURRENT (I_{SSM})

Supply current ($V_{DD} = 5\text{ V}$) $2.0\text{ V} \leq \text{setting voltage} \leq 4.1\text{ V}$

SUPPLY CURRENT (I_{SSH})

Supply current ($V_{DD} = 7\text{ V}$) $4.2 \leq \text{setting voltage} \leq 5.0\text{ V}$

OUTPUT CURRENT (I_{ON1})

Output sink current of output N channel FET
 $V_{DD} = 0.8\text{ V}$, $V_{DS} = 0.5\text{ V}$

OUTPUT CURRENT (I_{ON2})

Output sink current of output N channel FET
 $V_{DD} = 1.5\text{ V}$, $V_{DS} = 0.5\text{ V}$

OUTPUT CURRENT (I_{OP1})

Output source current of output P channel FET
 $V_{DD} = 4.5\text{ V}$, $V_{DS} = 2.1\text{ V}$, $2.0\text{ V} \leq \text{setting voltage} \leq 4.1\text{ V}$

VOLTAGE ACCURACY (V_{ERR})

Error ratio of set voltage
 $V_{ERR} = 100 * (V_{DET} - \text{Setting Voltage}) / \text{Setting Voltage}$
expressed in %

HYSTERESIS (HYS)

Ratio of hysteresis voltage to detection voltage
 $HYS = 100 * (V_{HYS} - V_{DET}) / V_{DET}$ expressed in %

MAXIMUM OPERATING VOLTAGE (V_{DDH})

The maximum operating voltage.

LOWEST OPERATING VOLTAGE (V_{DDL})

Voltage when V_{DD} is reduced and output goes up from 0 V to 100 mV.

DETECTION VOLTAGE TEMPERATURE COEFFICIENT ($\Delta V_{DET} / V_{DET} * \Delta T$)

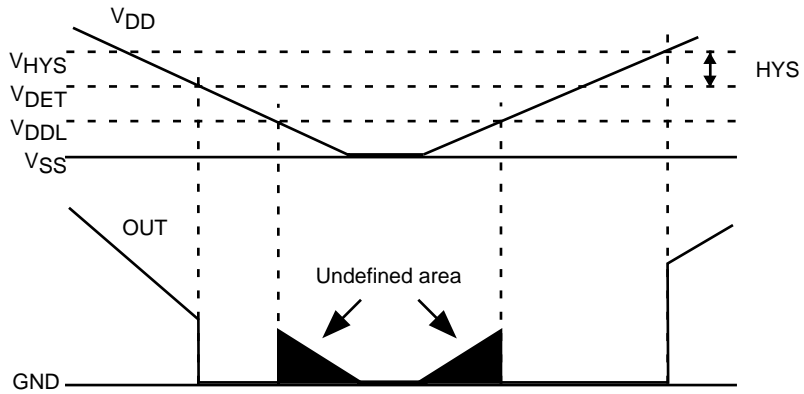
Temperature coefficient of detection voltage.

$$\frac{\Delta V_{DET}}{V_{DET} * \Delta T} = \frac{1000000 * (V_{DET}(T) - V_{DET}(25\text{ }^\circ\text{C}))}{V_{DET}(25\text{ }^\circ\text{C}) * (T - 25\text{ }^\circ\text{C})}$$

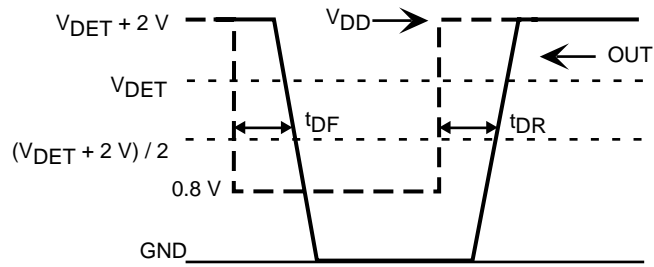
RISE PROPAGATION DELAY TIME (t_{DR})

The delay time for the output to reach $(V_{DET} + 2.0\text{ V}) / 2$ when V_{DD} goes from $V_{LOW} = 0.8\text{ V}$ to $V_{HIGH} = V_{DET} + 2.0\text{ V}$

OUTPUT CHARACTERISTICS



OUTPUT vs. SUPPLY VOLTAGE

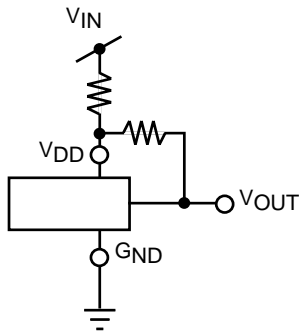


OUTPUT PROPAGATION DELAY

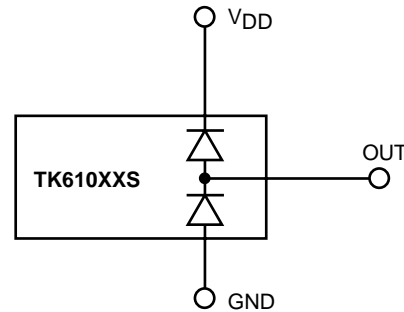
APPLICATION INFORMATION

CHANGING DETECTION VOLTAGE USING EXTERNAL RESISTORS

It is not recommended to set the detection voltage using external resistors (See figure below) as oscillations may occur.

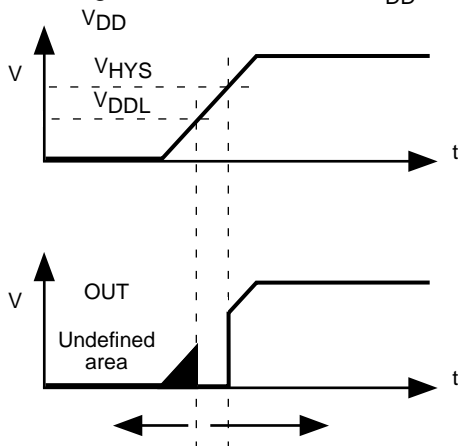


Note: For the TK610xx, there is an internal diode between GND and Output and another diode between Output and V_{DD} . Current will flow between these terminals if the diodes are forward biased. See the figure below for diode polarity.

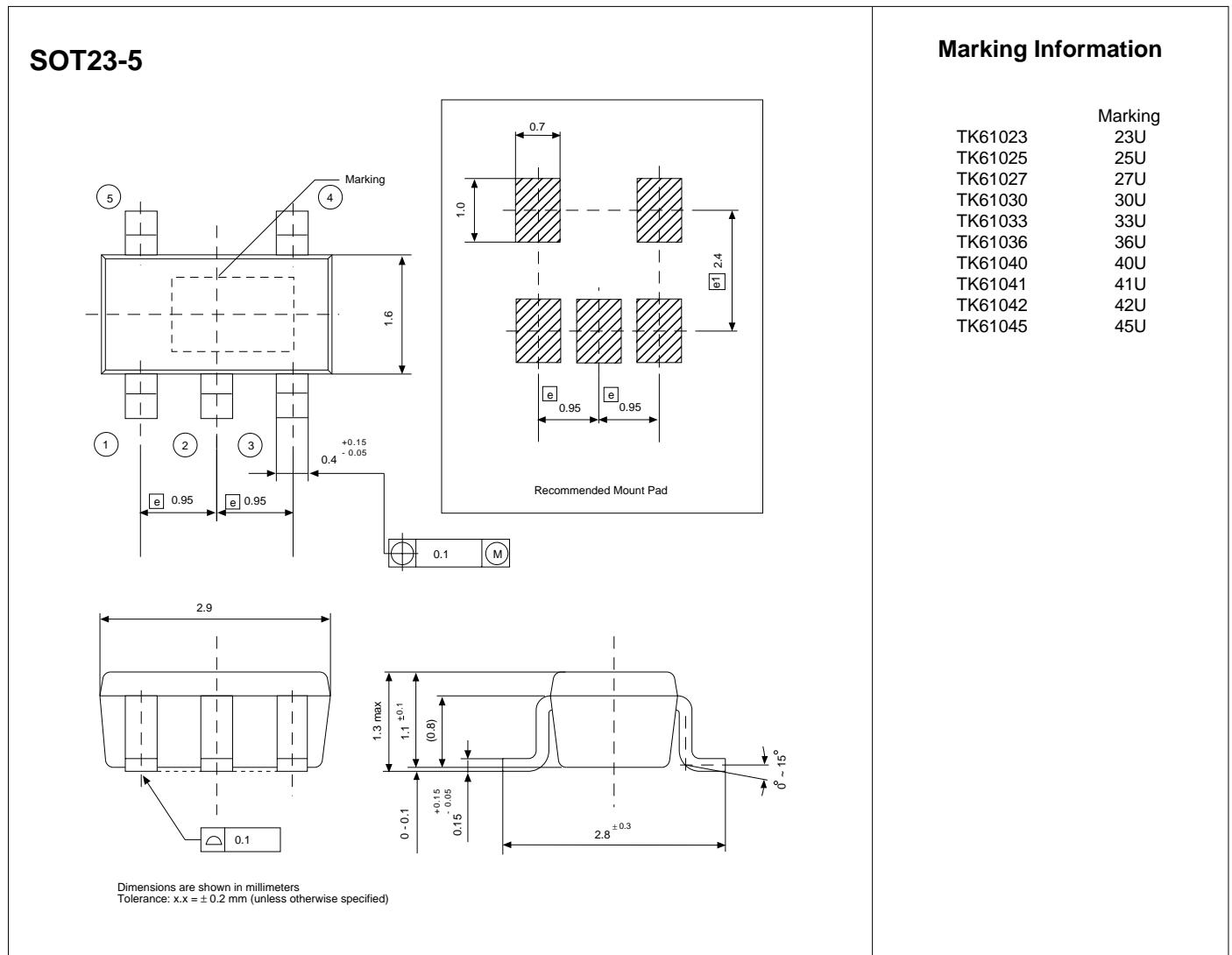


OUTPUT H CHARACTERISTICS FOR $V_{DD} < V_{DD1}$

The output voltage is not defined when $V_{DD} < V_{DDL}$.



PACKAGE OUTLINE



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