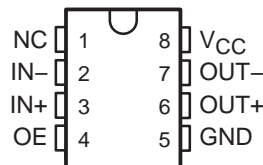


- Operates From a Single 5-V Supply
- 0-V to 5.5-V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

D, P, PS, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

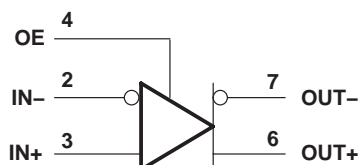
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| 0°C to 70°C | PDIP (P) | Tube of 50 | TL712CP | TL712CP |
| | SOIC (D) | Tube of 75 | TL712CD | TL712C |
| | | Reel of 2500 | TL712CDR | |
| | SOP (PS) | Reel of 2000 | TL712CPSR | T712 |
| | TSSOP (PW) | Tube of 150 | TL712CPW | T712 |
| | | Reel of 2000 | TL712CPWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

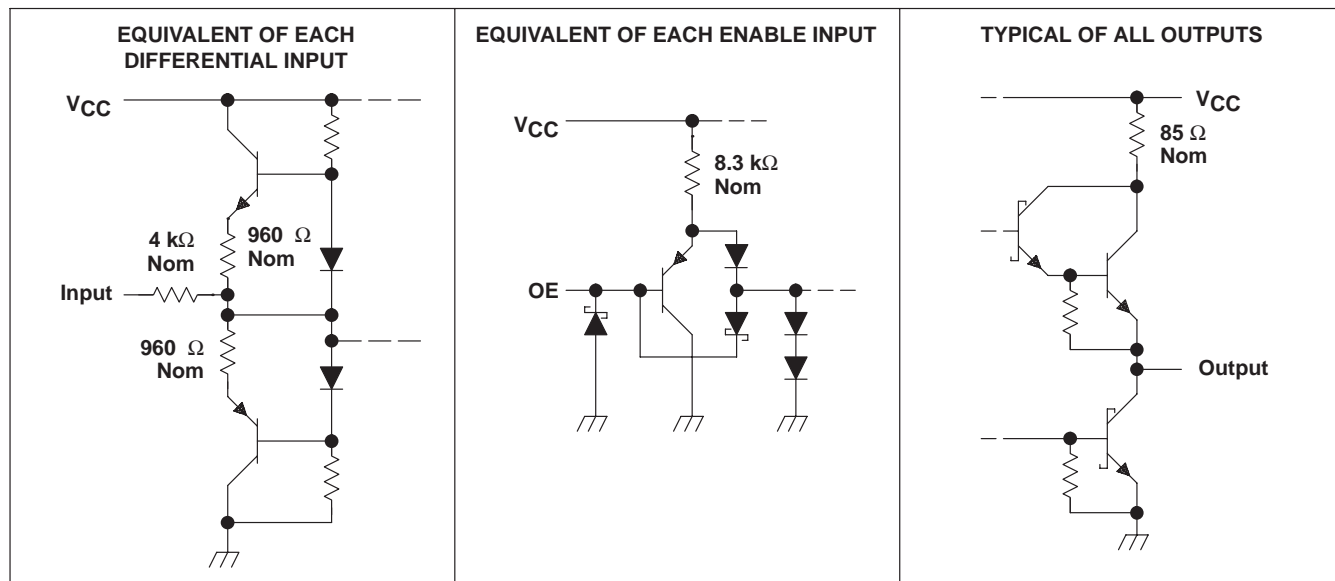
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TL712 DIFFERENTIAL COMPARATOR

SLCS002D – JUNE 1983 – REVISED AUGUST 2003

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 25 V |
| Input voltage, V_I , any differential input | ± 25 V |
| Output enable voltage | 7 V |
| Low-level output current, I_{OL} | 50 mA |
| Package thermal impedance, θ_{JA} (see Notes 3 and 4): | |
| D package | 97°C/W |
| P package | 85°C/W |
| PS package | 95°C/W |
| PW package | 149°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground.
 2. Differential voltage values are at $IN+$ with respect to $IN-$.
 3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| V _{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V _{IC} Common-mode input voltage | 0 | | 5.5 | V |
| I _{OH} High-level output current | | | -1 | mA |
| I _{OL} Low-level output current | | | 16 | mA |
| T _A Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics at V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-------------------|-----|------|------|
| V _T Threshold voltage (V _{T+} and V _{T-}) | V _{ICR} = 0 to 5 V | -100 [†] | | 100 | mV |
| V _{hys} Hysteresis (V _{T+} - V _{T-}) | | | 5 | | mV |
| V _{OH} High-level output voltage | V _{ID} = 100 mV, I _{OH} = -1 mA | 2.7 | 3.5 | | V |
| V _{OL} Low-level output voltage | V _{ID} = -100 mV, I _{OL} = 16 mA | | 0.4 | 0.5 | V |
| I _{OZ} Off-state output current | V _O = 2.4 V | | | -20 | μA |
| I _I Enable current | V _I = 5.5 V | | | 100 | μA |
| I _{IH} High-level enable current | V _{IH} = 2.7 V | | | 20 | μA |
| I _{IL} Low-level enable current | V _{IL} = 0.4 V | | | -360 | μA |
| r _i Differential input resistance | | 4 | | | kΩ |
| r _o Output resistance | | | | 100 | Ω |
| I _{OS} Short-circuit output current | | -15 | | -85 | mA |
| I _{CC} Supply current | V _{ID} = 0, No load | | 17 | 20 | mA |

[†] The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

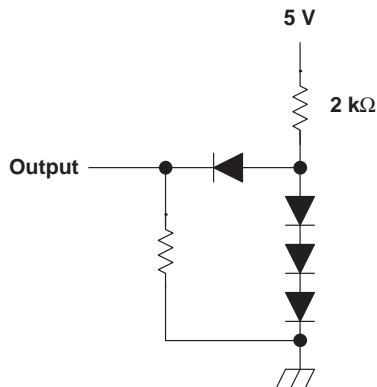
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------------------------|-----|------|
| t _{PLH} Propagation delay time, low-to-high-level output | TTL load, See Note 5 and Figure 1 | 25 | ns |
| t _{PHL} Propagation delay time, high-to-low-level output | | 25 | ns |

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.

TL712 DIFFERENTIAL COMPARATOR

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PARAMETER MEASUREMENT INFORMATION



NOTE A: All diodes are 1N4148 or equivalent.

Figure 1. TTL Output Load Circuit

TYPICAL CHARACTERISTICS

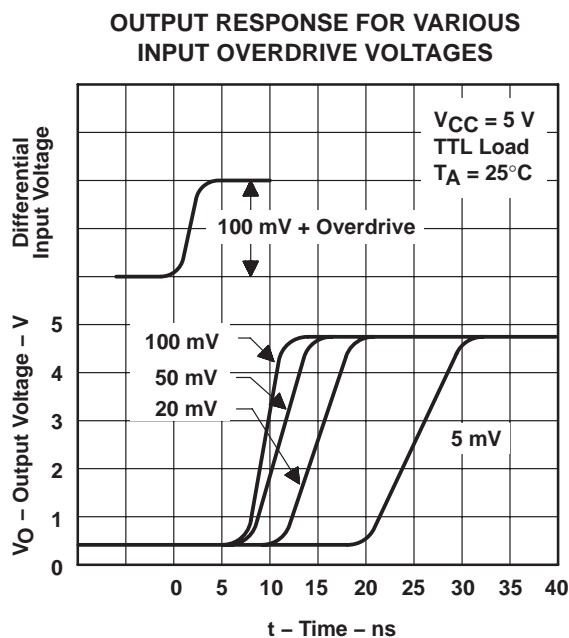


Figure 2

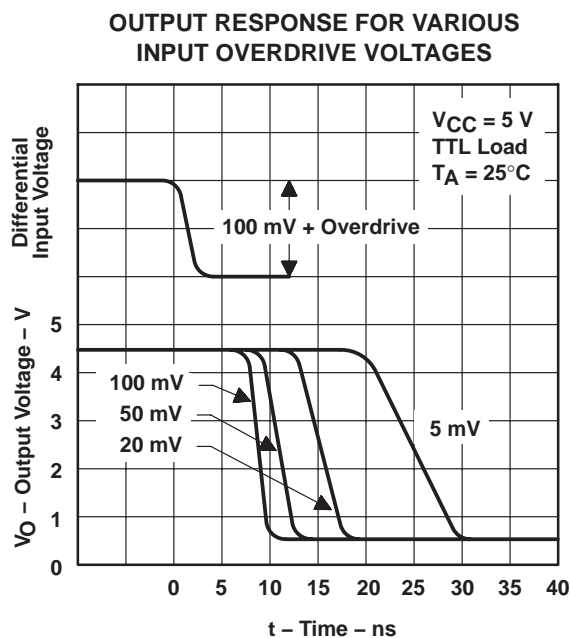


Figure 3

TYPICAL CHARACTERISTICS

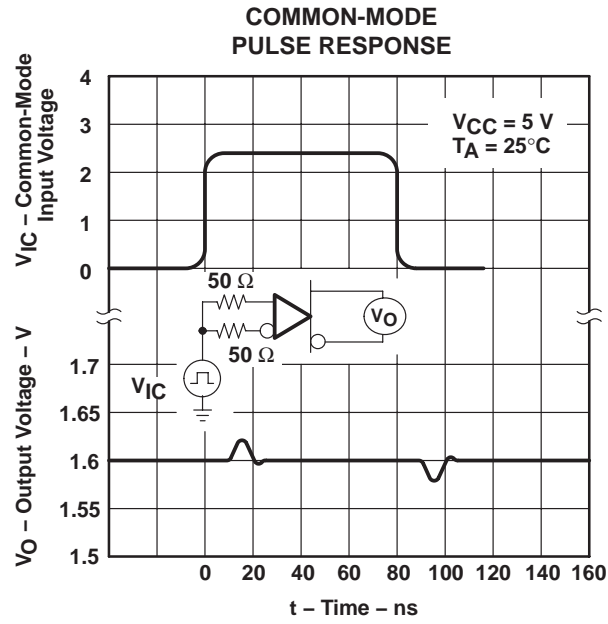


Figure 4

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TL712CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL712CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TL712CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CPSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CPWE4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL712CPWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



4040082/D 05/98

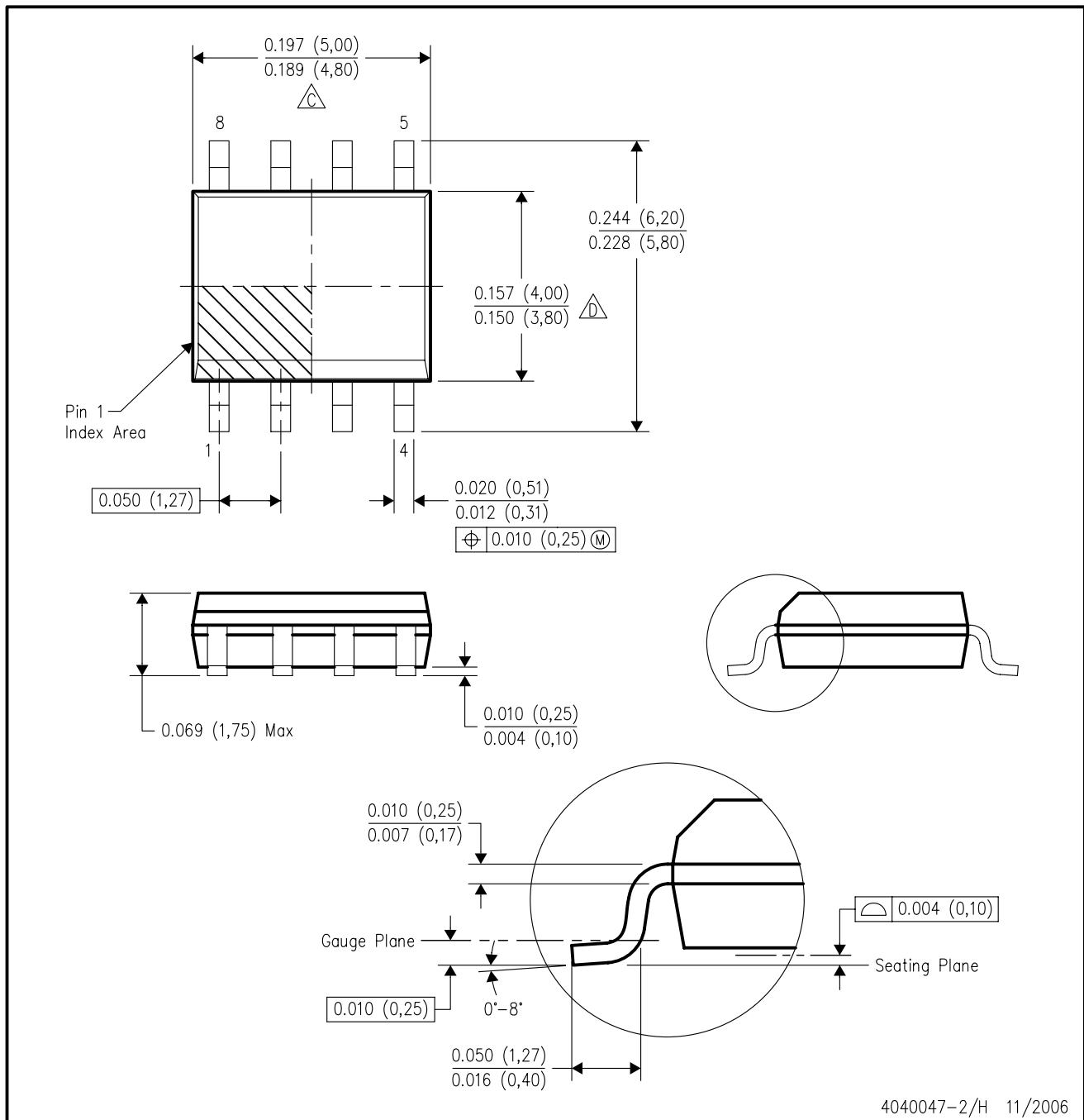
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 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
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 D. Falls within JEDEC MO-153

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