CMOS 4-BIT MICROCONTROLLER

TMP47C241N
TMP47C241M

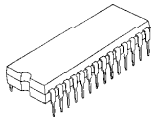
The 47C241 are high speed and high performance 4-bit single chip micro computers, integrating 8-bit A/D converter, watchdog timer and serial Interface based on the TLCS-47 series.

PART No.	ROM	RAM	RACKAGE	OTP
TMP47C241N	2048 × 8-bit	128 × 4-bit	SDIP28-P-400-1.78	TMP47P241VN
TMP47C241M			SOP28-P-450-1.27	TMP47P241VM

FEATURES

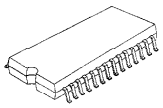
◆4-bit single chip microcomputer
◆Instruction execution time : 1.3 μs (at 6 MHz)
◆Low voltage operation : 2.7 V (at 4.2 MHz)
◆90 basic instructions
  •Table look-up instructions
◆Subroutine nesting : 15 levels max.
◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
◆I/O port (21 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 5 pins
  - I/O 4 ports 11 pins
◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
◆Interval timer
◆Watchdog Timer
◆Serial Interface with 4-bit buffer
  External / internal clock, and leading / trailing edge shift mode
◆8-bit successive approximate type A/D converter
  (With sample and hold)
  - 4 analog inputs
  - Converting time : 48 μs (4 MHz)
◆High current outputs
  LED direct drive capability : typ. 20 mA × 5 bits (Ports P1, P2)
  typ. 7 mA × 3 bits (Port R9)
◆Hold function
  Battery / Capacitor back-up
◆Real Time Emulator : BM47214A + BM1152 (SDIP)

SDIP28-P-400-1.78



TMP47C241N
TMP47P241VN

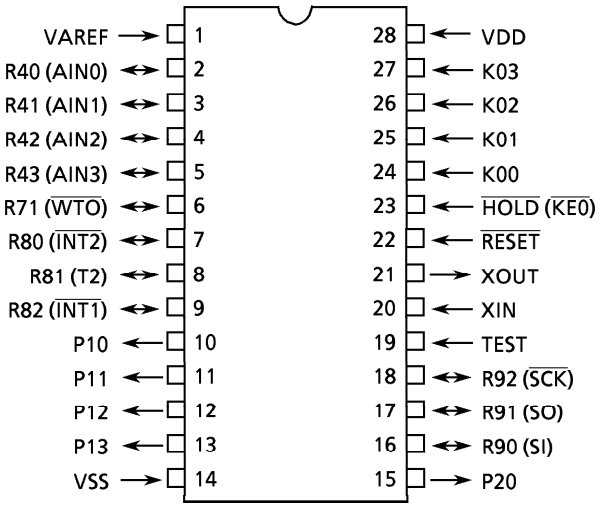
SOP28-P-450-1.27



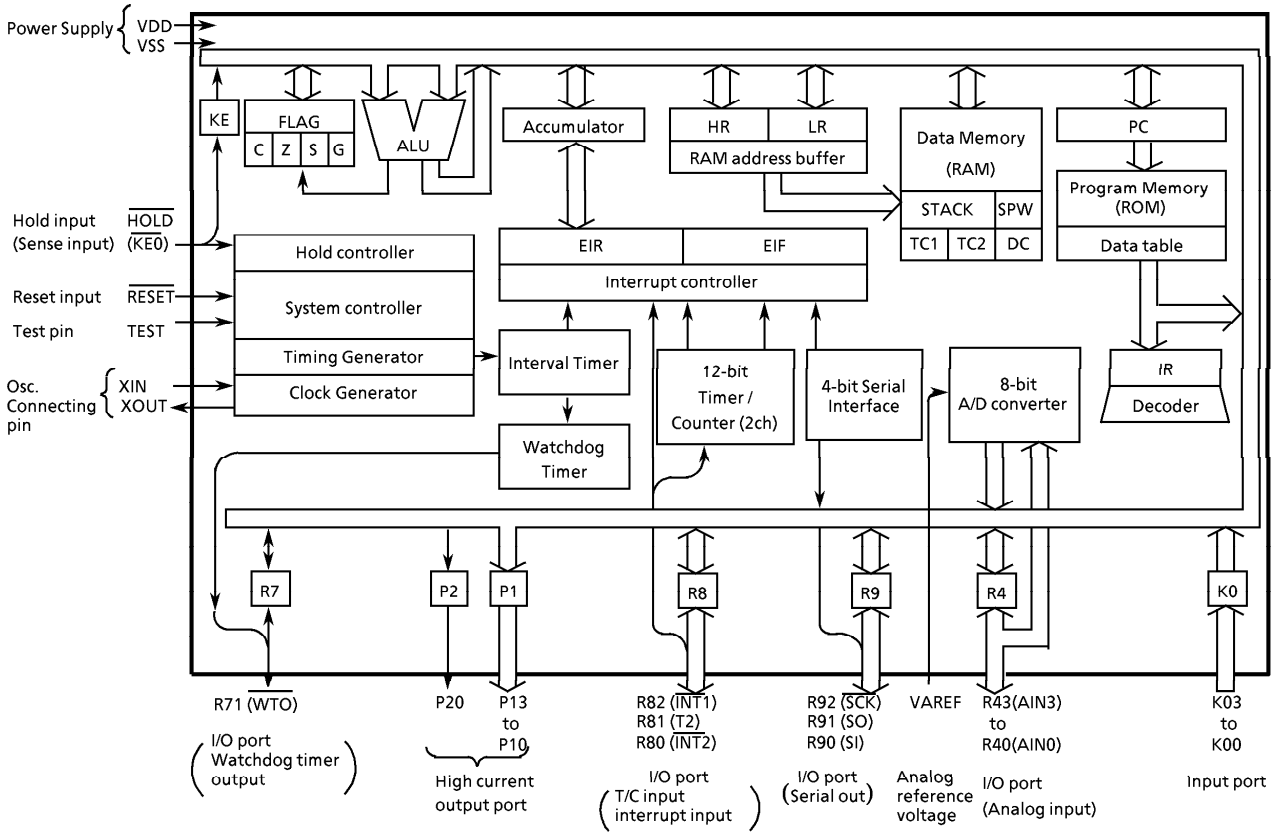
TMP47C241M
TMP47P241VM

PIN ASSIGNMENT (TOP VIEW)

SDIP28-P-400-1.78 / SOP28-P-450-1.27



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch.	
P20		1-bit output port with latch.	
R43 (AIN3) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	A / D converter analog input
R71 ($\overline{WTO}$)	I/O (Output)	1-bit I/O port with latch. When using as input port or watchdog timer output, the latch must be set to "1".	Watchdog timer output
R82 ($\overline{INT1}$)	I/O (Input)	3-bit I/O port with latch. When using as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request / release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	A/D converter analog reference voltage (GND)
VAREF		A/D converter analog reference voltage	

OPERATIONAL DESCRIPTION

Conserning the 47C241, the hardware configuration and operation are described.
As the description is porvided with priority on those parts differing from the 47C200B, the technical data sheets for the 47C200B shall also be referred to.

1. SYSTEM CONFIGURATION

(1) INTERNAL CPU FUNCTION

These as the same as the 47C200B.

(2) PERIPHERAL HARDWARE FUNCTION

① I/O Ports	④ A/D converter
② Interval Timer	⑤ Watchdog Timer
③ Timer/Counters	⑥ Serial Interface

This section describes ports of 1 and 3 to 6 which are added and changed from the 47C200B.

2. PERIPHERAL HARDWARE FUNCTION

2.1 Ports

The 47C241 has 8 I/O ports (21 pins) each as follows :

① K0	;	4-bit input
② P1	;	4-bit output
③ P2	;	1-bit output
④ R4	;	4-bitinput / output (shared by the A/D converter analog inputs)
⑤ R7	;	1-bit input / output (shared by the watchdog timer output)
⑥ R8	;	3-bit input / output shared by external interrupt request input and timer / counter input)
⑦ R9	;	3-bit input / output (shared by serial port)
⑧ KE	;	1-bit sense input (shared by hold request / release signal input)

This section describes ports of ③ to ⑥ which are changed from the 47C200B (The 47C241 dose not have R5, R6 ports).
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.
The 5-bit to 8-bit data conversion instruction [OUTB @HL] is invalid.

(1) Port P2 (P20)

Port P2 is 1-bit output port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. P21, P22 and P23pins do not exist actually. But these pins have the latches.

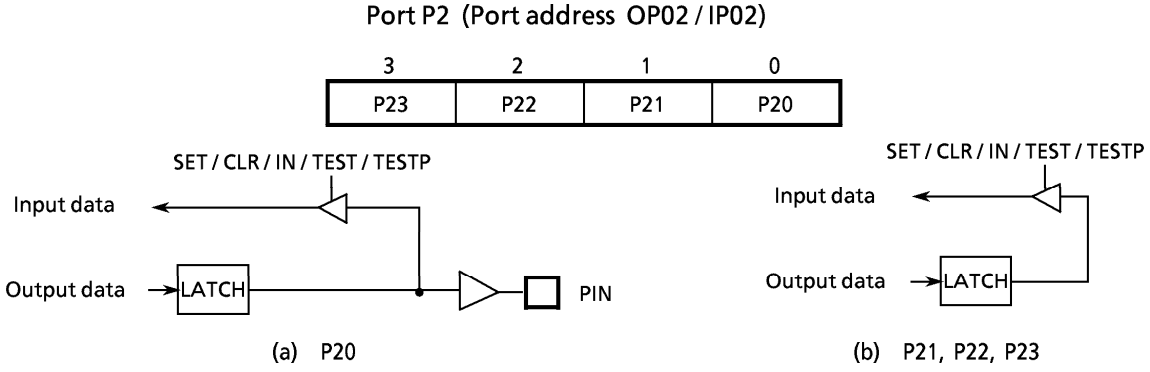


Figure 2-1. Port P2

(2) Ports R4 (R43 to R40)

Ports R4 is 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

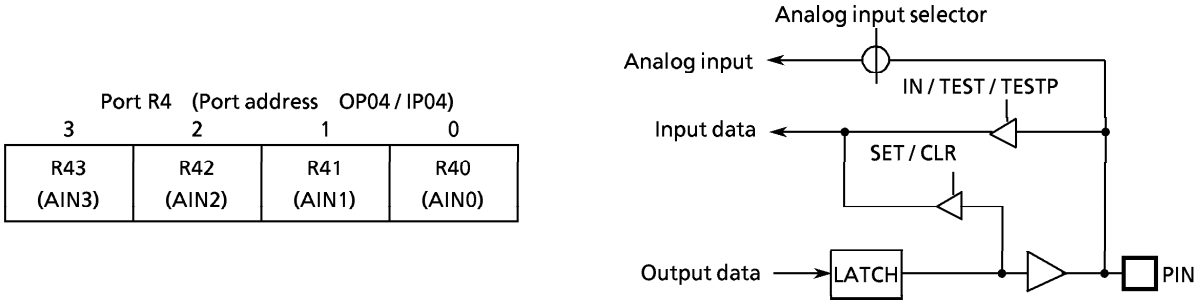
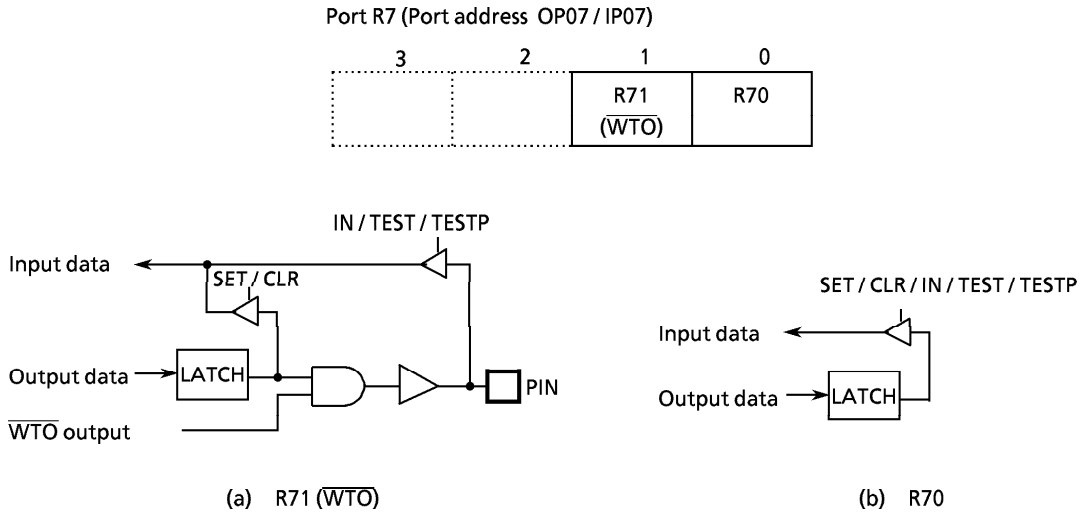


Figure 2-2. Port R4

(3) Port R7 (R71)

1-bit I/O pin with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70, R72, R73 pins do not exist actually but R70 has the latch. In R72 and R73, "1" is read when an input instruction is executed.

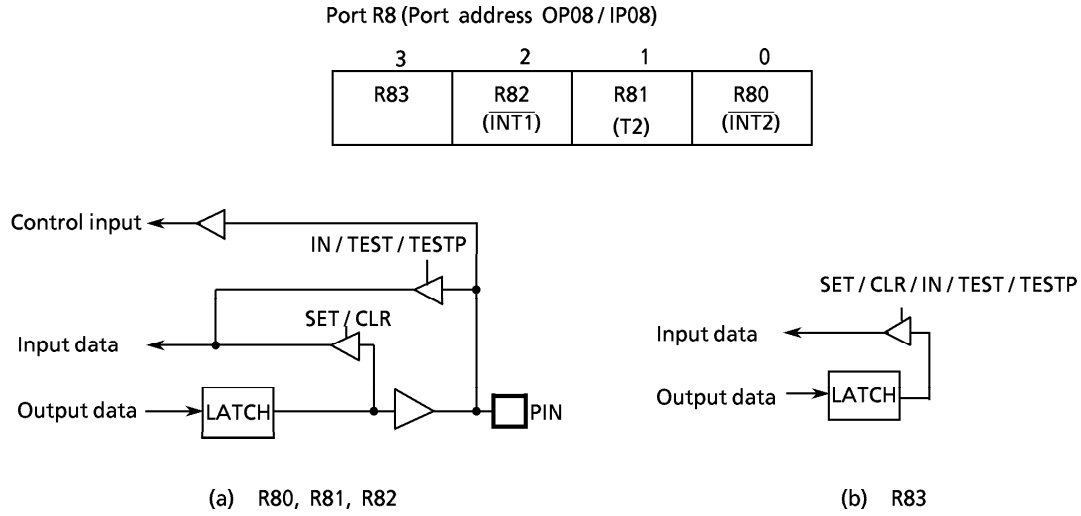


(a) R71 ($\overline{WTO}$) (b) R70

Figure 2-3. Port R7

(4) Port R8 (R82 to R80)

3-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. R83 pins does not exist actually but R83 has the latch. There is no timer / counter 1 external input pin (T1) .



(a) R80, R81, R82 (b) R83

Figure 2-4. Port R8

2.2 Timer / Counter (TC1, TC2)

The 47C241 does not have timer / counter 1 external input. Therefore, timer / counter 1 can be used as internal timer mode only. Other function are equivalent to the 47C200B.

Timer / counter 1 control
(Port address : OP1C) (Initial value : 0000)

3	2	1	0
TCMS1			IPR1

TCMS1	Mode selection

00 : Stop
01 : Reserved
10 : Timer mode
11 : Reserved

IPR1	Internal pulse rate selection

fc = 4.19 MHz

00 :	$fc/2^{10}$ [Hz]	4096 [Hz]
01 :	$fc/2^{14}$	256
10 :	$fc/2^{18}$	16
11 :	$fc/2^{22}$	1

(a) TC1

Timer / counter 2 control
(Port address : OP1D) (Initial value : 0000)

3	2	1	0
TCMS2			IPR2

TCMS2	Mode selection

00 : Stop
01 : Event counter mode
10 : Timer mode
11 : Pulse width measurement mode

IPR2	Internal pulse rate selection

fc = 4.19 MHz

00 :	$fc/2^{10}$ [Hz]	4096 [Hz]
01 :	$fc/2^{14}$	256
10 :	$fc/2^{18}$	16
11 :	$fc/2^{22}$	1

(b) TC2

Figure 2-5. Timer / Counter Control Command Registers

Table 2-1. Port Address Assignments and Available I/O Instructions

Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	–	○	○	–
02	P2 output latch	P2 output port	○	○	○	–	○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port (Analog input)	R4 output port	○	○	○	–	○	○	○
05	——	——	–	–	–	–	–	–	–
06	——	——	–	–	–	–	–	–	–
07	R7 input port	R7 output port ($\overline{WTO}$ output)	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	A / D Status input	——	○	–	–	–	–	○	–
0D	A / D converted value	——	○	–	–	–	–	–	–
0E	SIO, Hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operation mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	A / D analog input selector	–	○	–	–	–	–	–
13	Undefined	A / D start register	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer intrrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note *"——" means the reserved state. Unavailable for the user programs.*

2.3 A/D Converter

The 47C241 has a 8-bit successive approximate type A/D converter and is capable of processing 4 analog inputs.

2.3.1 Circuit configuration

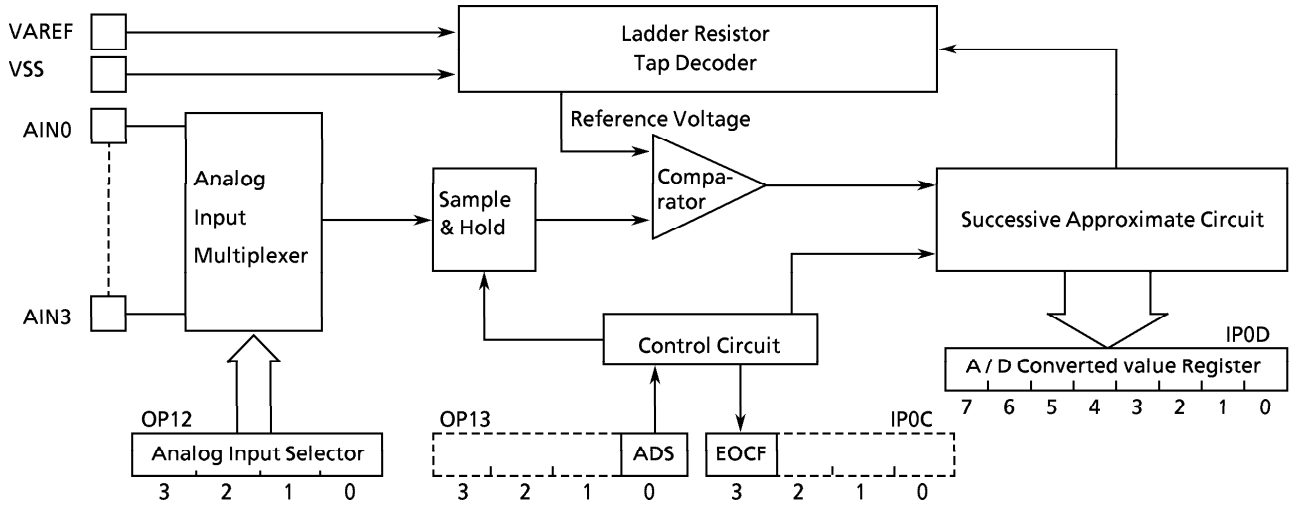


Figure 2-6. Block Diagram of A/D Converter

2.3.2 Control of A/D converter

The operation of A/D converter is controlled by a command register (OP12, OP13, IP0C, IP0D).

(1) Analog input selector (OP12)

Analog inputs (AIN0 through AIN3) are selected by values of this register.

Analog input select command register
(Port address OP12)

3	2	1	0	
SAIN				(Initial value 0000)

SAIN	Analog input selection
0000:	R40(AIN0)
0001:	R41(AIN1)
0010:	R42(AIN2)
0011:	R43(AIN3)
01** :	Analog input is not selected.
1*** :	Analog input is not selected.

*Note. * ; don't care*

Figure 2-7. Analog input selector

(2) Start of A/D conversion (OP13)

A/D conversion is started when ADS is set to "1" . After the conversion is started, ADS is cleared by hardware. If ADS is set to "1" during the A/D conversion, the conversion is started again at the time. Analog input voltage is hold by the sample hold circuit.

A / D conversion start command register
(Port address OP13)

3	2	1	0	
			ADS	(Initial value 0000)

ADS	A / D conversion enable

1: A/D conversion is started (clears after starting)

Figure 2-8. A/D conversion start register

(3) A/D converter and register (IP0C)

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

A / D converter status register
(Port address IP0C)

3	2	1	0
EOCF			

EOCF	End of conversion flag

0: Under A/D conversion or before A/D conversion
1: End of A/D conversion

Figure 2-9. A/D converter status register

(4) A/D converted value register (IP0D)

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L-registers).

A / D converted value register
(Port address IP0D)

3	2	1	0
D3	D2	D1	D0
D7	D6	D5	D4

D7 to D0	Reading of an A/D converted value

When $LR_0 = 0$, lower 4 bits of the converted value is read.
When $LR_0 = 1$, upper 4 bits of the converted value is read.

Figure 2-10. A/D converted value register

2.3.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VSS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VSS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.
Analog supply current (I_{REF}) is typically 500 μA at VAREF = 5 V.
Note that this ladder resistor is connected to VAREF and VSS even in the HOLD mode. Therefore to reduce the power consumption, VAREF should be disconnected from the analog reference voltage supply.

(1) Start of A / D conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.
A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".
Analog input voltage is sampled during the following 2 instruction cycles after setting ADS.

Note. The sample and hold circuit has capacitor (C_A = 12 pF typ.) with resistor (R_A = 5 kΩ typ.). See I/O circuitry table. This capacitor should be charged or discharged within 2 instruction cycles.

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).
Lower 4 bits of the A/D converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

(3) A/D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN3) , starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD      A, #3           ;  Selects analog input (AIN3)
        OUT     A, %OP12
        LD      A, #1           ;  Start of A/D conversion
        OUT     A, %OP13
SLOOP : TEST    %IP0C, 3        ;  To wait until EOCF goes to "1"
        B       SLOOP
        LD      HL, #10H        ;  HL ← 10H
        IN      %IP0D, @HL      ;  RAM [10H] ← Lower 4 bits
        INC     L               ;  Increment of L registers
        IN      %IP0D, @HL      ;  RAM [11H] ← Upper 4 bits
```

2.4 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.4.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

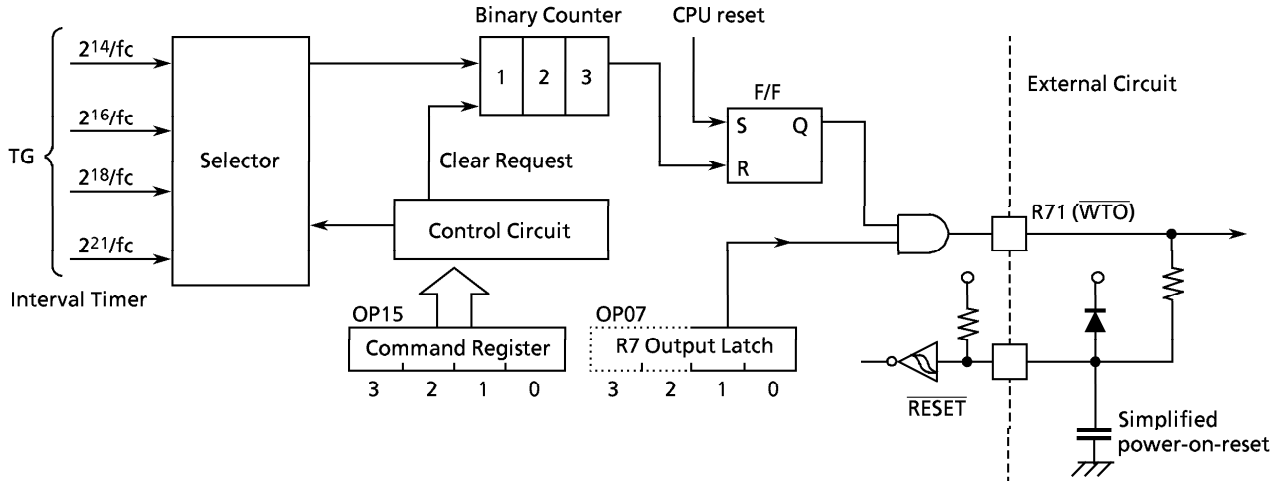


Figure 2-11. Watchdog Timer

2.4.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "0000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

② The watchdog timer should be become enable.

③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0"at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Watchdog Timer control command register (Port address OP15) (Initial value 0000)

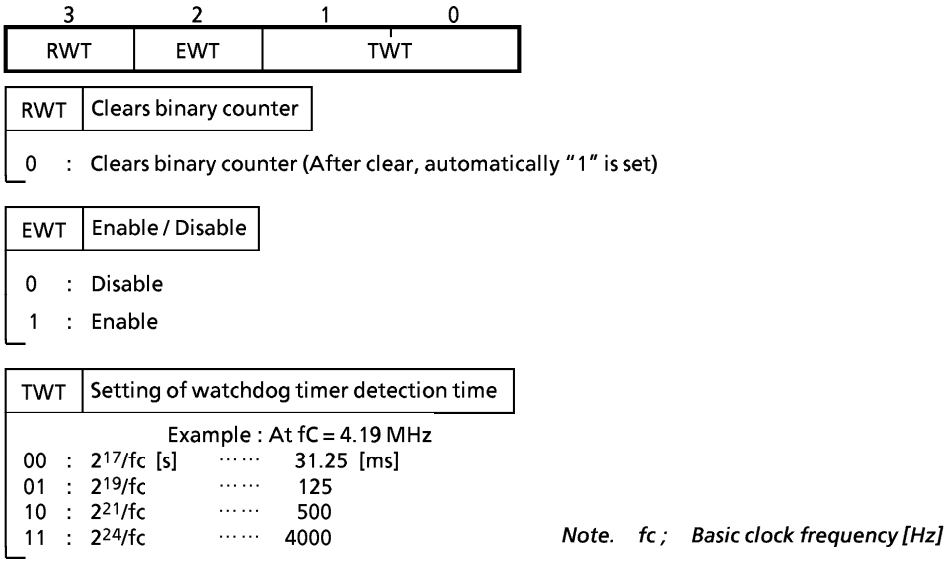


Figure 2-12. Command Register

Example : To set the watchdog detection time (2^{21}/fc [s]). And to enable the watchdog timer.

```
        LD      A, #0010B       ; OP15 ← 0010B
                                  (Sets WDT detection time. Clears binary counter)
        OUT     A, %OP15
        LD      A, #0110B       ; OP15 ← 0110B (Enables WDT)
        OUT     A, %OP15
        :
        :                                          Within WDT
        :                                          detection time
        LD      A, #0110B       ; OP15 ← 0110B (Clears binary counter)
        OUT     A, %OP15
        :
        :
```

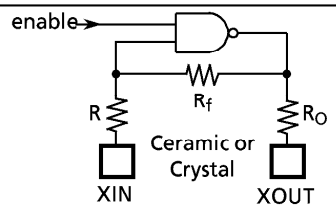
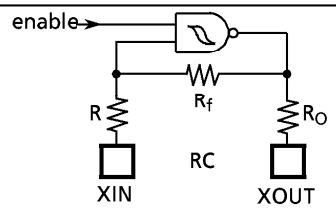
Note. It is not necessary to set RWT to "1". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

INPUT / OUTPUT CIRCUITRY

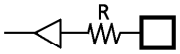
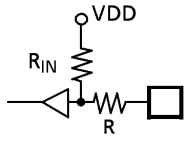
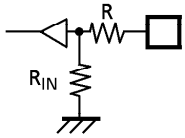
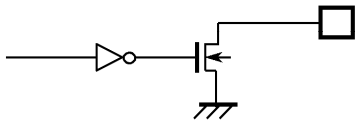
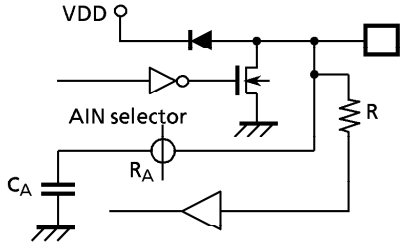
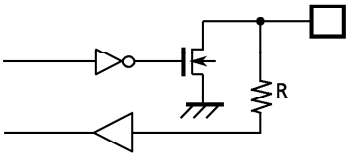
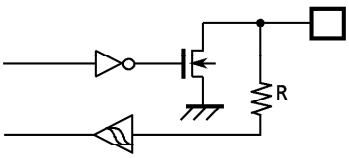
The input / output circuitries of the 47C241 (code SA-SC or SG) are shown as below.

(1) Control pins

The input / output circuitries of the 47C241 control pins except XIN and XOUT pins are similar to that of the 47C200B.

PINS	I/O	CIRCUITRY and CODE		REMARKS
		SA, SB, SC	SG	
XIN XOUT	Input Outut			Resonator connecting pins R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_o = 2 kΩ (typ.)

(2) I/O Ports

P O R T	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		SA, SG	SB	SC	
K0	Input				Pull-up/Pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 20 mA (typ.)
R4	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.) Analog input R_A = 5 kΩ (typ.) C_A = 12 pF (typ.)
R7	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" High current (R9) I_{OL} = 7 mA (typ.) Hysteresis input R = 1 kΩ (typ.)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P1, P2, R7 - R9	– 0.3 to 10	
	V_{OUT3}	Analog inputs	– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Port R9	15	
	I_{OUT3}	Ports R4, R7, R8	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2, R9	120	mA
Power Dissipation [T_{opr} = 70 °C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 6.0 MHz	4.5	6.0	V
			fc = 4.2 MHz	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	In the normal operating area	V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		V_{DD} × 0.75		
	V_{IH3}		In the HOLD mode	V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	In the normal operating area	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		In the HOLD mode		V_{DD} × 0.1	
Clock Frequency	fc		V_{DD} = 4.5 V to 6.0 V	0.4	6.0	MHz
			V_{DD} = 2.7 V to 6.0 V		4.2	
			In the RC oscillation		2.5	

D.C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R, P (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Low Output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
	I_{OL2}	Port R9		—	7	—	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	—	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	—	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	—	0.5	1	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V (V_{DD} = 5.5 V), 2.8 V / 0.2 V (V_{DD} = 3.0 V)

A / D CONVERSION CHARACTERISTICS

(T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{SS}	2.7	—	—	V
Analog Input Voltage	V_{AIN}		V_{SS}	—	V_{AREF}	V
Analog Supply current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

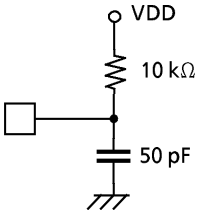
A. C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

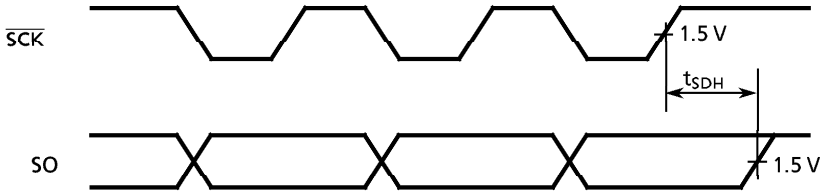
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	V_{DD} = 4.5 to 6.0 V	1.3	—	20	μs
		V_{DD} = 2.7 to 6.0 V	1.9			
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}		—	4	—	μs
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



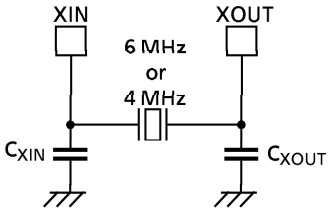
Serial port (completion of transmission)



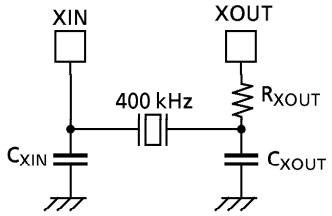
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 70 °C)

(1) 6 MHz
Ceramic Resonator
CSA6. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

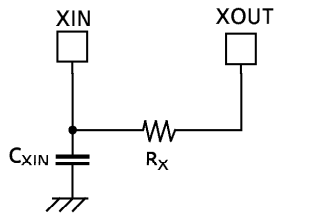


(2) 4 MHz
Ceramic Resonator
CSA4. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
FCR4.0M5 (TDK) $C_{XIN} = C_{XOUT}$ = 33 pF
Crystal Oscillator
204B-6F 4. 0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF



(3) 400 kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

(4) RC Oscillation (V_{SS} = 0 V, V_{DD} = 5.0 V, Topr = 25 °C)
2 MHz (typ.) C_{XIN} = 33 pF, R_X = 10 kΩ
400 kHz (typ.) C_{XIN} = 100 pF, R_X = 26 kΩ



TYPICAL CHARACTERISTICS