#### CMOS 8-Bit Microcontroller

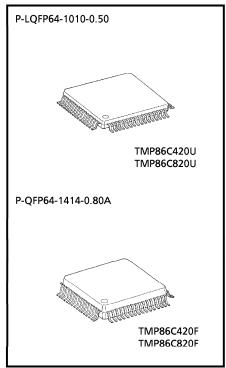
# TMP86C420U/F, TMP86C820U/F

The TMP86C420/820 are the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, LCD driver, multi-function timer/counter, serial interface (SIO), a 8-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	PACKAGE	OTP MCU	
TMP86C420U/F	4 K × 8 bits	250 0  -14-	P-LQFP64-1010-0.50	TN4D0CDN420A11/AF	
TMP86C820U/F	$8  \text{K} \times 8  \text{bits}$	256 × 8 bits	P-QFP64-1414-0.80A	TMP86PM29AU/AF	

#### **Features**

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- ♦ Instruction execution time: 0.25 μs (at 16 MHz) 122  $\mu$ s (at 32.768 kHz)
- ◆ 132 types and 731 basic instructions
- 15 interrupt sources (External: 5, Internal: 10)
- ◆ Input/Output ports (39 pins) (Out of which 24 pins are also used as SEG pins)
- 18-bit timer counter: 1 ch
  - Timer, Event counter, Pulse width measurement, Frequencymeasurement modes
- ◆ 8-bit timer counter: 2 ch
  - Timer, Event counter, PWM output, Programmable Divider Output PPG modes
- Time Base Timer
- Divider output function



● For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled

Quality and Reliability Assurance / Handling Precautions.

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

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- ♦ Watchdog timer
  - Interrupt source/reset output (programmable)
- ◆ Serial interface
  - 8-bit SIO: 1ch
- ♦ 8-bit successive approximation type AD converter
  - Analog input: 8 ch
- ◆ Four key-on wake-up pins
- ◆ LCD driver/controller
  - Built-in voltage booster for LCD driver
  - With displaymemory
  - LCD direct drive capability (Max 32 seg × 4 com)
  - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- ◆ Dual clock operation
  - Single/Dual-clock mode
- ♦ Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer.

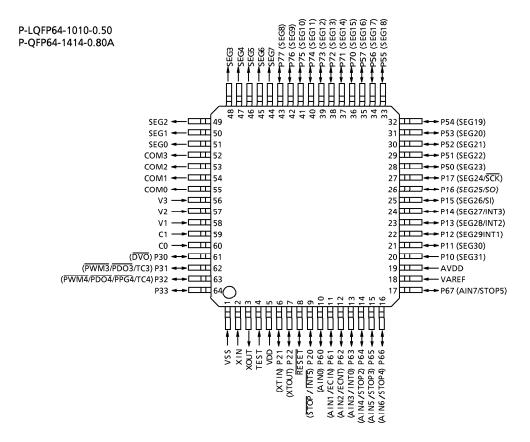
    Release by falling edge of TBTCR < TBTCK > setting.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interruputs.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interruputs.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer.

    Release by falling edge of TBTCR < TBTCK > setting.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- $\bullet~$  Wide operating voltage: 1.8 to 5.5 V at 4.2 MHz/32.768 kHz,

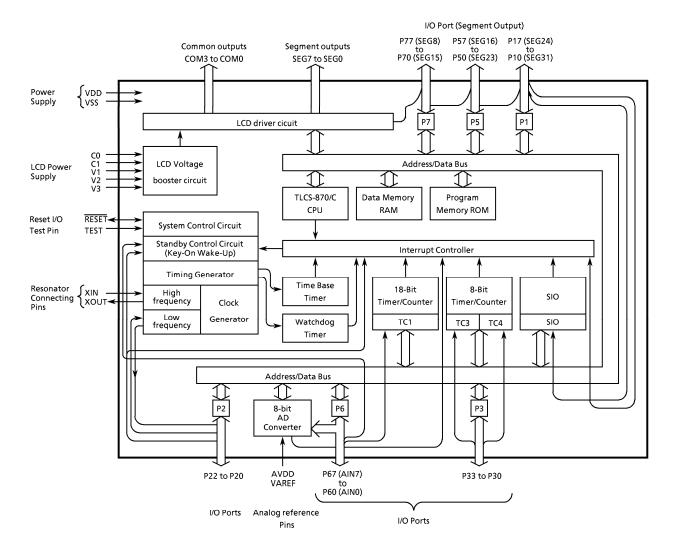
2.7 to 5.5 V at 8 MHz/32.768 kHz,

4.2 to 5.5 V at 16 MHz/32.768 kHz

## Pin Assignments (Top View)



## **Block Diagram**



# **Pin Function**

Pin Name	Input/Output		Function				
P17 (SEG24, SCK)	I/O (I/O)		Serial clock input/output				
P16 (SEG25, SO)	I/O (Output)	8-bit input/output port with latch.	Serial data input				
P15 (SEG26, SI)	I/O (I/O)	When used as input port, an external	Serial data input				
P14 (SEG27, INT3)	I/O (I/O)	interrupt input and serial interface input/output, the P1LCR must be set	External interrupt 3 input	LCD segment			
P13 (SEG28, INT2)	1/0 (1/0)	to "0" after setting output latch to	External interrupt 2 input	outputs.			
P12 (SEG29, INT1)	1/0 (1/0)	"1". When used as a LCD segment output,	External interrupt 1 input				
P11 (SEG30)	I/O (Output)	the P1LCR must be set to "1".					
P10 (SEG31)	I/O (Output)						
P22 (XTOUT)	I/O (Output)		Resonator connecting pins (32.				
P21 (XTIN)	I/O (Input)	3-bit input/output port with latch.	For inputting external clock, X	ΓIN is used and			
		When used as an input port, the output latch must be set to "1".	XTOUT is opened.	· · · · · · · · · · · · · · · · · · ·			
P20 (ĪNT5, STOP)	I/O (Input)	output later must be set to 1.	External interrupt input 5 or ST signal input	OP mode release			
P33	I/O	4-bit programmable input/output					
P32 (PWM4, PDO4,	I/O(I/O)	port (Nch high current output). When used as a timer/counter output	Timer securitor 4 in purt/output				
PPG4, TC4)	1/0(1/0)	or divider output, the output latch	Timer counter 4 input/output				
P31 (PWM3, PDO3, TC3)	I/O(I/O)	must be set to "1". When used as an input port or timer/counter input, the P3OUTCR must be set to "0" after	Timer counter 3 input/output				
P30 (DVO)	I/O(Output)	P3DR is set to "1".	Divider output				
P57 (SEG16) to P50 (SEG23)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P5LCR must be set to "1".	LCD segment outputs				
P67 (AIN7, STOP5)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port	STOP 5 input				
P66 (AIN6, STOP4)	I/O (Input)	can be individually configured as an	STOP 4 input				
P65 (AIN5, STOP3)	I/O (Input)	input or an output under software control. When used as an analog	STOP 3 input				
P64 (AIN4, STOP2)	I/O (Input)	input, the P6CR must be set to "0"	STOP 2 input	AD converter			
P63 (AIN3, <u>INT0</u> )	I/O (Input)	after setting output latch to "0".	External interrupt 0 input	analog inputs			
P62 (AIN2, ECNT)	I/O (Input)	When used as an input port, a key on wake up input, an external interrupt					
P61 (AIN1, ECIN)	I/O (Input)	input and timer/counter input, the	Timer/counter 1 input				
P60 (AIN0)	I/O (Input)	P6CR must be set to "0" after setting output latch to "1".					
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P7LCR must be set to "1".	LCD segment outputs				
SEG7 to SEG0 COM3 to COM0	Output	LCD segment outputs  LCD common outputs					
V 3 to V 1	LCD voltage	LCD voltage booster pin. Capacitors a	re required between C0 and C1	pin and V1/V2/V3			
C1 to C0	booster pin	pin and GND.					
XIN, XOUT	Input Output	Resonator connecting pins for high-fre used and XOUT is opened.	quency clock. For inputting ext	ernal clock, XIN is			
RESET	1/0	Reset signal input or watchdog timer ou	utput/address-trap-reset output				
TEST	Input	Test pin for out-going test. Be fixed to I	ow.				
VDD, VSS		+ 5 V, 0 (GND)					
VAREF	Power Supply	Analog reference voltage inputs (High)					
AVDD		AD circuit power supply					

## **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

### 1.1 Memory Address Map

The TMP86C420/820 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C420/820 memory address map. The general-purpose registers are not assigned to the RAM address space.

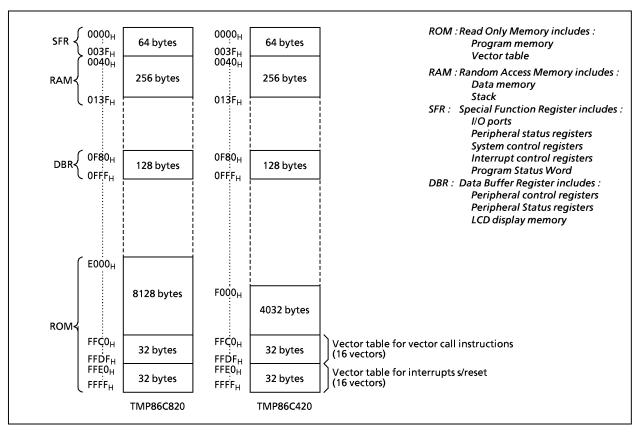


Figure 1-1. Memory Address Maps

### 1.2 Program Memory (ROM)

The TMP86C420 has a 4 K×8 bits (address  $F000_H$  to  $FFFF_H$ ), TMP86C820 has a 8 K×8 bits (address  $E000_H$  to  $FFFF_H$ ) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	1
Output Voltage	V <sub>OUT1</sub>		- 0.3 to V <sub>DD</sub> + 0.3	1 v
	I <sub>OUT1</sub>	P3, P6 Port	- 1.8	1
Output Current (Per 1 pin)	I <sub>OUT2</sub>	P1, P2, P5, P6, P7 Port	3.2	
	I <sub>OUT3</sub>	P3 Port	30	1
Output Compant (Tatal)	Σl <sub>OUT1</sub>	P1, P2, P5, P6, P7 Port	60	mA
Output Current (Total)	ΣI <sub>OUT2</sub>	P3 Port	80	1
Power Dissipation [T <sub>opr</sub> = 85℃]	PD		350	
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 125	°c
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Operating Condition** 

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	С	ondition	Min	Max	Unit
				NORMAL1, 2 mode	4.5		
			fc = 16 MHz	IDLE0, 1, 2 mode	4.5		
				NORMAL1, 2 mode	2.7		
			fc = 8 MHz	IDLE0, 1, 2 mode	2.7		
Supply Voltage	V <sub>DD</sub>			NORMAL1, 2 mode		5.5	
			fc = 4.2 MHz	IDLE0, 1, 2 mode			
			1 no -co	SLOW1, 2 mode	1.8		
				SLEEP0, 1, 2 mode			l v
				STOP mode			
	V <sub>IH1</sub>	Except Hysteresis input	V > 45V		$V_{DD} \times 0.70$		
Input high Level	V <sub>IH2</sub>	Hysteresis input	\ \v_C	$V_{DD} \ge 4.5 V$		$V_{DD}$	
	V <sub>IH3</sub>		V <sub>D</sub>	<sub>DD</sub> < 4.5 V	$V_{DD} \times 0.90$		
	V <sub>IL1</sub>	Except Hysteresis input		<sub>DD</sub> ≧ 4.5 V		$V_{DD} \times 0.30$	
Input low Level	$V_{IL2}$	Hysteresis input	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0D ≡ 4.3 V	0	$V_{DD} \times 0.25$	
	V <sub>IL3</sub>		V <sub>D</sub>	<sub>DD</sub> < 4.5 V		$V_{DD} \times 0.10$	
			V <sub>DD</sub> =	= 1.8 to 5.5 V		4.2	
Clock Frequency	fc	XIN, XOUT	V <sub>DD</sub> =	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$		8.0	MHz
Clock Frequency			V <sub>DD</sub> = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics  $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input		-	0.9	_	V
	I <sub>IN1</sub>	TEST					
Input Current	I <sub>IN2</sub>	Sink Open Drain, Tri-state	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$	-	-	± 2	μΑ
	I <sub>IN3</sub>	RESET, STOP					
Input Resistance	R <sub>IN1</sub>	TEST Pull-Down		-	70	_	kΩ
input Resistance	R <sub>IN2</sub>	RESET Pull-Up		100	220	450	K
Output Leakage Current	I <sub>LO</sub>	Sink Open Drain, Tri-state	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V/0 V	-	-	± 2	μΑ
Output High Voltage	V <sub>OH2</sub>	C-MOS, Tri-st Port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	
Output Low Voltage	V <sub>OL</sub>	Except XOUT and P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{mA}$	-	-	0.4	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Output Low Current	I <sub>OL</sub>	High Current Port (P3 Port)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	-	20	-	
Supply Current in NORMAL 1, 2 mode			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3/0.2 \text{ V}$ $fc = 16 \text{ MHz}$ $fs = 32.768 \text{ kHz}$	-	7.5	9	mA
Supply Current in IDLE 0, 1, 2 mode				_	5.5	6.5	
Supply Current in SLOW 1 mode	l <sub>DD</sub>			_	18	42	
Supply Current in SLEEP 1 mode	Supply Current in SLEEP 1 mode Supply Current in		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ $fs = 32.768 \text{ kHz}$	-	16	25	
Supply Current in SLEEP 0 mode			LCD driver is not enable.	_	12	20	μΑ
Supply Current in STOP mode			$V_{DD} = 5.5 V$ $V_{IN} = 5.3 V/0.2 V$	_	0.5	10	

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 \text{ V}$ 

Note 2: Input current ( $I_{[N1}, I_{[N2})$ ; The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

## **AD Conversion Characteristics**

## $(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V} \le V_{DD} \le 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	$V_{AREF}$		A <sub>VDD</sub> – 1.5	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit	A <sub>VDD</sub>			V <sub>DD</sub>		v
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$		3.0	-	_	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.6	1.0	mA
Non linearity Error			-	_	± 1	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V},$	_	_	± 1	ا , ر
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	_	_	± 1	LSB
Total Error		VAREF = 3.0 V		-	± 2	

## $(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		A <sub>VDD</sub> – 1.5	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit	A <sub>VDD</sub>			V <sub>DD</sub>		v
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$		2.5	-	_	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.5	0.8	mA
Non linearity Error			_	_	± 1	
Zero Point Error		$V_{DD} = A_{VDD} = 2.7 \text{ V},$	-	-	± 1	LSB
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 2.7 \text{ V}$	-	-	±1	LOB
Total Error		VAREF - 2.7 V		-	± 2	

# (V<sub>SS</sub> = 0.0 V, 2.0 V $\leqq$ V<sub>DD</sub> <2.7 V, Topr = -40 to 85°C) Note 5 (V<sub>SS</sub> = 0.0 V, 1.8 V $\leqq$ V<sub>DD</sub> <2.0 V, Topr = -10 to 85°C) Note 5

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	$V_{AREF}$		A <sub>VDD</sub> - 0.9	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit	A <sub>VDD</sub>			$V_{DD}$		
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$	$1.8 \text{ V} \le \text{V}_{DD} < 2.0 \text{ V}$	1.8	-	_	V
	∠ V AREF	$2.0 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	2.0	-	-	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.3	0.5	mA
Non linearity Error			-	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 1.8 \text{ V},$	-	-	± 2	LSB
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{ARFF} = 1.8 \text{ V}$	-	-	± 2	LOB
Total Error		AILEI	-	-	± 4	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.

  About conversion time, please refer to "2.9.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub> V<sub>SS</sub>.

  When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = V_{AREF} V_{SS}$
- Note 5: When AD is used with  $V_{DD} < 2.7 V$ , the guaranteed temperature range varies with the operating voltage.

### **AC** Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Machine Cycle Time		NORMAL 1, 2 mode				
	tcy	IDLE 1, 2 mode	0.25	-	4	_
		SLOW 1, 2 mode	447.6	-	133.3	μS
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	_	31.25	_	ns
Low Level Clock Pulse Width	twcL	fc = 16 MHz				115
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	_	15.26	-	
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz				μS

# $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode			4	
Machine Cycle Time	4	IDLE 1, 2 mode	0.5	-		
	tcy	SLOW 1, 2 mode	447.6	_	133.3	μS
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	_	62.5	_	ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz				113
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	-	15.26	-	c
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz				μ\$

# $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 2.7 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Machine Cycle Time		NORMAL 1, 2 mode			4	
	tor	IDLE 1, 2 mode	0.95	-		
	tcy	SLOW 1, 2 mode	447.6	-	133.3	$\mu$ S
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 4.2 MHz	_	119.05	-	115
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	_	15.26	-	
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz				μS

Timer Counter 1 input (ECIN) Characteristics  $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition		Min	Тур.	Max	Unit
TC1 input (ECIN input) t <sub>1</sub>		Frequency measurement mode V <sub>DD</sub> = 4.5 to 5.5 V	Single edge count	-	-	16	
	t <sub>TC1</sub>	Frequency measurement mode $V_{DD} = 2.7 \text{ to } 4.5 \text{ V}$	Single edge count	I	I	8	MHz
		Frequency measurement mode $V_{DD} = 1.8$ to 2.7 V	Single edge count	ı	-	4.2	

### **Recommended Oscillating Conditions - 1**

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

PARAMETER	Oscillator	Oscillation	Recommended Oscillator		Recommended Constant	
		Frequency			C <sub>1</sub>	C <sub>2</sub>
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF
Oscillation						

# Recommended Oscillating Conditions - 2

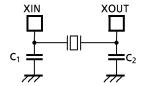
$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

PARAMETER	Oscillator	Oscillation	Recommended Oscillator		Recommended Constant	
		Frequency			C <sub>1</sub>	C <sub>2</sub>
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)

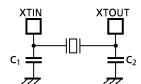
## Recommended Oscillating Conditions - 3

$$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

PARAMETER	Oscillator	Oscillation	Recommended Oscillator		Recommended Constant	
		Frequency			C <sub>1</sub>	C <sub>2</sub>
High-frequency	Ceramic Resonator	4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
Oscillation				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

  For up-to-date information, please refer to the following URL;

  http://www.murata.co.jp/search/index.html

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