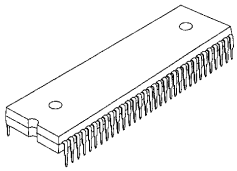
CMOS 8-BIT MICROCONTROLLER

TMP87C841N, TMP87CC41N, TMP87CH41N, TMP87CK41N, TMP87CM41N
TMP87C841F, TMP87CC41F, TMP87CH41F, TMP87CK41F, TMP87CM41F
TMP87C841U, TMP87CC41U, TMP87CH41U, TMP87CK41U, TMP87CM41U

The 87C841/C41/H41/K41/M41 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain CPU core, ROM, RAM, input/output ports, an A/D converter, six multi-function timer/counters, two serial interfaces, and two clock generators on a chip. The 87C841/CC41/CH41/CK41/CM41 provide high current output capability for LED direct drive.

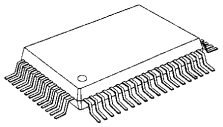
PART No.	ROM	RAM	PACKAGE	OTP MCU
TMP87C841N	8 K × 8-bit	256 × 8-bit	P-SDIP64-750-1.78	TMP87PM41N
TMP87C841F			P-QFP64-1420-1.00A	TMP87PM41F
TMP87C841U			P-LQFP64-1010-0.50D	TMP87PM41U
TMP87CC41N	12 K × 8-bit	512 × 8-bit	P-SDIP64-750-1.78	TMP87PM41N
TMP87CC41F			P-QFP64-1420-1.00A	TMP87PM41F
TMP87CC41U			P-LQFP64-1010-0.50D	TMP87PM41U
TMP87CH41N	16 K × 8-bit		P-SDIP64-750-1.78	TMP87PM41N
TMP87CH41F			P-QFP64-1420-1.00A	TMP87PM41F
TMP87CH41U			P-LQFP64-1010-0.50D	TMP87PM41U
TMP87CK41N	24 K × 8-bit	1K × 8-bit	P-SDIP64-750-1.78	TMP87PM41N
TMP87CK41F			P-QFP64-1420-1.00A	TMP87PM41F
TMP87CK41U			P-LQFP64-1010-0.50D	TMP87PM41U
TMP87CM41N	32 K × 8-bit		P-SDIP64-750-1.78	TMP87PM41N
TMP87CM41F			P-QFP64-1420-1.00A	TMP87PM41F
TMP87CM41U			P-LQFP64-1010-0.50D	TMP87PM41U

P-SDIP64-750-1.78



TMP87C841N
TMP87CC41N
TMP87CH41N
TMP87CK41N
TMP87CM41N
TMP87PM41N

P-QFP64-1420-1.00A



TMP87C841F
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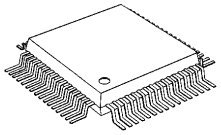
TMP87CH41F
TMP87CK41F
TMP87CM41F
TMP87PM41F

P-LQFP64-1010-0.50D



TMP87C841U
TMP87CC41U
TMP87CH41U
TMP87CK41U
TMP87CM41U
TMP87PM41U

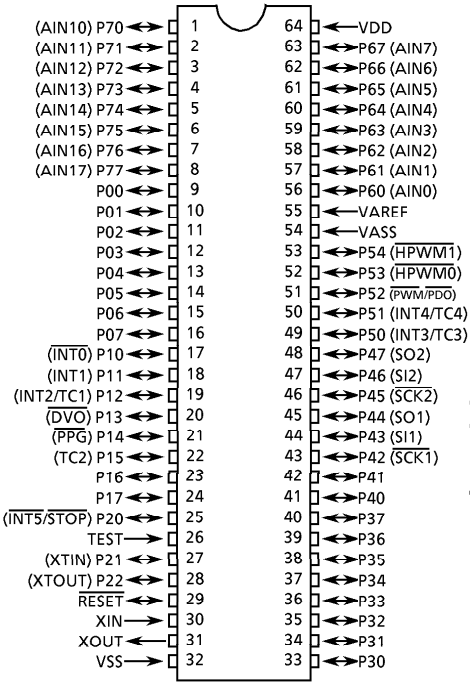
030519EBP2

FEATURES

- ◆8-bit single chip microcomputer TLCS-870 Series
- ◆Instruction execution time : 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- ◆412 basic instructions
  - Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
  - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
  - 16-bit data operations
  - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆15 interrupt sources (External : 6, Internal : 9)
  - All sources have independent latches each, and nested interrupt control is available.
  - 4 edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆Input/Output ports (56 pins)
  - High current output : 8 pins (typ. 20 mA)
- ◆Two 16-bit Timer/Counters
  - Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes
- ◆Two 8-bit Timer/Counters
  - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes
- ◆Time Base Timer (Interrupt frequency : 1 Hz to 16384 Hz)
- ◆Divider output function (frequency : 1 kHz to 8 kHz)
- ◆Watchdog Timer
- ◆High-speed PWM output (2 channel)
  - Cycle : 32 kHz, 64 kHz, 128 kHz.
  - Resolution : 8 bits, 7 bits, 6 bits
- ◆Two 8-bit Serial Interfaces
  - Each 8 bytes transmit/receive data buffer
  - Internal/external serial clock, and 4/8-bit mode
- ◆**10-bit** successive approximate type **A/D converter**
  - 16 analog inputs
  - Conversion time: 23 μs at 8 MHz
- ◆Dual clock operation
- ◆Five Power saving operating modes
  - STOP mode : Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
  - IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE2 mode : CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP mode : CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆**Wide operating voltage** : 2.7 to 5.5 V at 4.19 MHz / 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz.
- ◆Emulation Pod : BM87CM41N0A

PIN ASSIGNMENTS (TOP VIEW)

P-SDIP64-750-1.78



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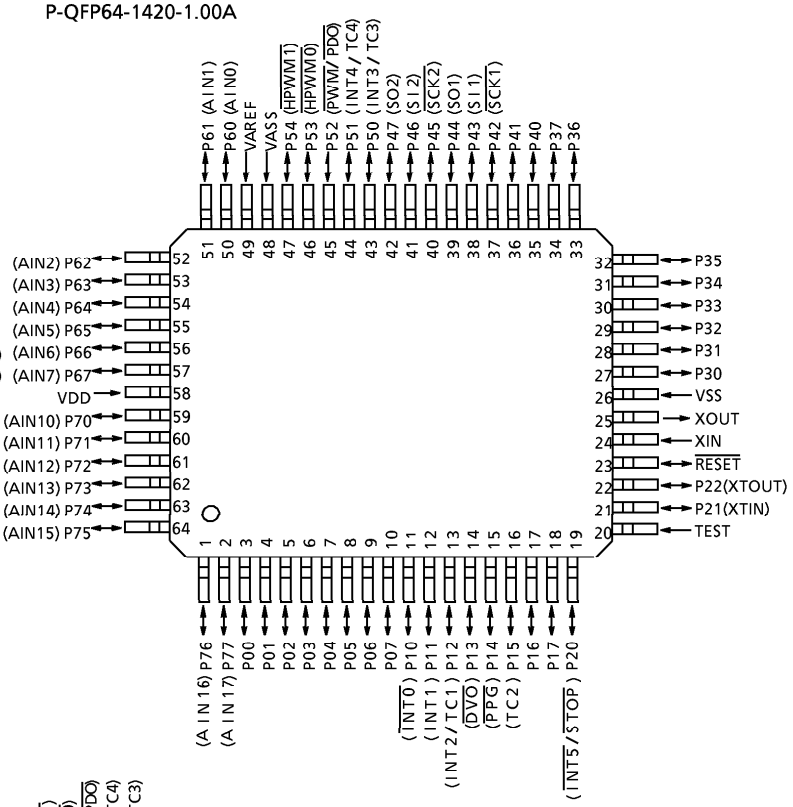

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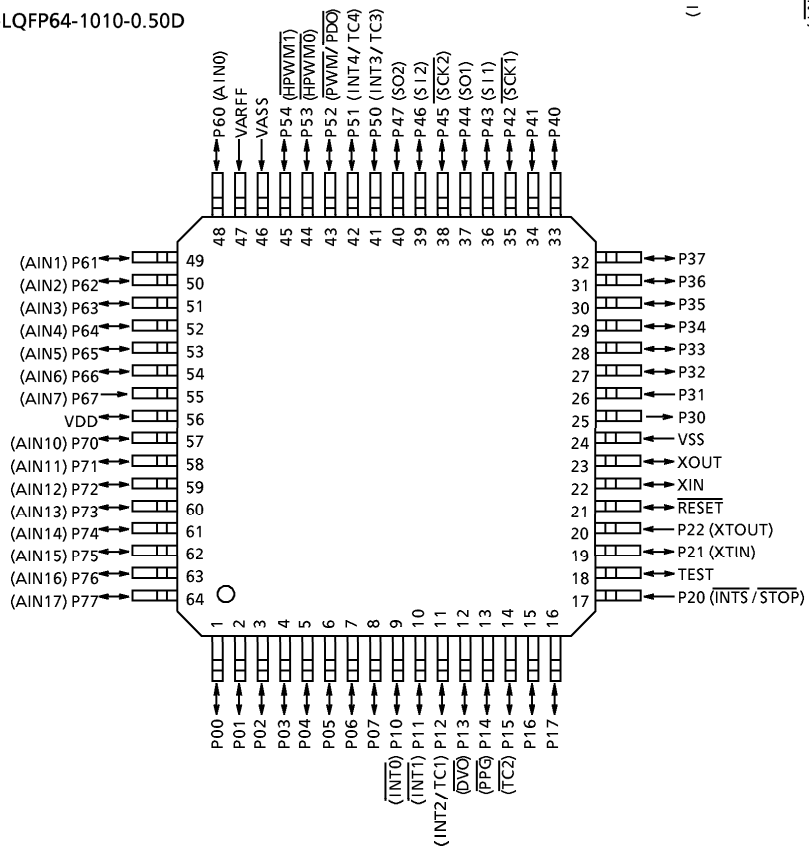
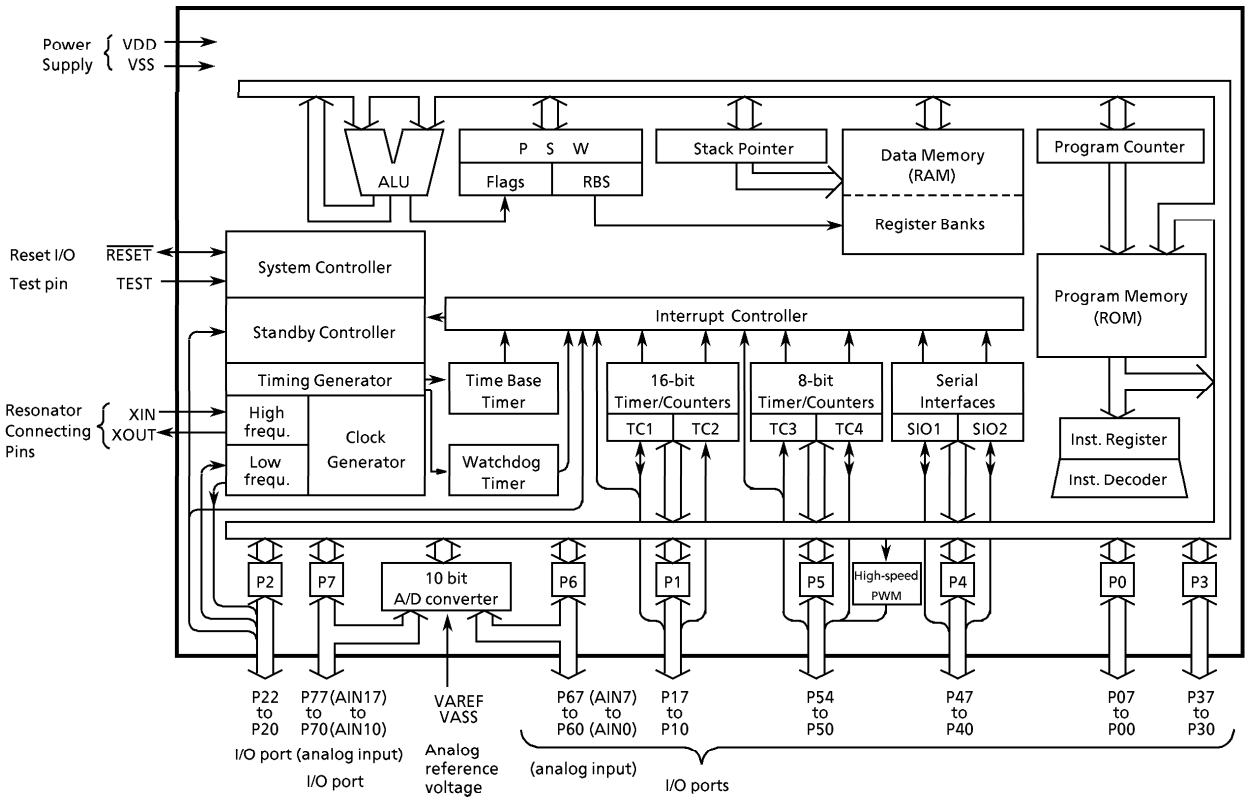


BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTION	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output or a PPG output, the latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P37 to P30	I/O	8-bit input/output port (high current output) with latch. When used as an input port, the latch must be set to "1".	
P47 (SO2)	I/O (Output)	8-bit input/output port with latch. When used as an input port or a SIO input/output, the latch must be set to "1".	SIO2 serial data output
P46 (SI2)	I/O (Input)		SIO2 serial data input
P45 ($\overline{SCK2}$)	I/O (I/O)		SIO2 serial clock input/output
P44 (SO1)	I/O (Output)		SIO1 serial data output
P43 (SI1)	I/O (Input)		SIO1 serial data input
P42 ($\overline{SCK1}$)	I/O (I/O)		SIO1 serial clock input/output
P41, P40	I/O		
P54 ($\overline{HPWM1}$)	I/O (Output)	5-bit input/output port with latch. When used as an input port, an external interrupt input, or a $\overline{PWM}$/$\overline{PDO}$, $\overline{HPWM0}$, $\overline{HPWM1}$ output, the latch must be set to "1".	8-bit High-speed PWM output
P53 ($\overline{HPWM0}$)	I/O (Output)		
P52 ($\overline{PWM}$/$\overline{PDO}$)	I/O (Input)		8-bit PWM output or 8-bit programmable divider output
P51 (INT4/TC4)	I/O (Input)		External interrupt input 4 or Timer/Counter 4 input
P50 (INT3/TC3)			External interrupt input 3 or Timer/Counter 3 input
P67 (AIN7) to P60 (AIN0) P77 (AIN17) to P70 (AIN10)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control. (When used an analog input, the latch must be set to P6CR and P7CR analog input.)	A/D converter analog inputs
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage inputs (High, Low)	

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87C841/CC41/CH41/CK41/CM41. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

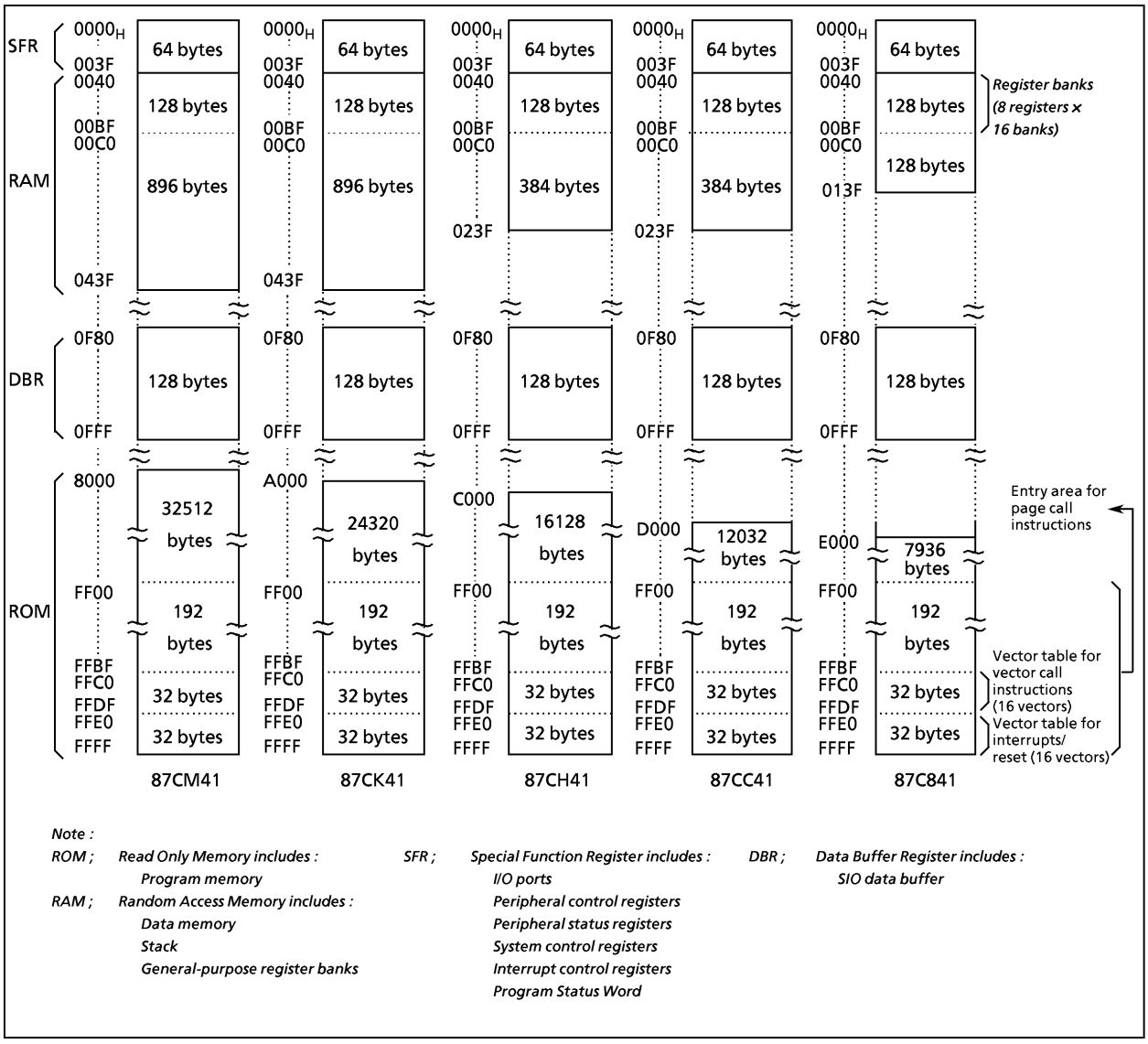


Figure 1-1. Memory Address Maps

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	Σ I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	120	mA
	Σ I_{OUT2}	Port P3	120	
Power Dissipation [Topr = 70 °C]	PD	TMP87C841N/CC41N/CH41N/CK41N/CM41N	600	mW
		TMP87C841F/CC41F/CH41F/CK41F/CM41F/U	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

D.C. CHARACTERISTICS

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis inputs			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V		–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Low Current	I_{IL}	Push pull ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V		–	–	– 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$			90	220	510	kΩ
Output Leakage Current	I_{LO}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	2	μA
		Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5/0 V		–	–	± 2	
Output High Voltage	V_{OH}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	mA
Output Low current	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 8 MHz fs = 32.768 kHz	87C841/CC41/CH41	–	8	14	mA
				87CK41/CM41	–	10	16	
Supply Current in IDLE 1, 2 modes				87C841/CC41/CH41	–	4	6	mA
				87CK41/CM41	–	4.5	6	
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz		–	30	60	μA
Supply Current in SLEEP mode					–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V		–	0.5	20	μA

Note 1 : Typical values show those at Topr = 25 °C , V_{DD} = 5 V.
Note 2 : Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-upor pull-down) is contained.
Note 3 : IDD except I_{REF}.

A/D CONVERSION CHARACTERISTICS

(Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.			UNIT
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	–	V_{DD}			V
	V_{ASS}		V_{SS}	–	1.5			
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}			V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0			mA
Nonlinearity Error		V_{DD} = 5.0, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	± 3	± 2	LSB
Zero Point Error			–	–	± 1	± 3	± 2	
Full Scale Error			–	–	± 1	± 3	± 2	
Total Error			–	–	± 2	± 6	± 4	

Note 1 : $\triangle V_{AREF} = V_{AREF} - V_{ASS}$
Note 2 : ADCDR1 ; 8 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 256)
ADCDR2 ; 10 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 1024)

A.C. CHARACTERISTICS

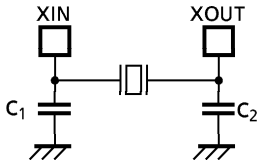
(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	62.5	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

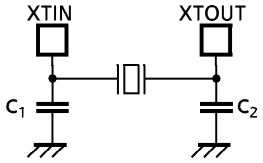
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 40 to 85 °C)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator	Recommended Constant	
				C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA KBR4.0MS		
			MURATA CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM 204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note : When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.