TMPZ84C40AP-6 / 41AP-6 / 42AP-6 / 43AF-6 / 44AT-6
TMPZ84C40AM-6 / 41AM-6 / 42AM-6
TMPZ84C40AP-8 / 41AP-8 / 42AP-8

TLCS-Z80 SIO: SERIAL INPUT/OUTPUT CONTROLLER

1. GENERAL DESCRIPTION AND FEATURES

The TMPZ84C40A (SIO/0), TMPZ84C41A (SIO/1), TMPZ84C42A (SIO/2), TMPZ84C43A, (hereinafter referred to as SIO) are CMOS version of Z80 SIO and have been designed to provide low power operation.

SIOs are designed for the adaptation to the various serial data communications which are needed to the microcomputer system.

SIOs are able to handle the asynchronous signal, the synchronous byte unit protocol and the synchronous bit unit protocol like HDLC and SDLC.

SIOs are fabricated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the SIOs are as follows.

(1) Compatible with the Zilog Z80 SIO.

(2) Compatible with the CCITT-X.25.

(3) Compatible with the HDLC/SDLC.

(4) Data transfer rate up to 800K bit/Sec.

(5) 2 independent full-duplex channels can be used.

(6) Built-in CRC generation and checking function.

(7) On chip daisy-chain structure interrupt circuit.

(8) Low power consumption

4mA Typ. (@5V @6MHz) ··· TMPZ84C40/41/42AP-6, TMPZ84C40/41/42AM-6, TMPZ84C43AF-6, TMPZ84C44AT-6

(9) Single power supply: 5V ± 10% (6MHz VERSION),
5V ± 5% (8MHz VERSION)

(10) Extended operating temperature: −40°C to 85°C (6MHz VERSION),
−10°C to 70°C (8MHz VERSION)

(11) 40 pin DIP package, 40 pin SOP package, 44 pin Mini Flat package, 44 pin PLCC package.

Note : Z80 is a trademark of Zilog Inc., U.S.A.

2. PIN CONNECTIONS AND PIN FUNCTIONS

The pin connections, pin functions and functions of SIOs are described in this chapter.

2.1.1 Pin connections (DIP, SOP)

The pin connections of the SIOs are as shown in Figure 2.1, Figure 2.3, and Figure2.5.

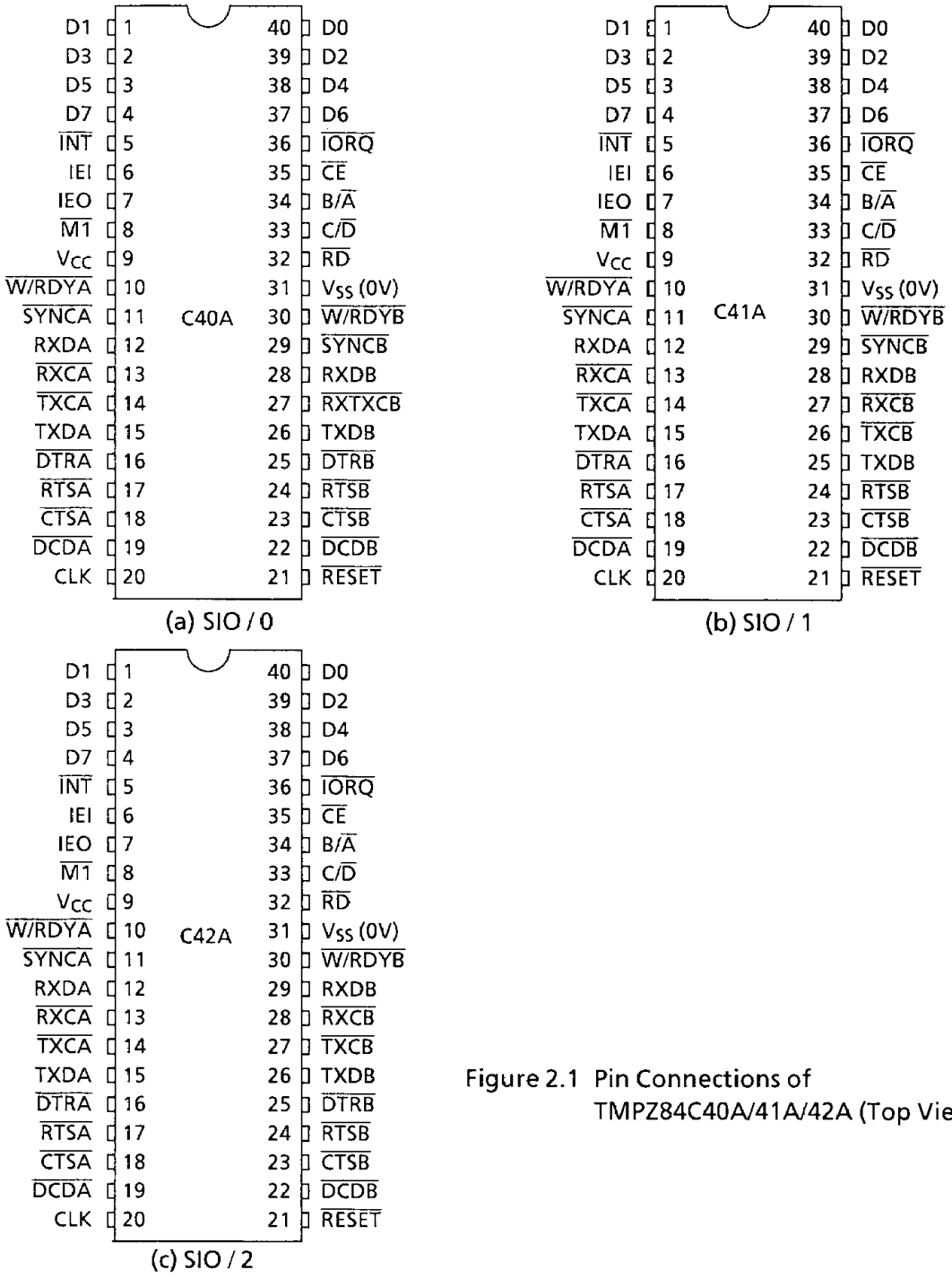

Figure 2.1 Pin Connections of TMPZ84C40A/41A/42A (Top View)

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However, it is necessary to choose the terminals in accordance with the purposes, because they are limited in number. The differences in SIO/0, SIO/1 and SIO/2 are shown in Figure 2.2 (a) SIOs version diagram.

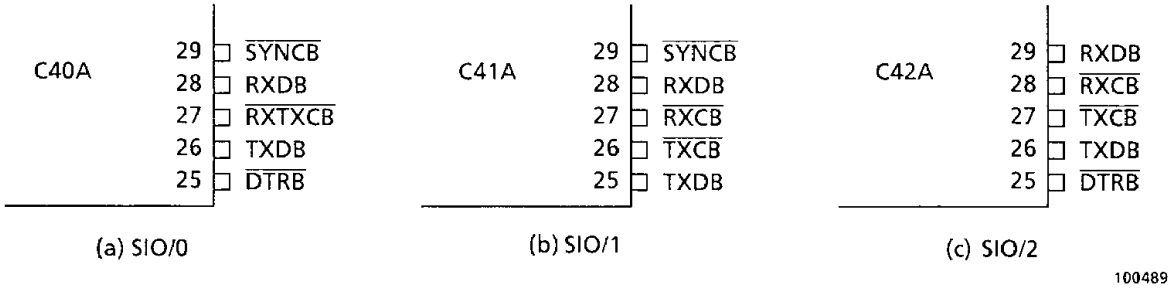
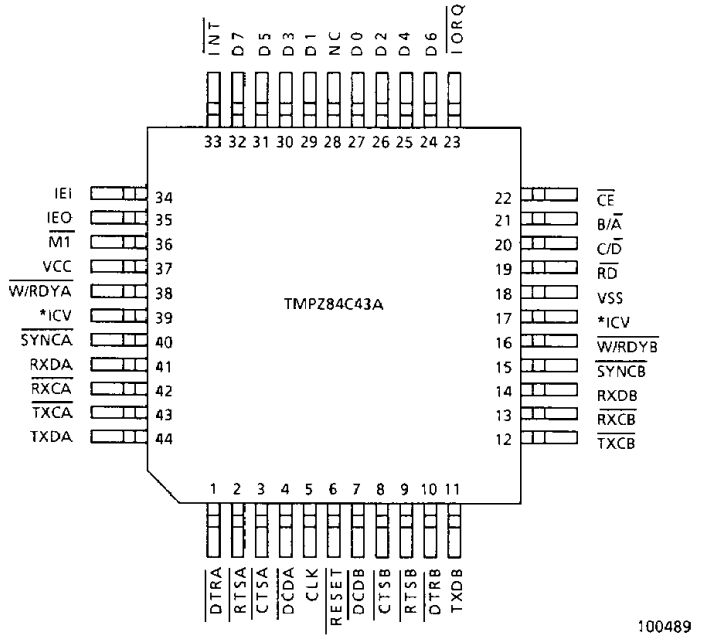


Figure 2.2 (a) SIOs Version (40-pin DIP, 40-pin SOP)

2.1.2 Pin connections (Mini Flat package)



Note 1 : NC must be used at open condition.
Note 2 : *ICV must be used at open condition or connected with VCC.

Figure 2.3 Pin Connections of TMPZ84C43A (Top View)

2.1.3 How to use TMPZ84C43A as SIO/0 or SIO/1 or SIO/2.

The Figure 2.4 shows six terminals to define TMPZ84C43A as SIO/0 or SIO/1 or SIO/2.

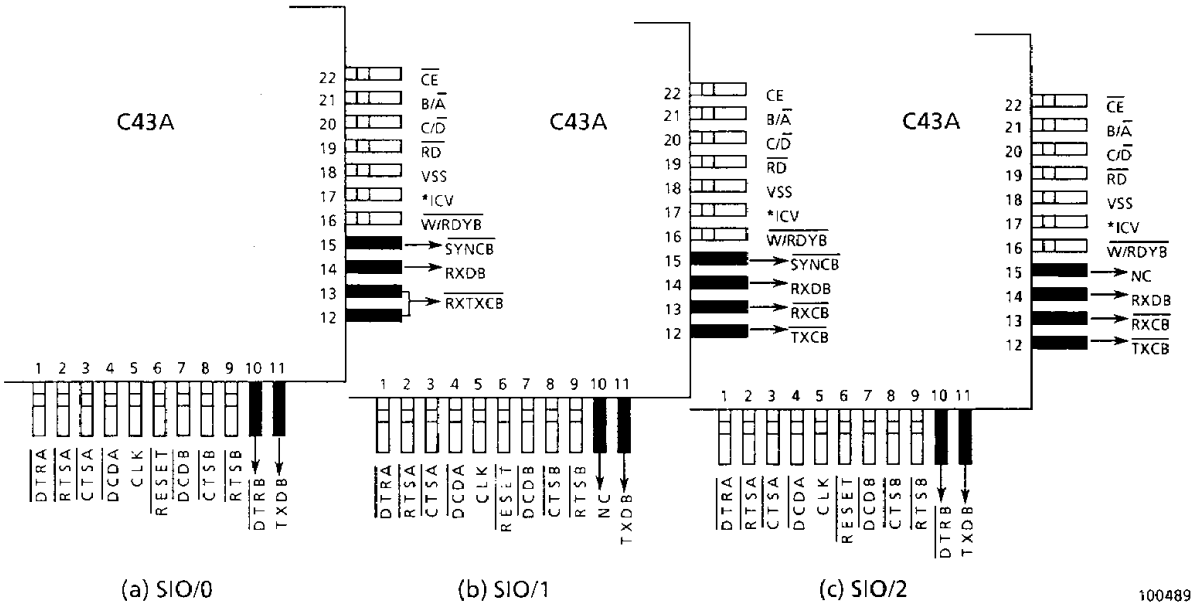
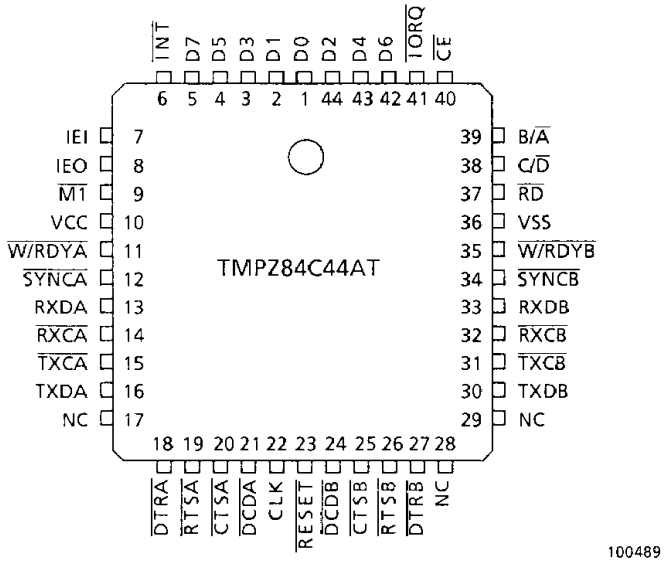


Figure 2.4 How to Use TMPZ84C43A as SIO/0 or SIO/1 or SIO/2

2.1.4 Pin connections (PLCC)



Note 1 : NC must be used at open condition.

Figure 2.5 Pin Connections of TMPZ84C44A (Top View)

2.1.5 How to Use TMPZ84C44A as SIO/0 or SIO/1 or SIO/2.

The Figure 2.6 shows six terminals to define TMPZ84C44A as SIO/0 or SIO/1 or SIO/2.

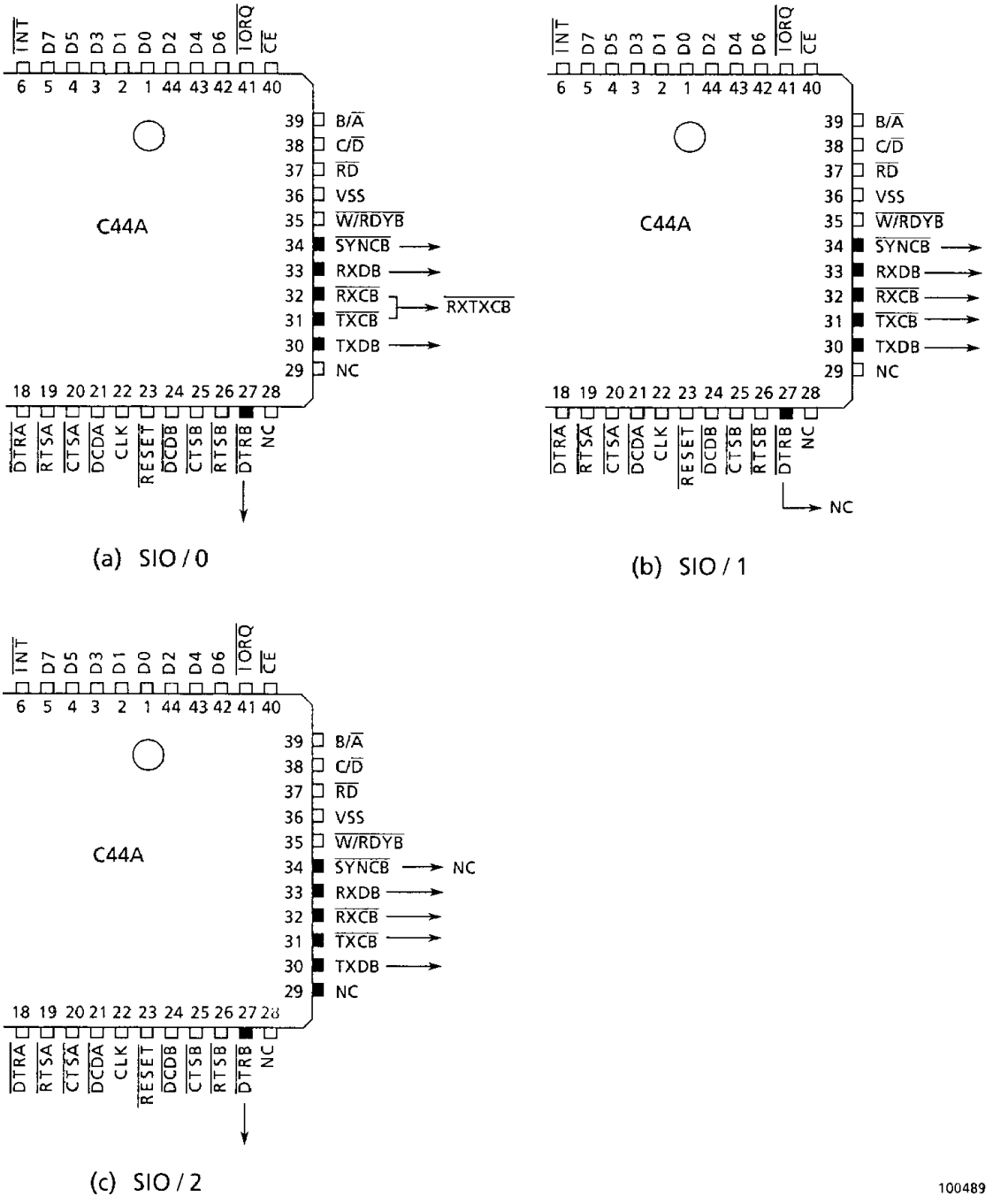


Figure 2.6 How to Use TMPZ84C44A as SIO/0 or SIO/1 or SIO/2

2.2 PIN NAMES AND FUNCTIONS

Table 2.2 Pin Names and Functions (1/2)

Pin Name	Number of Pin	Input/Output 3-state	Function
D0~D7	8	I/O 3-state	8-bit bidirectional data bus.
$\overline{INT}$	1	Output	Interrupt request signal. This is used, in case SIOs request MPU the interrupt. Wired OR connection is possible (because of the open drain).
IEI	1	Input	Interrupt enable input signal.
IEO	1	Output	Interrupt enable output signal. IEI and IEO are used for the daisy-chain structure. When IEI terminal is "1" and IEO terminal is "0", the SIO is being serviced by a MPU interrupt service routine.
$\overline{M1}$	1	Input	Machine cycle 1. When the both of $\overline{M1}$ and $\overline{IORQ}$ are "0", it is the interrupt acknowledge eycle by a MPU to the SIO's interrupt reguest.
$\overline{W/RDYA}$ $\overline{W/RDYB}$	2	Output	Wait/ready signal A, wait/ready signal B. These can be used as wait signal or ready signal according to SIOs-programming. SIO becomes active on "0", when pins are programmed as "WAIT" and are not ready to receive the data for MPU. SIO become active on "0", when pins are programmed as "READY" and ready to receive the data character for DMA.
$\overline{SYNCA}$ *$\overline{SYNCB}$	*2	I/O	Synchronous signal. In case of the asynchronous receive mode, These pins become the same input terminals as $\overline{CTS}$ and $\overline{DCD}$. In case of the external synchronous mode, pins become the input terminals and in case of the internal synchronous mode, become the output terminals.
RxDA RxDB	2	Input	Serial receive data
$\overline{RxCA}$ *$\overline{RxCB}$	*2	Input	Receive clock signal. In asynchronous mode, pins can choose the receive clocks which are 1, 16, 32 and 64 times as large as the data transfer rate according to the program.
TxDA TxDB	2	Output	Serial transmit data
$\overline{DTRA}$ *$\overline{DTRB}$	2	Output	Data terminal ready signal. These pins output the possibility or impossibility of the serial data receive.
$\overline{RTSA}$ $\overline{RTSB}$	2	Output	Transmit request signal. (Request to send) In serial data transmit, become "0".

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Table 2.2 Pin Names and Functions (2/2)

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{CTSA}$ $\overline{CTSB}$	2	Output	Transmittable signal. (Clear to send) When terminals are "0", SIOs can receive the serial data transmit of the modem which has sent these signals.
$\overline{DCDA}$ $\overline{DCDB}$	2	Input	Data carrier detect signal. When terminals are "0", SIOs can enable the serial data transmit.
CLK	1	Input	Signal-phase clock input. Inputs Z80 standard system clock of single-phase. When CLK terminal is DC state ("1" or "0"), SIOs are in stationary state.
$\overline{IORQ}$	1	Input	I/O request signal In case both of $\overline{IORQ}$ and $\overline{CE}$ are "0", the data or command are transferred between MPU and SIO by the combination of B/$\overline{A}$ and C/$\overline{D}$.
$\overline{CE}$	1	Input	Chip enable signal. When input becomes "0", SIOs are enabled.
B / $\overline{A}$	1	Input	Channel select signal Selects the channel (A/B)
C / $\overline{D}$	1	Input	Command/data select signal. Selects the command and data.
$\overline{RD}$	1	Input	Read signal. In case both of $\overline{CE}$ and $\overline{IORQ}$ are "0", if $\overline{RD}$ is "0", this pin performs the read operation and if $\overline{RD}$ is "1", this pin performs the write operation.
$\overline{RESET}$	1	Input	Reset signal. If $\overline{RESET}$ is turned into "0", the receiver and transmitter become disabled and the serial data become the mark state.
*$\overline{RxTxCB}$	*1	Input	Bonding terminal of $\overline{TxCB}$ and $\overline{RxCB}$.
Vcc	1	Power Supply	+ 5V
Vss	1	Power Supply	0V

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Note: The asterisk (*) mark is difference in accordance with the three versions (SIO/0, SIO/1, SIO/2).

3. FUNCTIONAL DESCRIPTION

3.1 BLOCK DIAGRAM

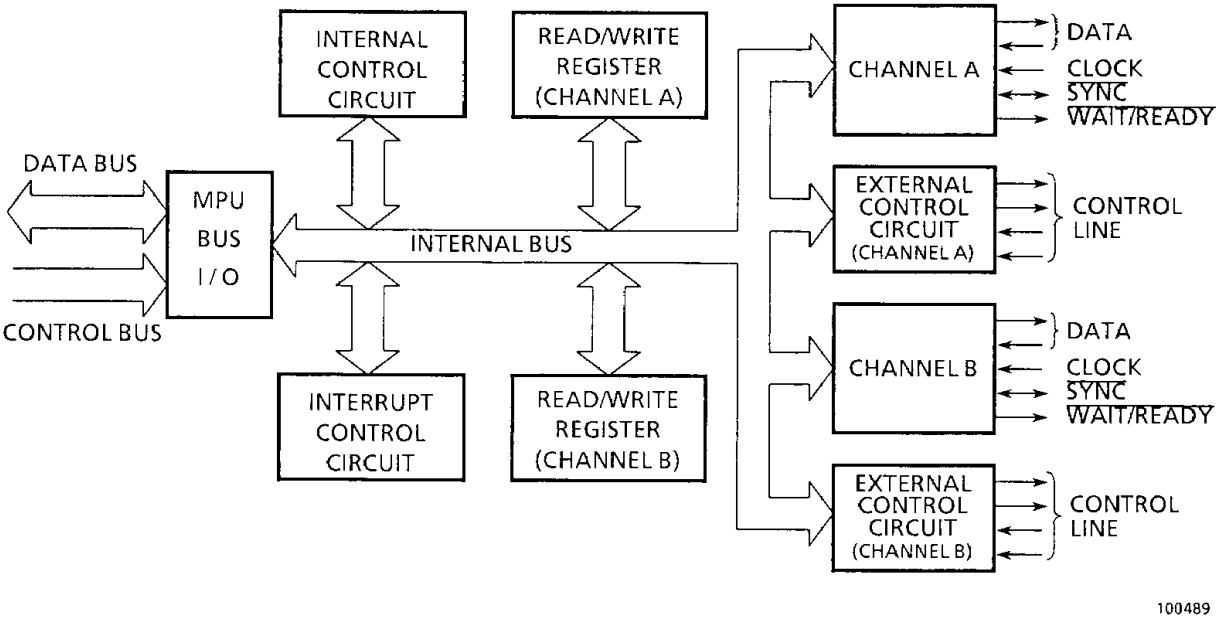

Figure 3.1 Block Diagram

3.2 SYSTEM CONFIGURATION

3.2.1 Architecture

As shown in Figure 3.1, the SIO is composed of MPU bus interface, the internal control circuit, the interrupt control circuit and two full-duplex channels which operate independently. Each channel has the read register, the write register and the external control circuit which is connected to the peripheral LSI or the external device.

Table 3.1 shows the registers in the SIO and their functions. Each channel has eight write registers and three read registers. Refer to 3.4 SIO programming for details.

(1) Communication data path

Figure 3.2 shows the communication path of the transmit/receive data of each channel.

① Receiving

The receiver has an 8-bit receive shift register and a 3-stage 8-bit buffer register in FIFO configuration. This saves time in high-speed data block transfers. The receivers also have the receive error FIFO which holds the status information such as parity and framing errors.

The receive data follow different paths according to the operation mode and character length as shown in Figure 3.2.

Table 3.1 (a) Write Registers

Register		Function
Write register 0	(WR0)	Resets CRC. Sets pointers of registers, and commands.
Write register 1	(WR1)	Sets the interrupt mode.
Write register 2	(WR2)	Sets the vector to be transmitted at interrupt. (Channel B only)
Write register 3	(WR3)	Provides the parameters to control the receiver.
Write register 4	(WR4)	Provides the parameters to control the receiver and transmitter.
Write register 5	(WR5)	Controls the transmitter.
Write register 6	(WR6)	Sets the sync character or the SDLC address field.
Write register 7	(WR7)	Sets the sync character or the SDLC flag.

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Table 3.1 (b) Read Registers

Register		Function
Read register 0	(RR0)	Indicates the receive/transmit buffer state and the pin state.
Read register 1	(RR1)	Indicates the error status and the end-of-frame code.
Read register 2	(RR2)	Indicates the interrupt vector contents. (Channel B only)

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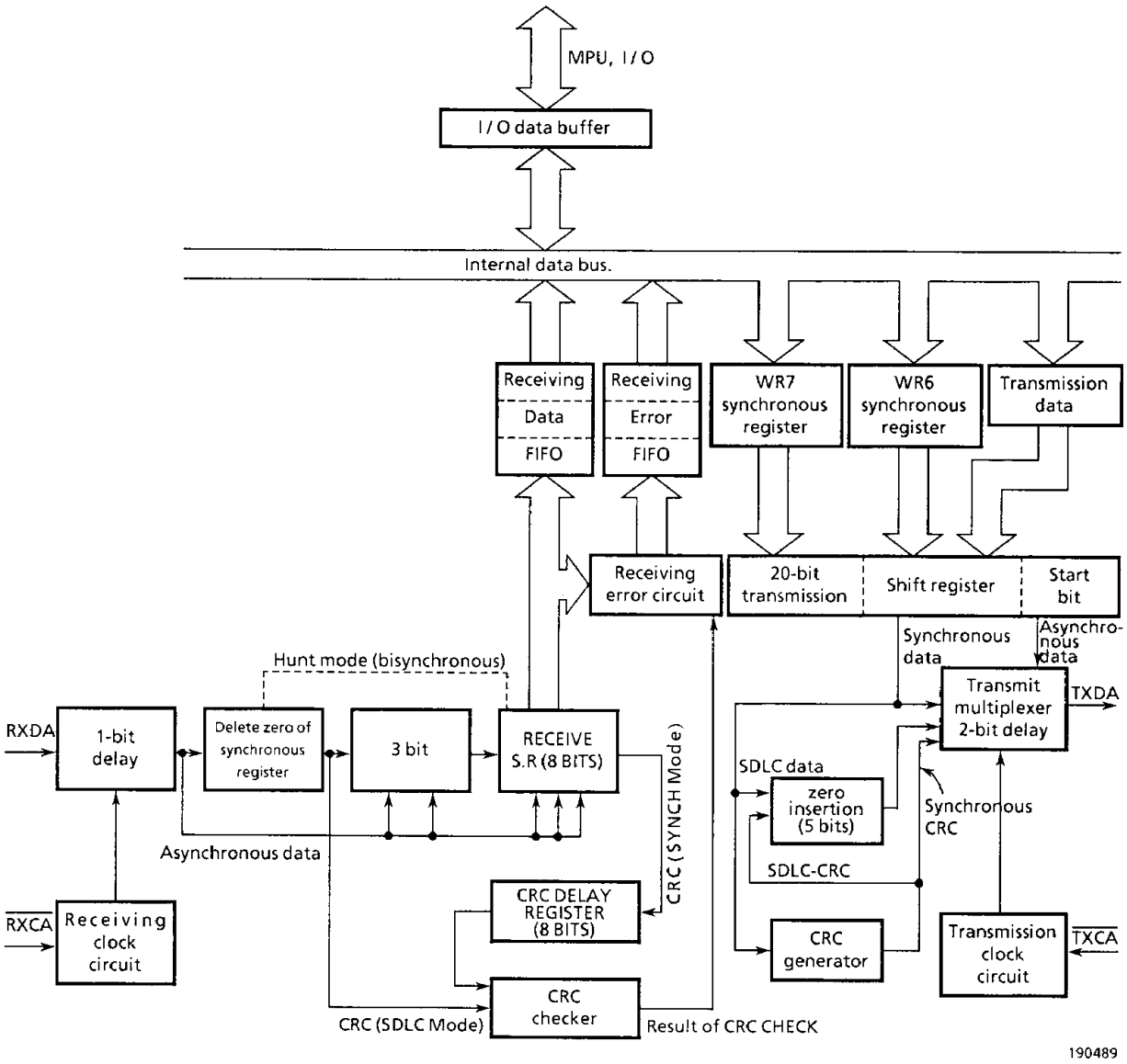

Figure 3.2 Transfer Data path (Channel A)

- Asynchronous mode

  In the asynchronous mode, the receive data enters the 3-bit buffer if the character length is 7 or 8 bits or the 8-bit receive shift register if the character length is 5 or 6 bits.

- Synchronous mode

  In the synchronous mode, the data path depends on the receive processing phase at the time.

The receiver operation starts from the hunt phase. In this mode, the receiver searches the receiver data for the bit pattern which matches the specified sync character. If the SIO is set in the monosync mode, the receiver searches for the bit pattern which matches the sync character set in WR7; if the SIO is set in the bisync mode, the receiver searches for the bit pattern which matches two consecutive sync characters set in WR6 and WR7. When synchronization has been established, the subsequent data enter the 3-bit buffer by bypassing the sync register.

- SDLC mode

In the SDLC mode, the sync register constantly monitors the receive data performing zero deletion as required. When the sync register detects 5 "1" s consecutively in the receive data, the following bit is deleted if it is "0". If it is "1", the bit that follows is checked. If it is "0", it is assumed as a flag, if it is "1", it is assumed an abort sequence (7 consecutive "1"s).

The reformatted data are put in the receive shift register via the 3-bit buffer. When synchronization has been established, the subsequent data follow the same path regardless of the character length.

② Transmission

The transmitter has an 8-bit transmit data register and a 20-bit transmit shift register. The 20-bit transmit shift register holds the data from the WR6, WR7, and transmit data register.

- Asynchronous mode

In the asynchronous mode, the data in the 20-bit transmit shift register are added with the start and stop bits to be sent to the transmit multiplexer.

- Synchronous mode

In the synchronous mode, the WR6 and WR7 hold the sync character. The contents of these registers are sent to the 20-bit transmit register as the sync character at the transmission of data blocks or as the idle sync character if a transmitter underrun occurs in data block transmission.

- SDLC mode

In the SDLC mode, the WR6 holds the station address and the WR7 holds the flag. The flag (WR7) is sent to the 20-bit transmit register at the start and end of each frame. For each of the other data fields, one "0" follows five consecutive "1"s.

(2) I/O functions

To transfer data from/to the MPU, the SIO must be set in the polling, interrupt, or block transfer mode.

- Polling

  To operate the SIO in the polling mode, all interrupts mode must be disabled. In the polling mode, the MPU reads the status bit D0 and D2 in each channel's RR0 to check for reception or transmission.

- Interrupts

  There are 3 types of SIO interrupt: transmit interrupt, receive interrupt, and external/status interrupt. These interrupts can be enabled by program. The receive interrput is further divided into the following three:

  - Interrupt on the first received character
  - Interrupt on all received characters
  - Interrupt on special receive conditions

  Higher priority is given to channel A than channel B. On the same channel, higher priority is given to reception, transmission, and external/status in this order.

  The SIO provides the daisy-chained interrupt priority control feature and the interrupt vector generating feature. Further, it provides the "status affected vector" feature. This feature outputs 4 interrupts depending on the interrupt source.

- Block transfer

  The SIO has the block transfer mode to adapt to the MPU's block transfer and the DMA controller. For block transfer, the $\overline{W/RDY}$ line is used. For the MPU's block transfer, this line is used as the wait line; for the DMA block transfer, it is used as the ready line. The SIO's ready output indicates to the DMA controller that the data is ready to transfer. The SIO's wait output indicates to the MPU that the SIO is not ready for data transfer and therefore requesting the extension of the output cycle.

3.2.2 SIO basic operations

(1) Asynchronous mode

For data transfer in the asynchronous mode, the character length, clock rate, and interrupt mode must be set. These parameters are written in the write registers. Note that WR4 must be set before the other registers are set.

Data transfer does not start until the transmit eneble bit is set. When the auto enable bit is set, the SIO starts transmission upon the $\overline{CTS}$ pin's going "0", allowing the programmer to send a message to the SIO without waiting for the $\overline{CTS}$ signal. Figure 3.3 shows the data format of the asynchronous mode.

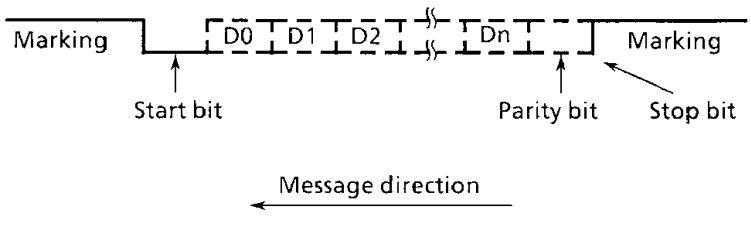

Figure 3.3 Data Format of Asynchronous Mode

① Transmission

Serial data are output from the TxD pin. Its transfer clock rate can be set to one of 1, 1/16, 1/32, and 1/64 times the clock rate to be supplied to the transmit clock input ($\overline{TxC}$). The serial data are output on the falling edge of $\overline{TxC}$.

② Reception

The receive operation in the asynchronous mode starts when the receive enable bit (D0 of WR3) is set. When the receive data input RxD is set to "0" for the duration of at least 1/2 bit time, the SIO interprets it as the start bit, sampling the input data at the middle of the bit time. The sampling is performed on the rising edge of the $\overline{RxC}$ signal.

When the receiver receives the data whose character length is not 8 bits, it converts the data into the one composed of the necessary bits, the parity bit and the unused bit set to "1".

Example : a 6-bit character "

1	P	D5	D4	D3	D2	D1	D0

"

When the external/status interrupt is enabled and a break state is detected in the receive data, the interrupt is generated and the break/abort status bit (D7 of RR0) is set and the SIO monitors the transmit data until the break state is cleared. The interrupt is also generated when the $\overline{DCD}$ signal is in the inactive state for more than the specified pulse width. The DCD status bit is set to "1".

In the polling mode, the MPU must refer the receive character valid bit (D0 of RR0) to read the data. This bit is automatically reset when the receive buffer is read. In the polling mode, the transmit buffer status must be checked before writing data in the transmitter to avoid overwwrite.

(2) Synchronous mode

There are 3 kinds of character synchronization: monosync, bisync, and external sync. In each of these synchronous modes, the times 1 clock rate is used for both transmission and reception. The receive data is sampled on the rising edge of the receive clock input ($\overline{RxC}$).

The transmit data changes on the falling edge of the transmit clock input.

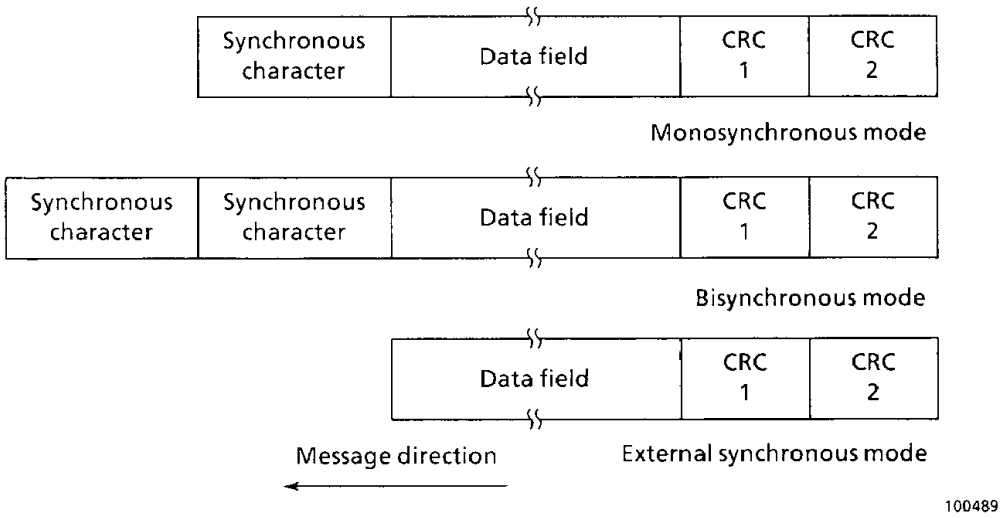

Figure 3.4 Data Format of Synchronous Mode

① Monosync

In this mode, synchronization is established when a match with the sync character (8 bits) set to WR7 is found, enabling data transfer.

② Bisync

In this mode, synchronization is established when a match with 2 consecutive sync characters set to WR6 and WR7 is found, enabling data transfer. In this mode as well as the monosync mode $\overline{\text{SYNC}}$ is active during the receive clock period in which the sync character is being detected.

③ External sync

In this mode, synchronization is performed externally. When synchronization is established, it is indicated by the $\overline{\text{SYNC}}$ pin. The $\overline{\text{SYNC}}$ input must be kept to "0" until the character synchronization is lost. Character assembly starts from the rising edge of the $\overline{\text{RxC}}$ after the falling of the $\overline{\text{SYNC}}$.

After reset, the SIO enters the hunt phase to search for the sync character. If synchronization is lost, the SIO sets the enter-hunt-phase-bit (D4 of WR3) to reenter the hunt phase.

- Transmission

a. Data transfer using interrupt

When the transmit interrupt is enabled, the interrupt is caused upon the transmit buffer's being emptied. For the interrupt processing, other data are written in the transmitter. If these data are not ready for some reason, the transmit underrun condition occurs.

b. Bisync mode

In the bisync mode, if the transmitter runs out of data during transmission, supply characters are inserted. This is done in two methods. In one method, sync characters are inserted. In the other, characters generated so far are transmitted followed by sync characters. Either of these methods can be selected by the reset transmit underrun/EOM command in WR0.

c. End of transmission

Break can be performed by setting bit D4 of WR5. When break is performed, the data in the transmit buffer and the shift register are lost. When the external/status interrupt is enabled, the SIO generates the interrupt depending on the transmitter state and outputs the vector. This mode can be used for block transfer.

- Reception

a. Interrupt on the first received character

This mode is used for ordinary block transfer. In this mode, the SIO generates the interrupt only for the first character; subsequently, it does not generate the interrupt unless special receive conditions are satisfied.

To initialize these settings, command 4 of WR0 (to be enabled by the next receive interrupt) must be set in advance.

b. Interrupt on all received characters

In this mode, the SIO generates the interrupt for all characters coming into the receive buffer. When the status affect vector has been set, a special vector is generated on a special receive condition.

c. Special receive condition interrupt

This interrupt occurs when any of the above interrupts is selected. The special receive conditions include parity error, receive overrun error, framing error, and end-of-frame (SDLC). These error status bits are latched, so that they must be reset after they are read.

They can be reset by command 6 of WR6 (error reset).

(3) SDLC mode

The SIO supports both the SDLC and HDLC protocols. They resemble each other, so that only the SDLC mode is explained here.

Figure 3.5 shows the data format in the SDLC mode. In the SDLC mode, one data block is called a frame and the message in it is put between the open flag and the close flag. The address field in the frame contains the address of a secondary station. Checking this address, the SIO receives or ignores the frame.

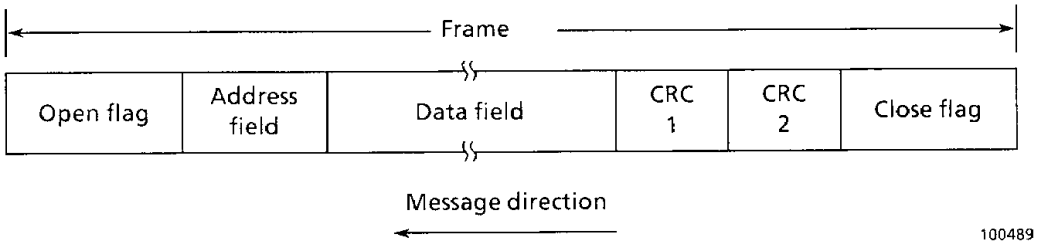

Figure 3.5 Data Format in SDLC Mode

- Transmission

a. Data transfer using interrupt

When the transmit interrupt has been set, the interrupt occurs each time the transmit buffer becomes empty. In the SDLC mode, data are sent to the SIO by this interrupt.

b. Data transfer using wait/ready

The wait function in the wait/ready capability is used to make the MPU extend the output cycle when the SIO's transmit buffer is not empty. The ready function indicates to the DMA that the SIO's transmit buffer is empty and therefore ready to receive data. If no data has been written in the transmit shift register before transmission, the SIO goes in the underrun state. This capability permits data transfer to the SIO.

c. Transmit underrun/EOM

The SIO automatically ends the SDLC frame if there is no data to be transmitted to the transmit data buffer. To implement this, the SIO sends a 2-byte CRC when there is no data to send, then the SIO transmits one or more flags. After reset, the transmit underrun/ EOM status bit is set to prevent the CRC character from being inserted when there is no data to be sent. Using this function, the SIO starts frame transmission. Here, the transmit underrun/EOM reset command must be set in advance between the transmission of the first data and the data end. Thus, the SIO goes in the reset state at the end of each message with the CRC character being sent automatically.

d. CRC generation

For CRC calculation, the CRC generator must be reset before transmission (bits D6 and D7 of WR0). CRC calculation starts when the address field is written in the SIO (WR6).

The transmit CRC enable bit (D0 of WR5) must be set before the address field is written.

e. End of transmission

When the transmitter is disabled during transmission, the data currently transmitted is all transmitted to its end. The subsequent data is put in the marking state. When the transmitter is disabled, characters remain in the buffer. However, the abort sequence is made active when the abort command is written in the command register, deleting all data.

- Reception

As in the transmit mode, several parameters must be preset in the receive mode. The address field is written in WR7 and the flag character in WR7. Receiving the open flag, the receiver compares the contents of the following address field with the address set in WR6 or the global address ("1111 1111"). If the contents of the address field in frame matches either of these address, the SIO starts reception.

a. Interrupt on the first received character

This mode is generally used for the block transfer using the wait/ready capability. In this mode, the SIO generates the interrupt only on the first character. The stauts flag of this interrupt is latched, so that command 4 (to be enabled by the next received character) of WR0 must be preset for re-initialization. When the external/status interrupt is set, an interrupt occurs every time the $\overline{DCD}$ changes. This interrupt also occurs when the special receive condition is satisfied.

b. Interrupt on all received characters

In this mode, the SIO generates an interrupt on all received characters. When the status affect vector has been set, the SIO generates a special vector on the special receive condition interrupt.

c. Special receive condition interrupt

Using the special receive condition, the interrupt on the first received character or the interrupt on all received characters must be selected in advance. The receive overrun status of the special receive condition interrupt is latched. The status bit can be reset by the error reset command (WR0 command).

d. CRC check

The receive CRC check is reset when the open flag at the head of a frame is received. CRC calculation is performed on the subsequent characters up to the close flag. In the SDLC mode, the transmit CRC is inverted, so that a special check sequence is used. The check must end with "0001 1101 0000 1111". Since SIO handles the CRC character as a data, the MPU must discard it after reading it.

e. End of transmission

When the SIO receives the close flag, the end-of-frame-bit is set to indicate that the close flag has been received. When the status affect vector has been set, the special receive condition interrupt occurs and the interrupt vector is output. Any frame can be aborted by abort transmission. When the external/status interrupt has been set, the interrupt occurs and the break/abort bit in RR0 is set.

3.3 SIO STATUS TRANSITION DIAGRAM AND BASIC TIMING

3.3.1 Status transition diagram

Figure 3.6 shows the SIO status transition diagram.

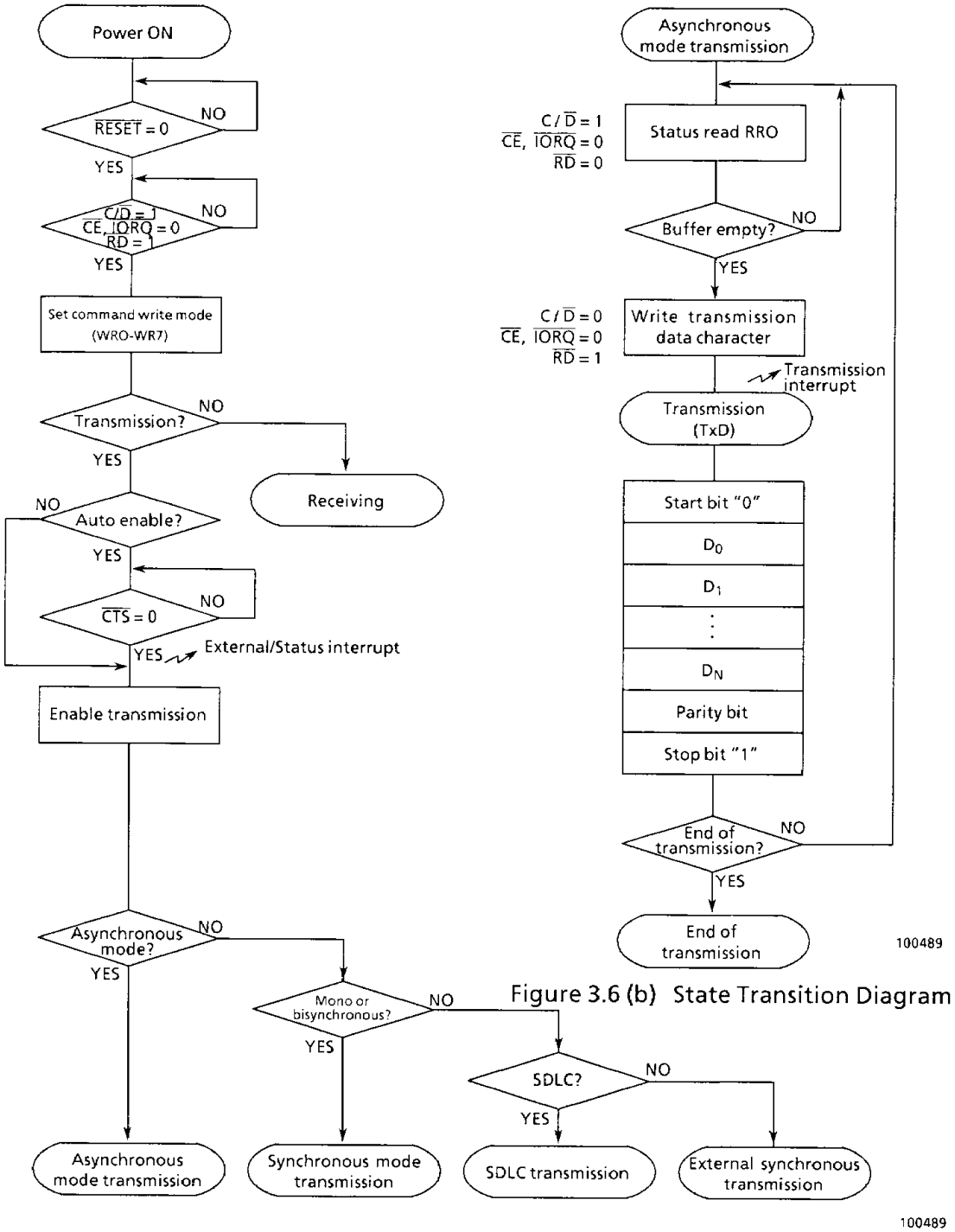

Figure 3.6 (b) State Transition Diagram

Figure 3.6 (a) SIO Status Transition Diagram

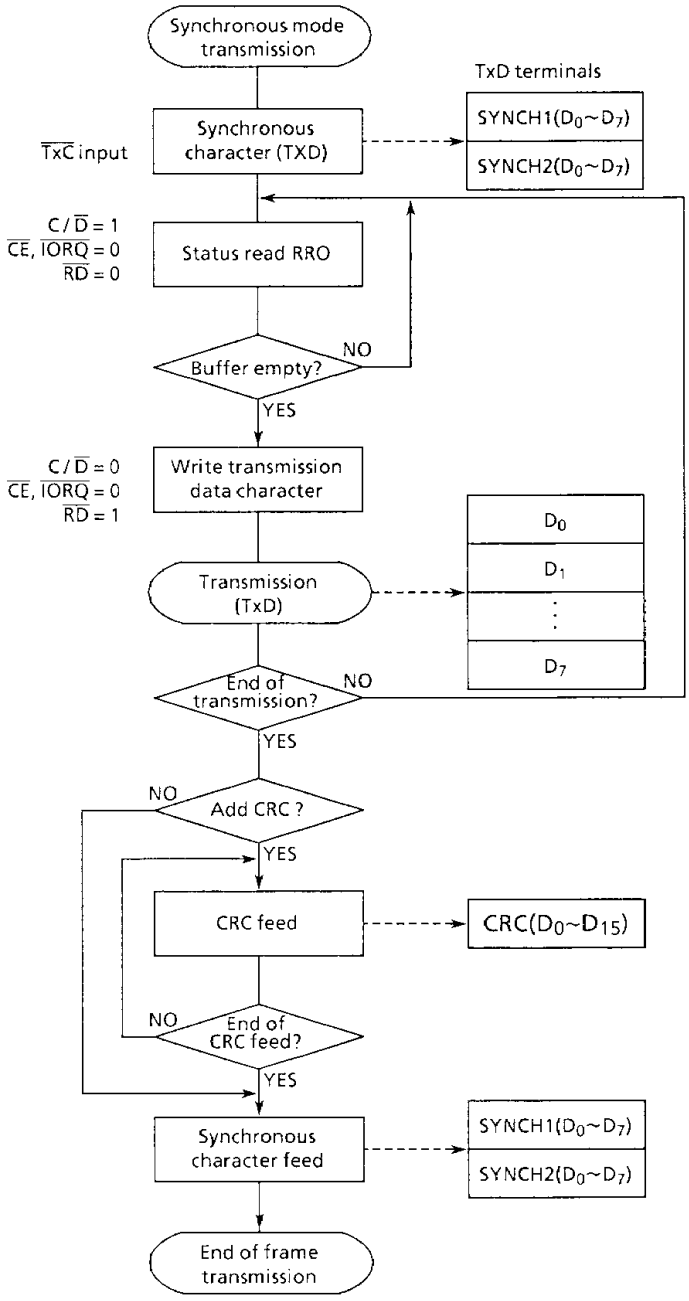

Figure 3.6 (c) State Transition Diagram

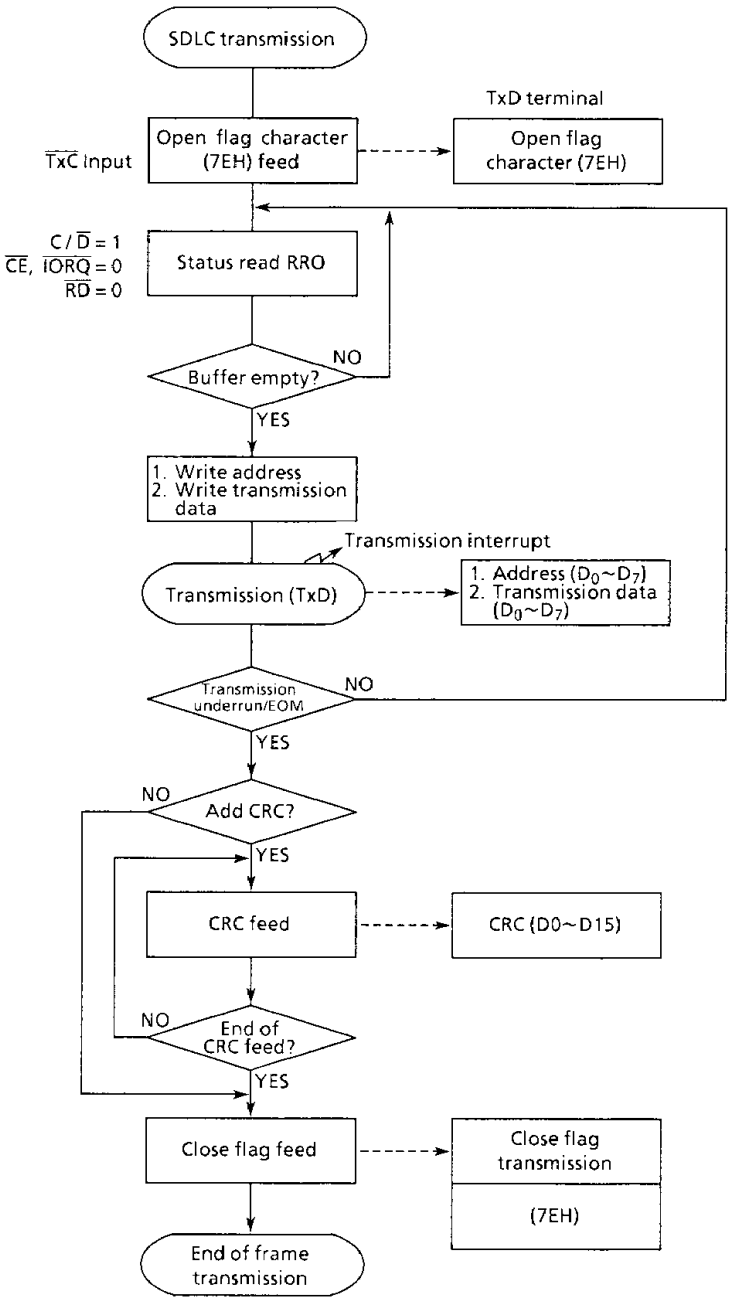

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Figure 3.6 (d) SIO Status Transition Diagram

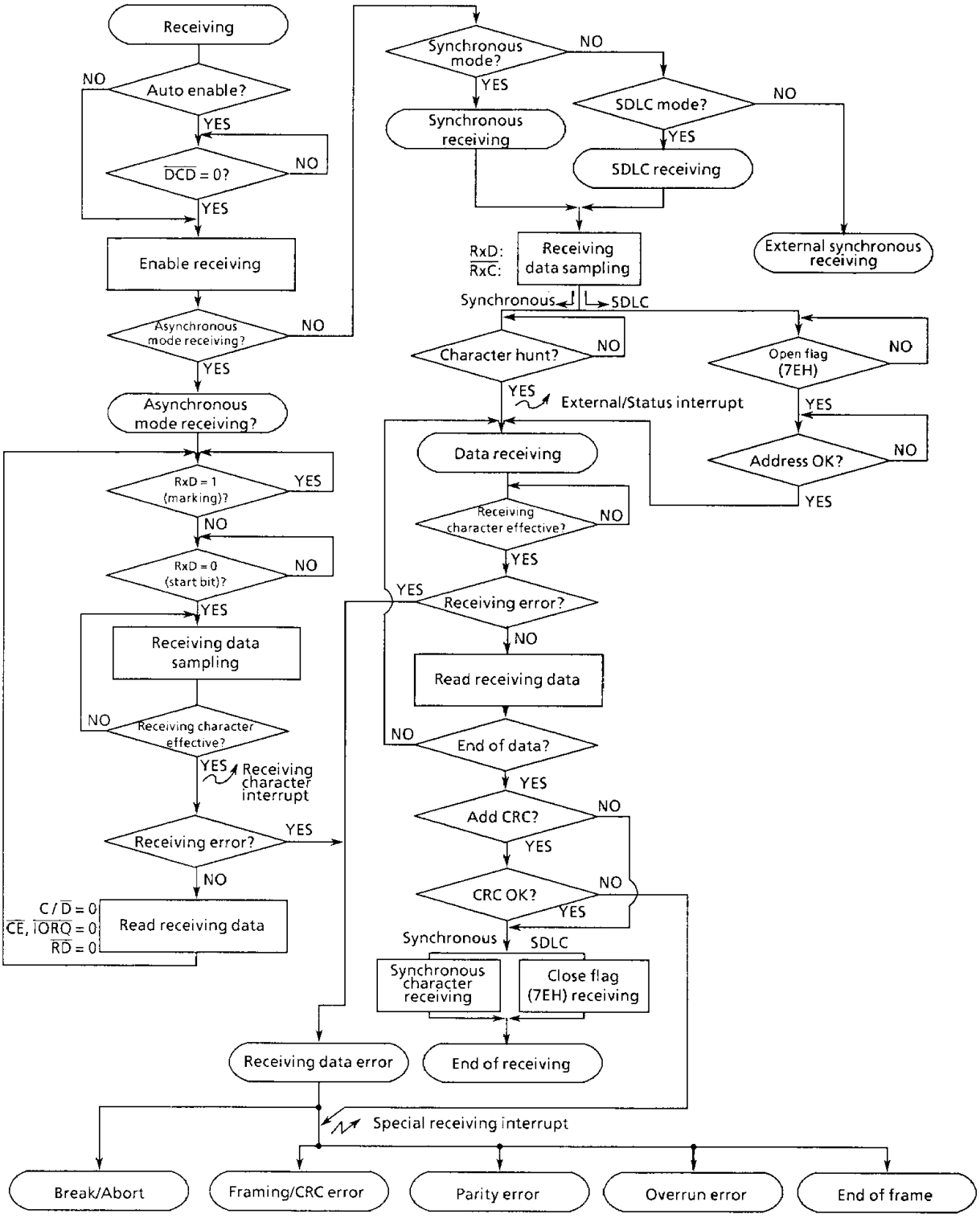

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Figure 3.6 (e) State Transition Diagram

3.3.2 Basic timing

Figure 3.7 shows the timing in which data or a command is written from the MPU to the SIO. Figure 3.8 shows the timing in which data is read from the SIO to the MPU. Figure 3.9 shows the interrupt acknowledge timing in which the MPU gives an interrupt response to the SIO's interrupt request to set the $\overline{IORQ}$ pin to "0" several clocks after setting the $\overline{M1}$ pin to "0" as the acknowledge signal. To maintain the interrupt serviced state in daisy chain structure, the interrupt request state cannot be changed while $\overline{M1}$ is active.

Figure 3.10 shows the timing in which the return from interrupt is performed.

Figure 3.11 shows how the daisy chain structure works. First, suppose that the SIO is servicing interrupt. When the PIO issues an interrupt request immediately before the first byte "EDH" of the RETI instruction is decoded with $\overline{M1}$ being active, "IEO" of the PIO goes "0". However, when "EDH" is decoded, the PIO's interrupt request is not acknowledged.

Therefore, the PIO's "IEO" returns to "1". When the second byte "4DH" is decoded, the SIO's "IEO" returns to "1". Therefore, the "IEI" and "IEO" of each peripheral LSI at this point of time all go "1", or out of the interrupt serviced state. The PIO keeps the $\overline{INT}$ pin at "0" until this state is set. Then, the interrupt is serviced starting with the peripheral device of the higher priority.

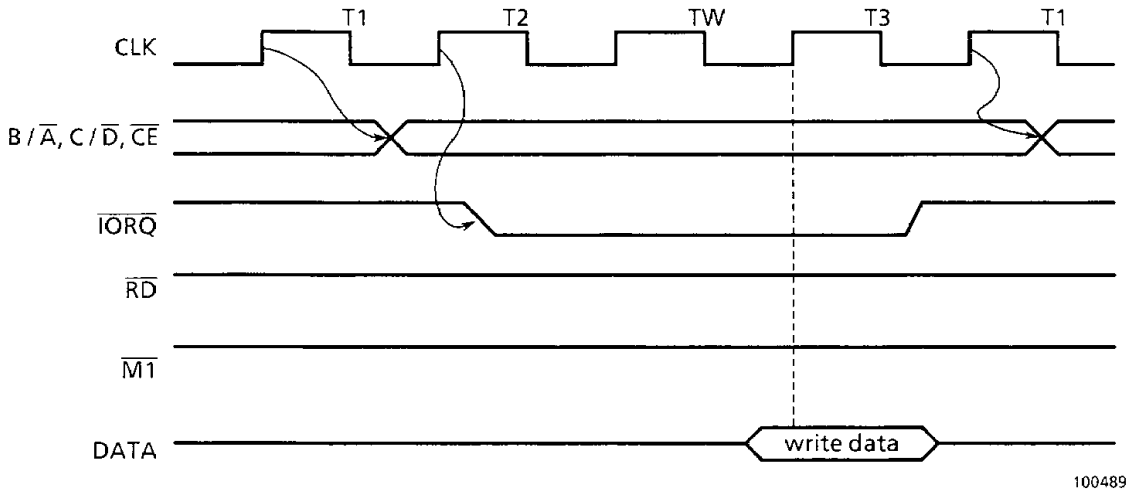


Figure 3.7 Write Timing

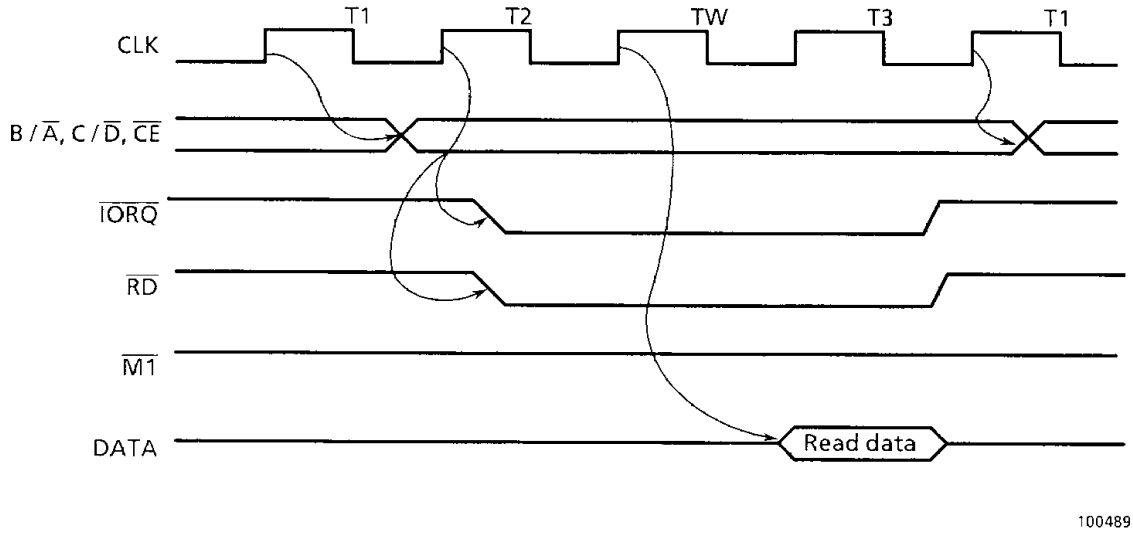


Figure 3.8 Read Timing

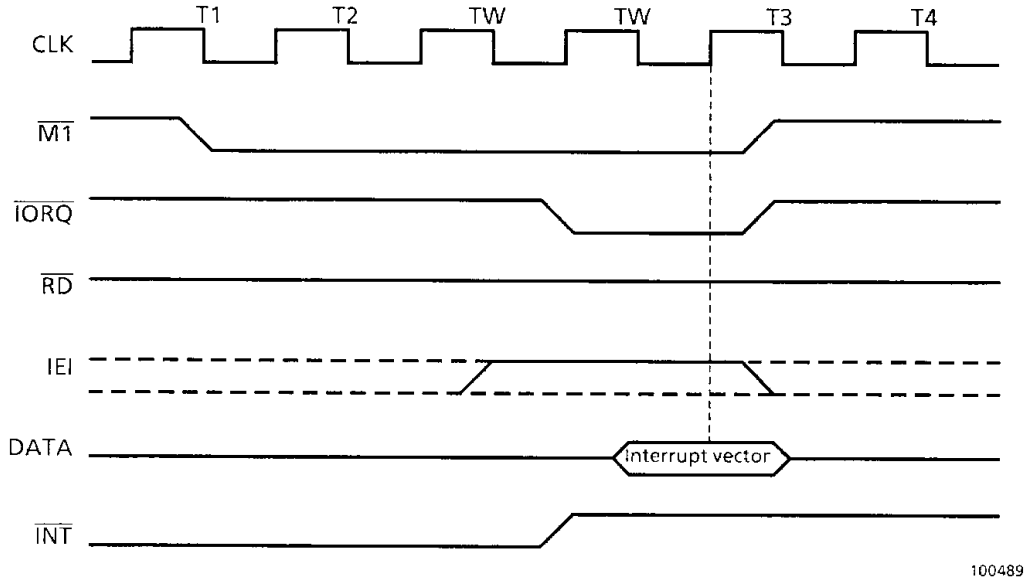


Figure 3.9 Interrupt Acknowledge Timing

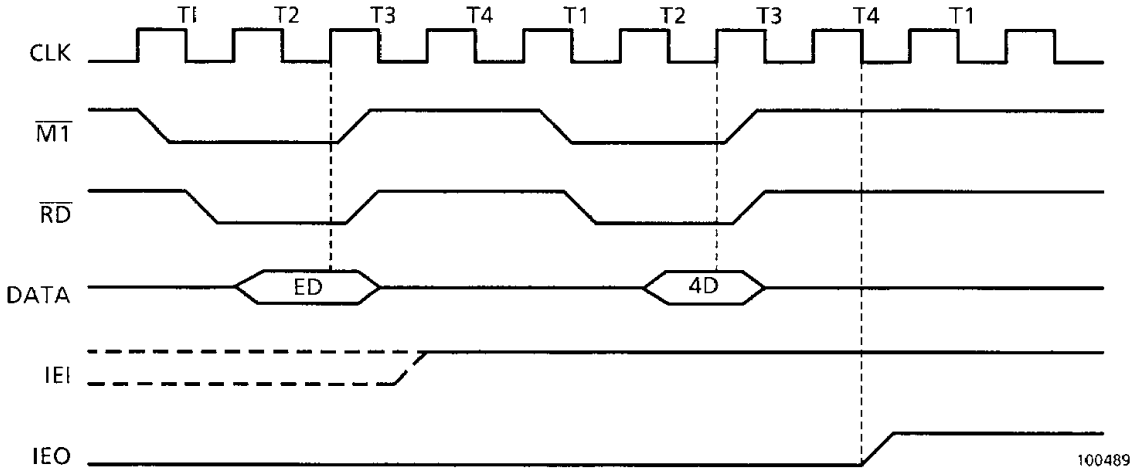
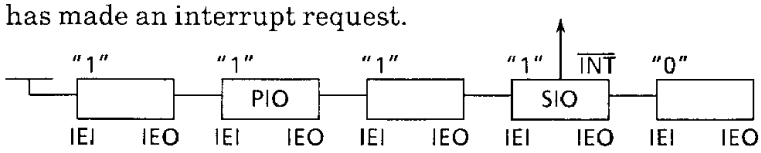
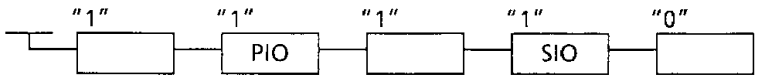


Figure 3.10 Return Timing from Interrupt

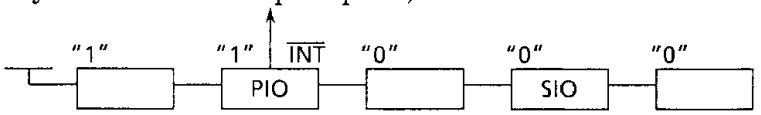
① The SIO has made an interrupt request.



② The SIO is servicing the interrupt.



③ The PIO has made an interrupt request immediately before "EDH" is decoded by the SIO. By the PIO's interrupt request, PIO's IEO is set to "0".



④ Because "EDH" has been decoded, the PIO's interrupt request is not acknowledged. Therefore, PIO's IEO returns to "1".

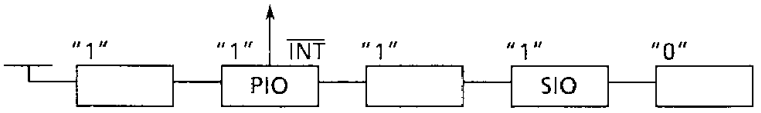


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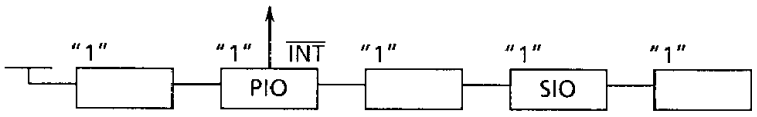
Figure 3.11 Daisy Chain at Execution of RETI Instruction (1/2)

⑤ Because "4DH" has been decoded, the SIO's IEO is set to "1".



⑥ The PIO's interrupt request is acknowledged and the PIO's IEO is set to "0".

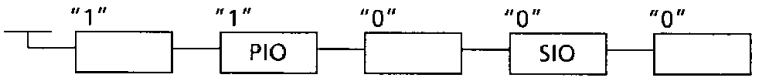


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Figure 3.11 Daisy Chain at Execution of RETI Instruction (2/2)

3.4 SIO OPERATIONAL PROCEDURE

The following mainly describes the meaning of each bit of the write and read registers. Special attention should be directed to the fact that the parameters of the write register (WR4) should be set before the others.

(1) Write registers

WR0; Write register 0

Table 3.2 Configuration of Write Register 0

D7	D6	D5	D4	D3	D2	D1	D0
CRC reset code		Primary command bit			Register pointer bit		

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Bits D0 through D2: Register pointer bits

These bits specify the register on which read/write is performed by the next byte. When read/write is completed, the register pointer points to WR0.

Bits D3 through D5: Basic command bits

- Command 0 (=000) : No operation

  This command only sets the register pointer without making the SIO operate. It is used to invalidate the command in the command chain for the SIO or hold the location at which a command is inserted in the command chain if required.

- Command 1 (=001) : Abort sequence generation

  This command is used to generate the abort sequence (7 or more consecutive "1"s). Note that command 1 is used only in the SDLC.

- Command 2 (=010) : External/status interrupt reset

  Once an external interrupt or a status interrupt has occurred, the status bit of RR0 is latched. This command is issued to enable the RR0's status bit in order to enable the interrupt again.

- Command 3 (=011) : Channel reset

  This command performs generally the same operation as when the $\overline{\text{RESET}}$ pin is set. The difference is that reset is performed only on a single channel. The command for channel A resets the interrupt priority circuit as well.

- Command 4 (=100) : Enable the interrupt at the next character reception.

  This command is used to enable an interrupt when the end of data block has been detected followed by the reception of the next block.

- Command 5 (=101) : Reset transmit interrupt pending

  If the transmit buffer becomes empty in the transmit interrupt enable mode, an interrupt occurs. This command is used to disable the transmit interrupt when there is no data in the transmit buffer.

- Command 6 (=110) : Error reset

  The error (parity or overrun error) caused in block transfer is latched in bits D4 and D5 of RR1. This commands is used to clear these bits.

- Command 7 (=111) : Return from interrupt

  This command performs the same operation as the operation required to execute the RETI instruction on the SIO's data bus. Therefore, non-Z80 CPUs (that is, systems using no RETI instruction) can use the daisy chain in the SIO. This command is available only on channel A.

Bits D6 and D7: CRC reset code

These 2 bits allow the programmer to select between the receive CRC checker reset, the transmit CRC generator reset, and the transmit underrun/EOM reset.

Table 3.3 List of Reset Command Codes

Reset command	D7	D6
No operation	0	0
Reset the receive CRC checker	0	1
Reset the transmit CRC generator	1	0
Reset the transmit underrun/EOM	1	1

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WR1; Write register 1

Table 3.4 Configuration of Write Register 1

D7	D6	D5	D4	D3	D2	D1	D0
Enable	Wait/ready Select function	Select receiving/ transmission	Receiving interrupt mode		Status -affect vector	Enable transmission interrupt	Enble external/ status interrupt

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Bit D0: External/status interrupt enable

When this bit is set, an interrupt is generated at the start of sync character transmission even if the execution is terminated upon detection of break/abort, the $\overline{DCD}$, $\overline{CTS}$ or $\overline{SYNC}$ signal has changed, or the transmit underrun/EOM latch is set.

Bit D1: Transmit interrupt enable

When this bit is set, a transmit interrupt is generated upon the transmit buffer becoming empty.

Bit D2: Status affect vector

When this bit is set, bits D1 through D3 (V1 through V3) of WR2 is changed. When this bit is not set, the same interrupt vector as the contents of WR2 issued. Note that this bit is available only on channel B.

Bits D3 and D4: Receive interrupt mode

These bits are used to select a receive interrupt mode.

Bits D5 through D7: Selection wait/ready functions

These 3 bits are used to select a $\overline{W/RDY}$ pin function. The wait or the ready function is selected by program and they are not used simultaneously. The meaning of these bits are:

- When D5 is set to "1", it indicates that the $\overline{W/RDY}$ pin responds to the receive buffer; when D5 is reset to "0", it indicates that the pin responds to the transmit buffer.
- When D6 is set to "1", the $\overline{W/RDY}$ pin functions as the $\overline{READY}$ pin; when D6 is reset to "0", the pin functions as the $\overline{WAIT}$ pin.
- When D7 is set to "1", the wait/ready function is enabled; when D7 is reset to "0", the function is disabled.

For example, when D7, D6, and D5 are "1", "1", and "0" respectively, and the transmit buffer is full, the $\overline{READY}$ pin goes "1"; when the transmit buffer is empty, the pin goes "0".

Table 3.5 shows the summary of the above description of bits D3 and D4 and D5 through D7.

Table 3.5 List of Receive Interrupt Mode Codes

Receive interrupt mode	D4	D3
Receive interrupt disable	0	0
Interrupt on first received character or special receive conditon*	0	1
Interrupt on received character or special receive condition*	1	0
Interrupt on received character or special receive condition* (except for parity error)	1	1

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* Special receive conditions:
- End of frame (in SDLC mode only)
- Receive overrun error
- Parity error
- Framing error

Table 3.6 Wait/Ready Select Function (D5 through D7)

Pin state			Buffer state	D7	D6	D5
Pin (Function)		Pin output				
DISABLE	$\overline{WAIT}$	Floating	–	0	0	–
	$\overline{READY}$	High	–		1	
ENABLE	$\overline{WAIT}$	Low	The transmit buffer is full and the SIO data port is selected.	1	0	0
		Floating	The transmit buffer is empty.			
	$\overline{READY}$	High	The transmit buffer is full.		1	
		Low	The transmit buffer is empty.			
	$\overline{WAIT}$	Floating	The receive buffer is full.		0	1
		Low	The receive buffer is empty and the SIO data port is selected.			
	$\overline{READY}$	Low	The receive buffer is full.		1	
		High	The receive buffer is empty.			

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WR2; Write register 2

Table 3.7 Configuration of Write Register 2

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	V0

Subject to change under different interrupt conditions if the status-affect vector bit is set.

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This write register is the interrupt vector register. When bit D2 of WR1 is not set, the interrupt vector is issued. When bit D2 of WR1 is set, bits D1 through D3 (V1 through V3) are changed depending on the interrupt generation condition. This time, the contents of WR2 remain unchanged. Because WR2 is available only on channel B, WR2 must be programmed even if only channel A of the SIO is used.

Table 3.8 shows the WR2 bit states in the interrupt condition with the status affect vector being set.

Table 3.8 Channel Interrupt Condition Codes

Channel	Interrupt condition	V3	V2	V1
B	Transmit buffer empty	0	0	0
	Change of external/status	0	0	1
	Received character available	0	1	0
	Special receive condition *	0	1	1
A	Transmit buffer empty	1	0	0
	Change of external/status	1	0	1
	Received character available	1	1	0
	Special receive condition *	1	1	1

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* Special receive conditions :

- End of frame (in SDLC mode only)
- Receive overrun error
- Parity error
- Framing error

WR3; Write resgister 3

Table 3.9 Configuration of Write Register 3

D7	D6	D5	D4	D3	D2	D1	D0
Receiving bit /character		Auto enable	Enter hunt phase	Enable receiving CRC	Address search mode	Prohibit synchronous character load	Enable receiving

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Bit D0: Receive enable

When this bit is set, the receive operation starts. Because this bit is used to start the receive operation, it must be set after the receive-associated programming has been all completed.

Bit D1: Sync character load inhibit

When this bit is set in the sync mode, the sync character is not loaded into the receive buffer.

This bit is used to remove the sync character and idle sync from the received characters.

Bit D2: Address search mode

When this bit is set in the SDLC mode, any message having a programmed address or an address other than the global address (FFH) is not received by WR6. Thefore, the receive interrupt does not occur unless an address match occurs.

Bit D3: Receive CRC enable

When this bit is set, CRC calculation starts at the start of the last data transfer from the receive shift register to the receiver buffer.

Bit D4: Enter hunt Phase

When the establishment of synchronization is required, set this bit to enter the SIO into the hunt phase. The hunt phase is automatically cleared upon establishment of synchronization.

Bit D5: Auto enable

When this bit is set, the transmitter is enabled at the time the $\overline{CTS}$ pin is "0". When the $\overline{DCD}$ pin is "0", the receiver is enabled.

Bits D6 and D7: Receive character length

These bits are used to specify the number of receive bits which make up one character (character length). Table 3.10 shows the number of bits per character.

Table 3.10 Receive Character Length Codes

Bits/character	D7	D6
5	0	0
7	0	1
6	1	0
8	1	1

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WR4; Write register 4

Table 3.11 Configuration of Write Register 4

D7	D6	D5	D4	D3	D2	D1	D0
Clock mode		Synchronous mode		Stop bit		Parity Even/$\overline{\text{Odd}}$	Parity Enable

100489

Bit D0: Parity enable

When this bit is set, 1-bit transmit data is added to the number of bits specified by D6 and D7 of WR3 and the data is received in the resulting number of bits. If a character length other than 8 bits is selected, the added parity bit is set to the MSB side to be transferred to the receive data FIFO. When the 8-bit character length is selected, the parity bit is not transferred to the receive data FIFO.

Bit D1: Parity even/odd

This bit is used to determine whether to perform transfer and check in even or odd parity. (Even parity = "1", odd parity = "0")

Bit D2 and D3: Stop bit length

These bits are used to select the stop bit length in the asynchronous mode. In the synchronous mode, both D2 and D3 must be set to "0".

Table 3.12 Stop Bit Length Codes

Stop bit	D3	D2
Sync mode	0	0
1 stop bit/character	0	1
1.5 stop bits/character	1	0
2 stop bits/character	1	1

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Bits D4 and D5: Sync mode

These bits are used to select the sync mode.

Table 3.13 Sync Mode Codes

Sync mode	D5	D4
8-bit sync mode	0	0
16-bit sync mode (bisync mode)	0	1
SDLC mode (flag character; 7EH)	1	0
External sync mode	1	1

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Bits D6 and D7: Clock mode

These bits are used to select the factor between the transmit/receive clock and the data transfer rate. In the synchronous mode, the ×1 clock mode must be set. In the asynchronous mode, the transmit side and the receive side must have the same factor.

Table 3.14 Clock Mode Codes

Clock mode (data transfer rate)	D7	D6
×1 data transfer rate	0	0
×16 data transfer rate	0	1
×32 data transfer rate	1	0
×64 data transfer rate	1	1

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WR5; Write register 5

Table 3.15 Configuration of Write Register 5

D7	D6	D5	D4	D3	D2	D1	D0
DTR	Transmit bit /character		Break transmission	Enable transmission	CRC-16 / SDLC	RTS	Enable CRC transmission

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Bit D0: Transmit CRC enable

When this bit is set at the time the transmit data is loaded from the transmit data buffer into the transmit shift register, the CRC calculation is performed on that data. If this bit is not set, the CRC calculation and transmission are not performed in the transmit underrun state in the synchronous or SDLC mode.

Bit D1: Request to send (RTS)

When this bit is set, the $\overline{RTS}$ pin goes "0". When this bit is not set, the $\overline{RTS}$ pin goes "1". In the asynchronous mode, the $\overline{RTS}$ pin goes "1" when the transmit buffer becomes empty. In the synchronous or SDLC mode, this bit state is followed by the $\overline{RTS}$ pin state.

Bit D2: CRC-16/SDLC

When this bit is set, the CRC-16 polynomial ($X^{16}+X^{15}+X^{2}+1$) is selected. When this bit is reset to "0", the CRC-CCITT polynomial ($X^{16}+X^{12}+X^{5}+1$) is selected.

Bit D3: Transmit enable

When this bit is set, the transmitter is enabled. Even if this bit is reset to "0" after the start of transmission, the sync character and the data being transmitted are transmitted to the last.

Bit D4: Transmit break

When this bit is set, transmitting any data forcibly puts the transmit data line (TxD pin) in the space state. When this bit is reset to "0", the TxD pin is put in the marking state.

Bits D5 and D6: Transmit character length

These bits indicate the character length of transmit data.

Table 3.16 Transmit Character Length Codes

Bits/character	D6	D5
Less than 5 bits	0	0
7 bits	0	1
6 bits	1	0
8 bits	1	1

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As shown in Table3.16, for the transmission of less than 5 bits (4 bits or 3 bits) per character, D6 and D5 are "0" and "0", which do not indicate how many bits the transmit data consists of. To solve this problem, the data characters must be processed by the format shown in Table 3.17. Note that D indicates data.

Table 3.17 Data Transfer Format with Transmit Data Consisting of Less than 5 bits

Transmit bits/character	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	0	0	D
2	1	1	1	0	0	0	D	D
3	1	1	0	0	0	D	D	D
4	1	0	0	0	D	D	D	D
5	0	0	0	D	D	D	D	D

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Bit D7: data terminal ready

This bit indicates the $\overline{DTR}$ pin state. When this bit is set, the $\overline{DTR}$ pin goes "0", when it is reset, the $\overline{DTR}$ pin goes "1".

WR6; Write register 6

Table 3.18 Configuration of Write Register 6

D7	D6	D5	D4	D3	D2	D1	D0
SYNC							
7	6	5	4	3	2	1	0

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This register is programmed as follows:

- In the external sync mode : Transmit sync character
- In the monosync mode : Transmit sync character
- In the bisync mode : First sync character
- In the SDLC mode : Slave station address

WR7; Write register 7

Table 3.19 Configuration of Write Register 7

D7	D6	D5	D4	D3	D2	D1	D0
SYNC							
15 (7)	14 (6)	13 (5)	12 (4)	11 (3)	10 (2)	9 (1)	8 (0)

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This register is programmed as follows:

- In the monosync mode : Receive sync character
- In the bisync mode : Second sync character
- In the SDLC mode : Flag character (7EH)

This register is not used in the external sync mode.

(2) Read registers

RR0; Read register 0

Table 3.20 Configuration of Read Register 0

D7	D6	D5	D4	D3	D2	D1	D0
Break/ Abort	Transmission underrun /EOM	CTS	Synchro- nize/Hunt	DCD	Transmission buffer empty	Reserve interrupt	Receiving character effective

Used with the external/status interrupt

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Bit D0: Receive character available

This bit is set when the receive buffer holds characters of 1 byte or more. This bit is reset when the buffer becomes empty.

Bit D1: Interrupt pending

This bit is set when an interrupt occurs in the SIO regardless of the interrupt condition type.

This bit is available only on channel A.

Bit D2: Transmit buffer empty

This bit is set when the transmit data buffer becomes empty or the SIO is reset. However, in the sync and SDLC modes where the CRC character is being transmitted, bit D2 is reset.

Bit D3: Data carrier detect

This bit indicates the $\overline{DCD}$ pin input state. This bit is latched when the external/status interrupt occurs.

Bit D4: Sync/hunt

The meaning of this bit depends on the operation mode:

(i) Asynchronous mode

Bid D4 indicates the SIO's $\overline{\text{SYNC}}$ pin state. When the $\overline{\text{SYNC}}$ pin state changes, the external/status interrupt occurs.

(ii) External sync mode

When synchronization has been established by the detection of external synchronization, the last bit of the sync character must be set to "0" at the second $\overline{\text{RxC}}$ falling edge from the rising edge of the received $\overline{\text{RxC}}$. That is, to set the $\overline{\text{SYNC}}$ input to "0" by the external circuit after the detection of synchronization, full 2 receive cycle clocks must be awaited.

When the $\overline{\text{SYNC}}$ input goes "0", the sync hunt bit is set. When synchronization is lost or the end of message is detected, the enter hunt phase bit is set.

(iii) Internal sync mode

In the monosync and bisync modes, bit D4 is initialized to "1" by the enter hunt phase command (D4 of WR3). This bit is reset when the SIO detects the sync character.

(iv) SDLC mode

Bit D4 is set when the receiver is disabled or the enter hunt phase command is issued.

Then, when the frame open flag is detected, this bit is reset.

Bit D5: Clear to send (CTS)

This bit indicates the opposite of the $\overline{\text{CTS}}$ pin input state.

Bit D6: Transmit underrun/EOM

This bit is set when the SIO is reset (including channel reset). Only the reset transmitter underrun/EOM latch command WR0 bits D7, D6 = "1", "1") can reset this bit. When the transmit underrun state occurs, the external/status interrupt is generated. Bit D5 is also used to control transmission in the sync or SDLC mode.

Bit D7: Break/abort

In the asynchronous mode in reception, this bit indicates the break state detection. When the break state is detected, this bit is set, generating the external/status interrupt. This bit is reset by the external/status interrupt reset command.

After break, the external/status interrupt is generated again. In the SDLC mode, bit D7 is set when the abort sequence is detected, generating the external/status interrupt.

RR1; Reader register 1

Table 3.21 Configuration of Read Register1

D7	D6	D5	D4	D3	D2	D1	D0
End of frame	framing error	Receiving overrun error	Parity error	Fraction			Feed all characters

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Bit D0: All sent

In the asynchronous mdoe, this bit is set when all characters are sent from the transmitter or there is no transmit data in the SIO. In the synchronous mode, this bit is always set.

Bits D1 through D3: Fraction codes

Normally, I field is an integral multiple of character length. If it is not, these bits show the number of fraction bits. These codes are effective only for the transmission for which the end of frame bit is set in the SDLC mode.

Example: Figure 3.12 shows examples of fractions in which the number of bits/ character at the end of I field is 8 bits (1) and 4bits (2).

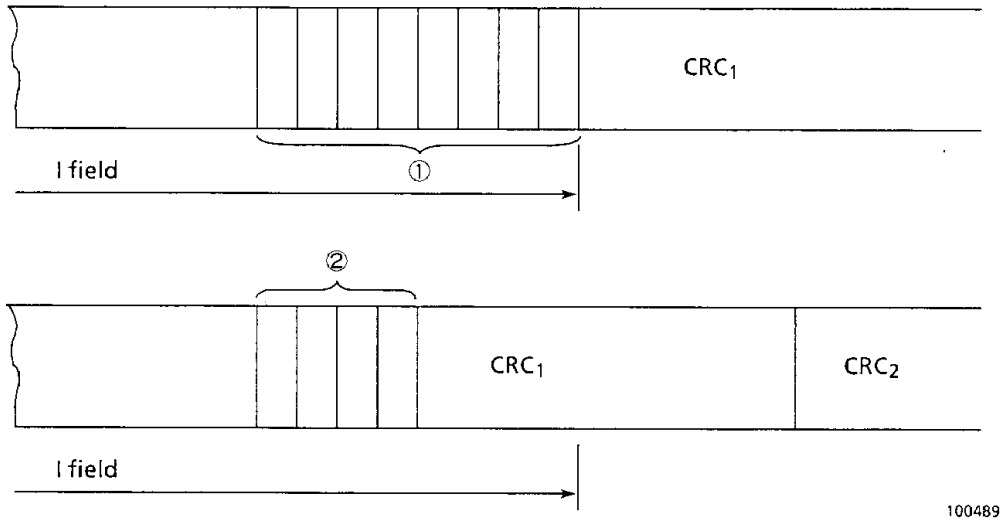

Figure 3.12 Examples of Fraction Bits in I Field

Table 3.22 (a) shows the fraction codes for the receive character whose character length is 8 bits.

Table 3.22 (a) Bit Patterns by Fraction Bits at End of I Field

Number of fraction bits at end of I field		D3	D2	D1
1 byte before	2 bytes before			
0	3	1	0	0
0	4	0	1	0
0	5	1	1	0
0	6	0	0	1
0	7	1	0	1
0	8	0	1	1
1	8	1	1	1
2	8	0	0	0

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The same table can also be provided for each character length when the receive character length of I field is other than 8 bits.

Table 3.22 (b) Bit Patterns by Number of Bits/Character (No Fractions)

Bits/character	D3	D2	D1
5 bits/Character	0	0	1
6 bits/Character	0	1	0
7 bits/Character	0	0	0
8 bits/Character	0	1	1

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Bit D4: Parity error

This bit is latched when the parity select bit (D0 of WR4) is set and a parity error is detected in the receive data. Latch can be cleared by the error reset command (WR0 bits D5, D4, D3 = "1", "1", "0").

Bit D5: Receive overrun error

The receive data FIFO holds up to 3 characters. When more characters are received without read out by the MPU, the excess character is set to the receive FIFO. When this character is read by the MPU, this receive overrun error is set. Once set, bit D5 latches that state. When the error reset command (command 6 of WR0 bits D3 through D5) is written, this bit is also reset.

Bit D6: CRC/framing error

In the asynchronous mode, this bit is set when a framing error is detected in the received character. Because this bit is not latched, it is always updated.

In the synchronous and SDLC modes, this bit indicates the transmitted CRC check result. This bit is reset when the error reset command (command 6 of WR0 bits D3 through D5) is written.

Bit 7: End of frame

This bit is set when the end flag is detected in the receive data. This bit is reset when the error reset command (command 6 of WR0 bits D3 through D5) is written. This bit is used only in the SDLC mode and is updated when the first character of the next frame is received.

RR2; Read register 2

Table 3.23 Configuration of Read Register 2

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt vector							
V7	V6	V5	V4	V3	V2	V1	V0

Subject to change under different interrupt conditions if the status-affect bit is set.

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When the status affect vector bit (D2 of WR1) is set, bits V3 through V1 are changed depending on the interrupt condition at the time. The vector to be read is determined by the interrupt condition having the highest priority at the time of read. When the status affect vector bit is reset, the contents of this register are the same as those of WR2.

3.5.6 Using SIO

The following describes some system examples using the SIO. Figure 3.13 shows an inter-processor communication system. In this example, the MPU on the left side controls the data transfer with the modules on the right side. Both diagrams shown in Figure 3.13 (a) and (b) are communication systems. As shown, the SIO is used to interface with external devices in data communication. The greatest advantage of the SIO is the smaller number of data lines than parallel communication.

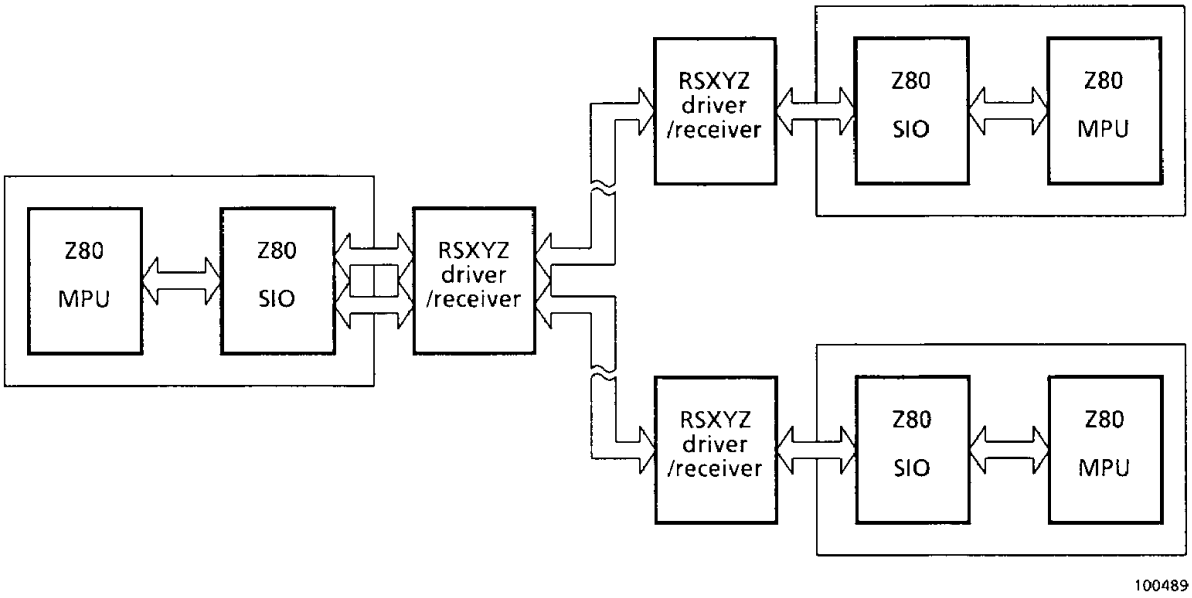

Figure 3.13 (a) Example of Data Communication between Processors

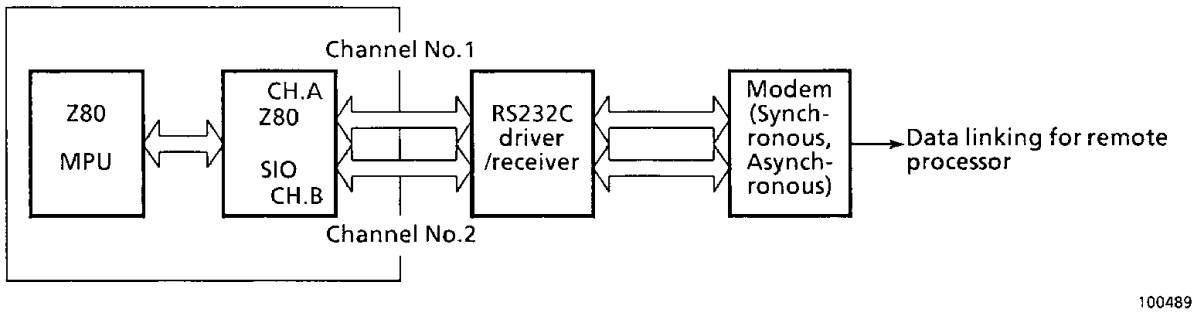

Figure 3.13 (b) Example of Data Communication between Processors

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
V_{CC}	Supply Voltage		0.5 to +7.0	V
V_{IN}	Input Voltage		−0.5 to VCC + 0.5	V
PD	Power Dissipation (6MHz VERSION : TA = 85°C) (8MHz VERSION : TA = 70°C)		250	mW
TSOLDER	Soldering Temperature (10 sec)		260	°C
TSTG	Storage Temperature		−65 to 150	°C
TOPR	Operating Temperature	6MHz VERSION	−40 to 85	°C
		8MHz VERSION	−10 to 70	

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4.2 DC ELECTRICAL CHARACTERISTICS

6MHz VERSION : $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$
8MHz VERSION : $T_A = -10°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

SYMBOL	ITEM	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage			−0.3	—	0.6	V
VIHC	High Clock Input Voltage			Vcc − 0.6	—	VCC + 0.3	V
VIL	Input Low Voltage (Except CLK)			−0.5	—	0.8	V
VIH	Input High Voltage (Except CLK)			2.2	—	VCC	V
VOL	Output Low Voltage	IOL = 2.0mA		—	—	0.4	V
VOH1	Output High Voltage (I)	IOH = −1.6mA		2.4	—	—	V
VOH2	Output High Voltage (II)	IOH = −250μA		Vcc − 0.8	—	—	V
ILI	Input Leakage Current	VSS ≦ VIN ≦ VCC		—	—	±10	μA
ILO	Output Leakage Current	VSS + 0.4 ≦ VOUT ≦ VCC		—	—	±10	μA
IL (SY)	$\overline{SYNC}$ Pin Leakage Current	VSS + 0.4 ≦ VIN ≦ VCC		−40	—	10	μA
ICC1	Power Supply Current	VCC = 5V fCLOK = (1) VIHC = VIH = VCC − 0.2V VILC = VIL = 0.2V	(2)	—	4	10	mA
			(3)	—	5	12	
ICC2	Standby Supply Current Except SYNC at "L" output	VCC = 5V VIH = VIHC = VCC − 0.2V VIL = VILC = 0.2V		—	—	10	μA

Note : (1) fCLK = 1/TcC (MIN.), (2) AP-6/AM-6/AF-6/AT-6, (3) AP-8

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4.3 AC ELECTRICAL CHARACTERISTICS (1/2)

6MHz VERSION : $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

8MHz VERSION : $T_A = -10°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

(1/2)

NO.	SYMBOL	PARAMETER	(1) (6MHZ)		(2) (8MHZ)		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	165	DC	125	DC	ns
2	TwCH	Clock pulse width (High)	70	DC	50	DC	ns
3	TfC	Clock fall time	—	15	—	15	ns
4	TrC	Clock rise time	—	15	—	15	ns
5	TwCl	Clock pulse width (Low)	70	DC	50	DC	ns
6	TsCS (C)	Control signal to clock setup time ($\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$)	60	—	60	—	ns
7	TsRD (C)	$\overline{IORQ}\downarrow$, $\overline{RD}\downarrow$ to clock $\uparrow$ setup time	60	—	55	—	ns
8	TdC (DO)	Clock $\uparrow$ to data out delay	—	150	—	100	ns
9	TsDI (C)	Data in to clock $\uparrow$ setup (Write or $\overline{M1}$ cycle)	30	—	30	—	ns
10	TdRD (DOz)	$\overline{RD}\uparrow$ to data out float delay	—	90	—	70	ns
11	TdIO (DOI)	$\overline{IORQ}\downarrow$ to data out delay (INTACK cycle)	—	120	—	85	ns
12	TsM1 (C)	$\overline{M1}$ to clock $\uparrow$ setup time	75	—	50	—	ns
13	TsIEI (IO)	IEI $\downarrow$ to $\overline{IORQ}\downarrow$ setup time (INTACK cycle)	120	—	80	—	ns
14	TdM1 (IEO)	$\overline{M1}\downarrow$ to IEO $\downarrow$ delay (interrupt before $\overline{M1}$)	—	160	—	120	ns
15	TdIEI (IEOr)	IEI $\uparrow$ to IEO $\uparrow$ delay (after ED decode)	—	110	—	110	ns
16	TdIEI (IEOf)	IEI $\downarrow$ to IEO $\downarrow$ delay	—	70	—	70	ns
17	TdC (INT)	Clock $\uparrow$ to $\overline{INT}\downarrow$ delay	—	150	—	100	ns
18	TdIO (W / RWf)	$\overline{IORQ}\downarrow$ or $\overline{CE}\downarrow$ to $\overline{W/RDY}\downarrow$ delay (Wait mode)	—	175	—	130	ns
19	TdC (W / RRf)	Clock $\uparrow$ to $\overline{W/RDY}\downarrow$ delay (Ready mode)	—	100	—	80	ns
20	TdC (W / RWZ)	Clock $\downarrow$ to $\overline{W/RDY}$ float delay (Wait mode)	—	110	—	90	ns
21	Th, Th (CS)	Any unspecified hold when setup is specified	0	—	0	—	ns
22	TwPh	Pulse width (High)	200	—	200	—	ns

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AC ELECTRICAL CHARACTERISTICS (2/2)

NO.	SYMBOL	PARAMETER	(1) (6MHZ)		(2) (8MHZ)		UNIT
			MIN.	MAX.	MIN.	MAX.	
23	TwPI	Pulse width (Low)	200	—	200	—	ns
24	TcTxC	$\overline{TxC}$ cycle time	330	∞	250	∞	ns
25	TwTxCl	$\overline{TxC}$ width (Low)	100	∞	80	∞	ns
26	TwTxCh	$\overline{TxC}$ width (High)	100	∞	80	∞	ns
27	TdTxC (TxD)	$\overline{TxC}\downarrow$ to TxD delay (x1 mode)	—	220	—	180	ns
28	TdTxC (W/RRf)	$\overline{TxC}\downarrow$ to $\overline{W/RDY}\downarrow$ delay (Ready mode)	5	9	5	9	CLK Periods*
29	TdTxC (INT)	$\overline{TxC}\downarrow$ to $\overline{INT}\downarrow$ delay	5	9	5	9	CLK Periods*
30	TcRxC	$\overline{RxC}$ cycle time	330	∞	250	∞	ns
31	TwRxCl	$\overline{RxC}$ width (Low)	100	∞	80	∞	ns
32	TwRxCh	$\overline{RxC}$ width (High)	100	∞	80	∞	ns
33	TsRxD (RxC)	RxD to $\overline{RxC}\uparrow$ setup time (x1 mode)	0	—	0	—	ns
34	ThRxD (RxC)	$\overline{RxC}\uparrow$ to RxD hold time (x1 mode)	100	—	80	—	ns
35	TdRxC (W/RRf)	$\overline{RxC}\uparrow$ to $\overline{W/RDY}\downarrow$ delay (Ready mode)	10	13	10	13	CLK Periods*
36	TdRxC (INT)	$\overline{RxC}\uparrow$ to $\overline{INT}\downarrow$ delay	10	13	10	13	CLK Periods*
37	TdRxC (SYNC)	$\overline{RxC}\uparrow$ to $\overline{SYNC}\downarrow$ delay (Output modes)	4	7	4	7	CLK Periods*
38	TsSYNC (RxC)	$\overline{SYNC}\downarrow$ to $\overline{RxC}\uparrow$ setup (External sync modes)	− 100	—	− 100	—	ns

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Note : (1) AP-6/AM-6/AF-6/AT-6, (2) AP-8

AC test condition

VIH = 2.4V, VIHC = VCC-0.6V, VIL = 0.4V, VILC = 0.6V

VOH = 2.2V, VOL = 0.8V CL = 100pF

* System Clock

In all modes, the System Clock rate must be at least five times the maximum data rate.

4.4 CAPACITANCE

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f = 1MHz	—	—	7	pF
CIN	Input Capacitance	All terminals except that to be measured should be earthed.	—	—	5	pF
COUT	Output Capacitance		—	—	10	pF

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4.5 TIMING DIAGRAM

Numbers shown in the following figures correspond with those in the 4.3 A.C. Electrical Characteristics Table.

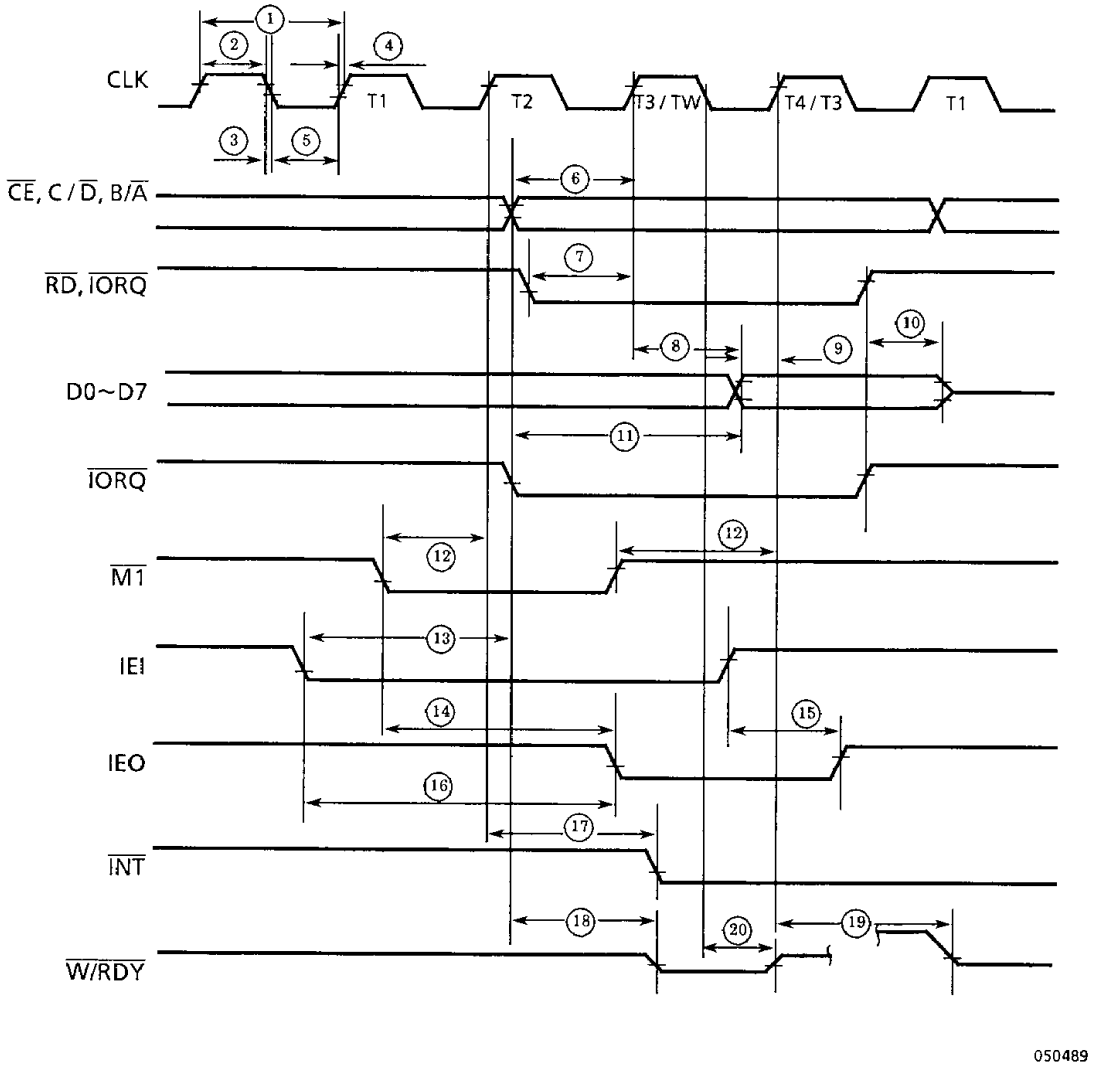


Figure 4.1 (a) Timing Diagram

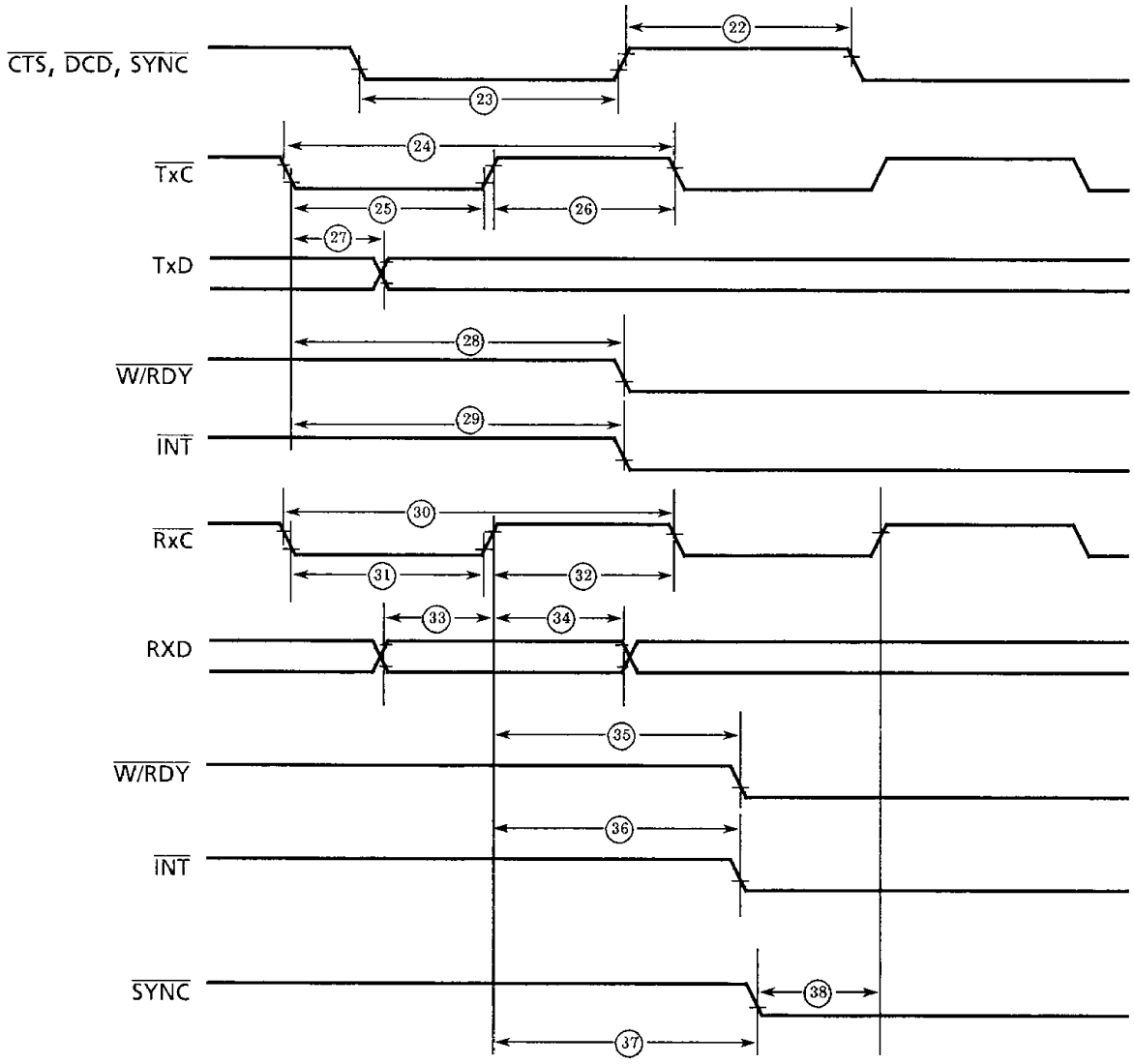


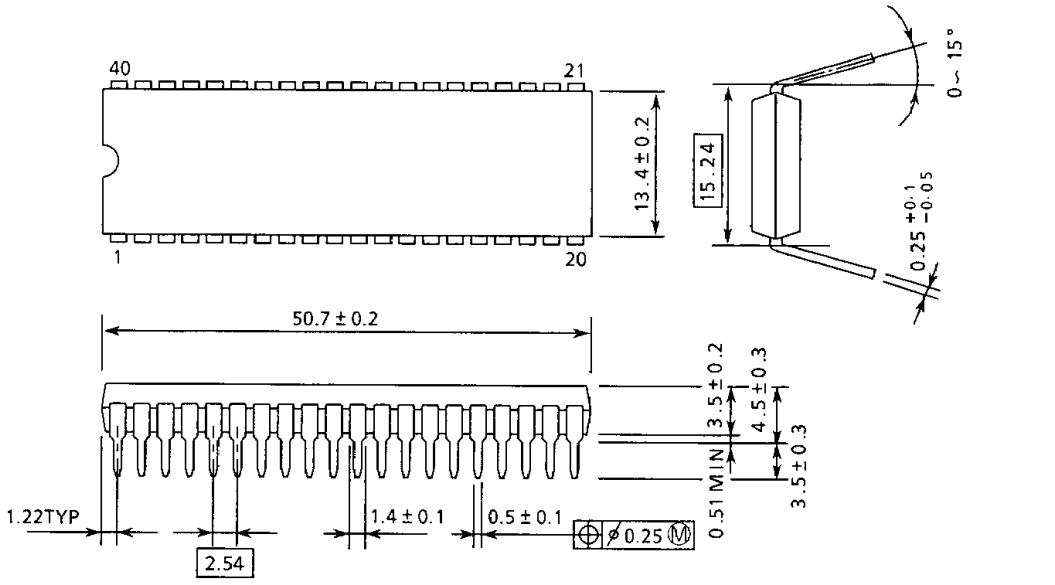
Figure 4.1 (b) Timing Diagram

5. PACKAGE DESCRIPTION

5.1 40-PIN DIP

DIP40-P-600

Unit : mm



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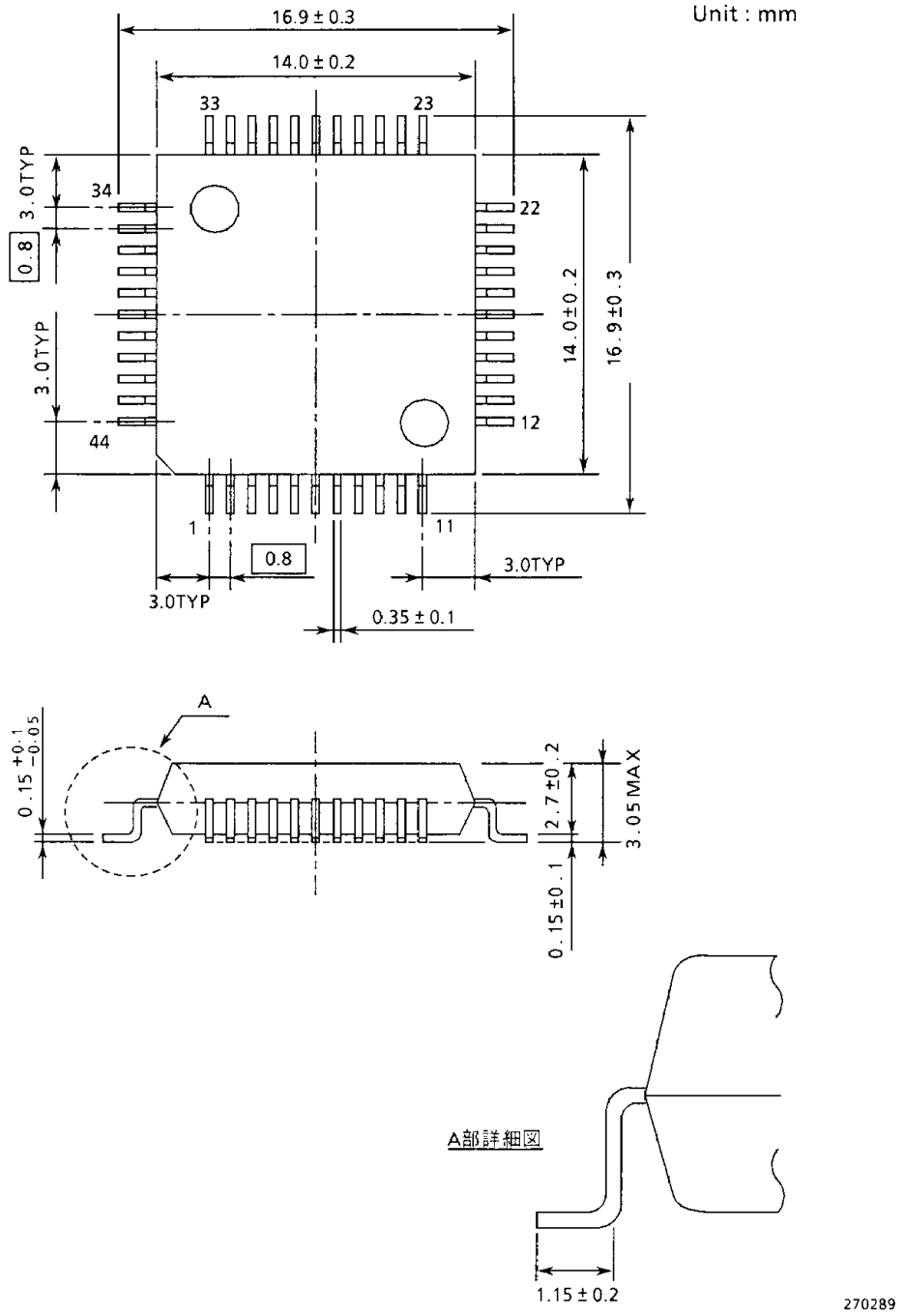
Note 1 : This dimension is measured at the center of bending point of leads.

Note 2 : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

5.2 44-PIN MINI-FLAT PACKAGE

QFP44-P-1414F

Unit : mm

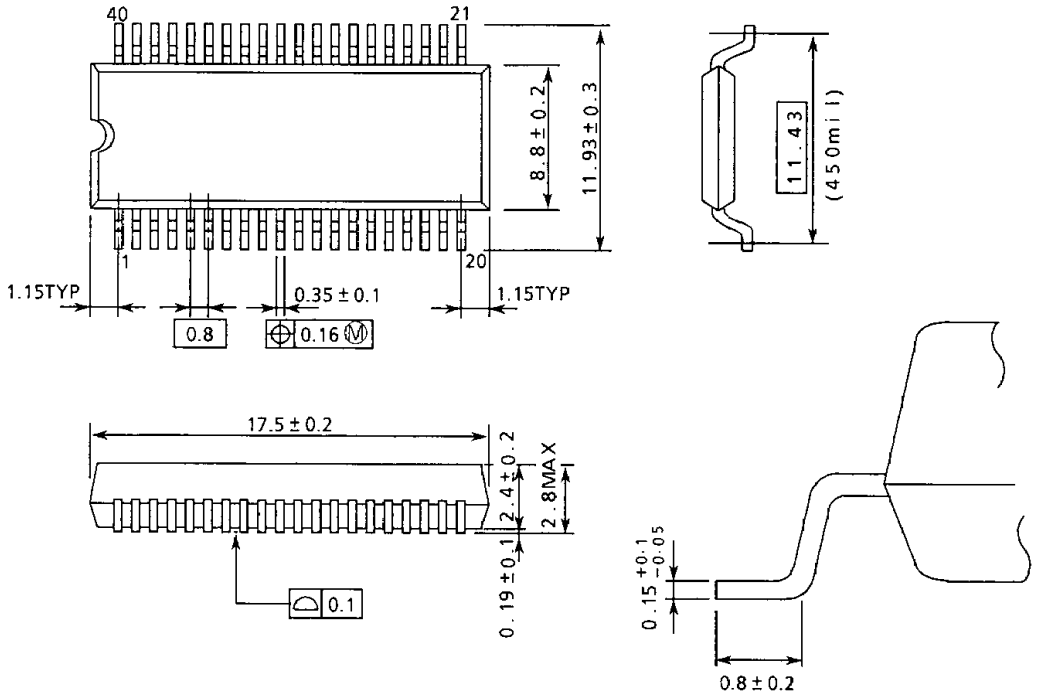


Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

5.3 SOP PACKAGE

SSOP40-P-450

Unit : mm



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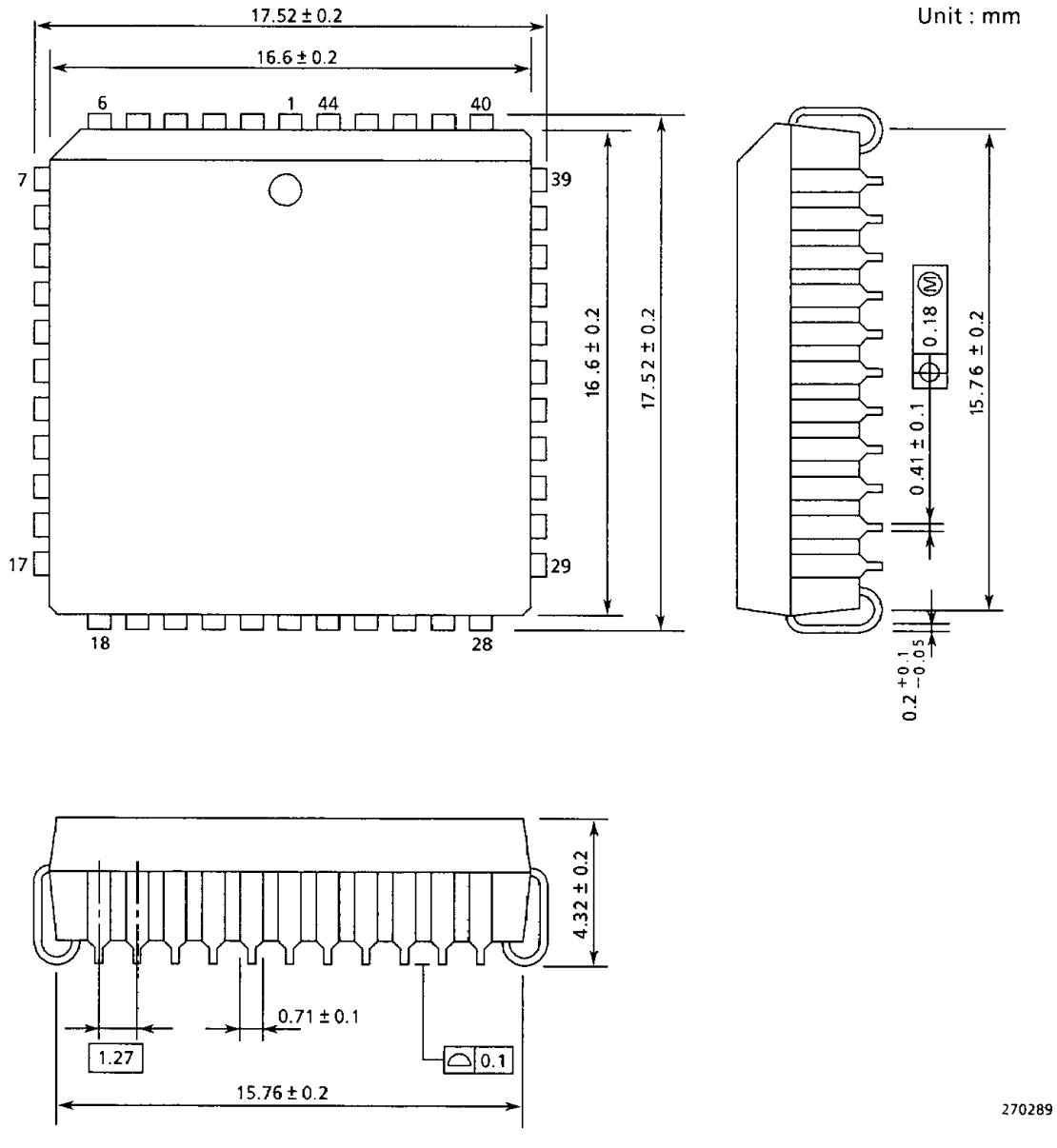
Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

5.4 44-PIN PLCC PACKAGE

QFJ44-P-S650

Unit : mm



6. PRECAUTIONS

In the programming using the SIO, it can be used only for single channel according to registers and bits.