TP07L

Low Threshold

Objective

T-39-17

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
-20V	3.0Ω	-0.35A	-1.3V	TP0702N3	TP0702ND

† MIL visual screening available

Features

- Low threshold —1.0V max
- On resistance guaranteed at V_{GS} = 2, 3, and 5 volts
- High input impedance
- Low input capacitance —130 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interface
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

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Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.35A	-0.40A	1W	125	170	-.035A	0.75A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-20			V	V_{GS} = 0, I_D = -1mA
$V_{GS(th)}$	Gate Threshold Voltage	-0.7		-1.3	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-100	nA	V_{DS} = 20V, V_{GS} = 0V
				-100	µA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-0.35			A	V_{GS} = V_{DS} = 5V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10.0	Ω	V_{GS} = 2V, I_D = -30mA
				5.0		V_{GS} = 3V, I_D = -120mA
				3.0		V_{GS} = 5V, I_D = -250mA
G_{FS}	Forward Transconductance	80			m℧	V_{DS} = 5V, I_D = -250mA
C_{ISS}	Input Capacitance		130	200	pF	V_{GS} = 0V, V_{DS} = -20V, f = 1MHz
C_{OSS}	Common Source Output Capacitance		70	125		
C_{RSS}	Reverse Transfer Capacitance		30	60		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 20V, I_D = -250mA, R_S = 50Ω
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			-1.0	V	V_{GS} = 0V, I_{SD} = -250mA

Notes:
1. All D C parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300 µs pulse, 2% duty cycle.)
2. All A.C parameters sample tested.

Switching Waveforms and Test Circuit