

TPS2070, TPS2071 FOUR-PORT USB HUB POWER CONTROLLERS

SLVS287A – SEPTEMBER 2000 – REVISED FEBRUARY 2001

- Complete USB Hub Power Solution
- Meets USB Specifications 1.1 and 2.0
- Independent Thermal and Short-Circuit Protection
- 3.3-V Regulator for USB Hub Controller
- Overcurrent Logic Outputs
- 4.5-V to 5.5-V Operating Range
- CMOS- and TTL-Compatible Enable Inputs
- 185 μ A Bus-Power Supply Current
- Available in 32-Pin HTSSOP PowerPAD™
- -40°C to 85°C Ambient Temperature Range

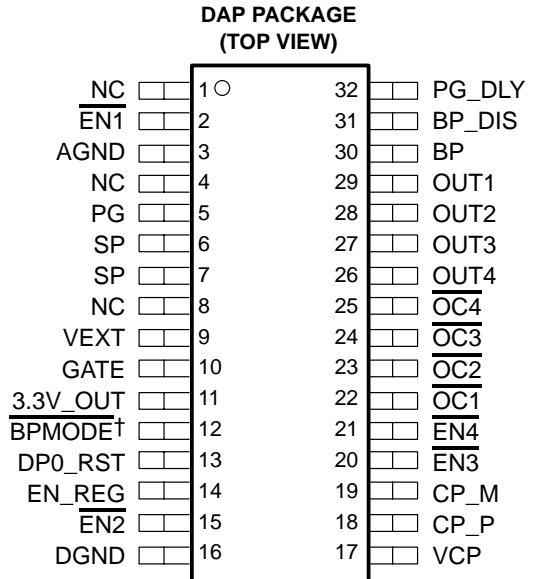
description

The TPS2070 and TPS2071 provide a complete USB hub power solution by incorporating four major functions: current-limited power switches for four ports, a 3.3-V 100-mA regulator, a 5-V regulator controller for self power, and a DP0 line control to signal attach/detach of the hub.

These devices are designed to meet bus-powered and self-powered hub requirements. These devices are also designed for hybrid hub implementations and allow for automatic switching from self-powered mode to bus-powered mode if loss of self-power is experienced (can be disabled by applying a logic high to BP_DIS).

Each port has a current-limited 107-m Ω N-channel MOSFET high-side power switch for 500 mA self-powered operation. Each port also has a current-limited 560-m Ω N-channel MOSFET high-side power switch for 100-mA bus-powered operation. All the N-channel MOSFETs are designed without parasitic diodes, preventing current backflow into the inputs.

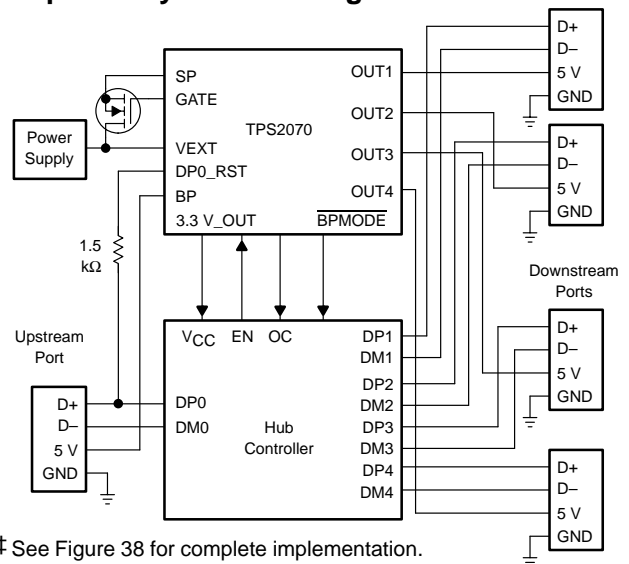
For applications not requiring a 5-V regulator controller, use the TPS2074 or TPS2075 device.



NC – No internal connection

† Pin 12 is active low (BPMODE) for TPS2070 and active high (BPMODE) for TPS2071.

simplified hybrid-hub diagram†



† See Figure 38 for complete implementation.

SELECTION GUIDE

| T _A | USB HUB POWER CONTROLLERS | PACKAGED DEVICES | | | |
|---|---|------------------|-------------|---------------|-----------|
| | | PIN COUNT | BPMODE | HTSSOP (DAP)† | SSOP (DB) |
| -40°C to 85°C | Four-port with internal LDO controller | 32 | Active low | TPS2070DAP | — |
| | | 32 | Active high | TPS2071DAP | — |
| | Four-port without internal LDO controller | 24 | Active low | — | TPS2074DB |
| | | 24 | Active high | — | TPS2075DB |

† The DAP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2070DAPR).



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**TEXAS
INSTRUMENTS**

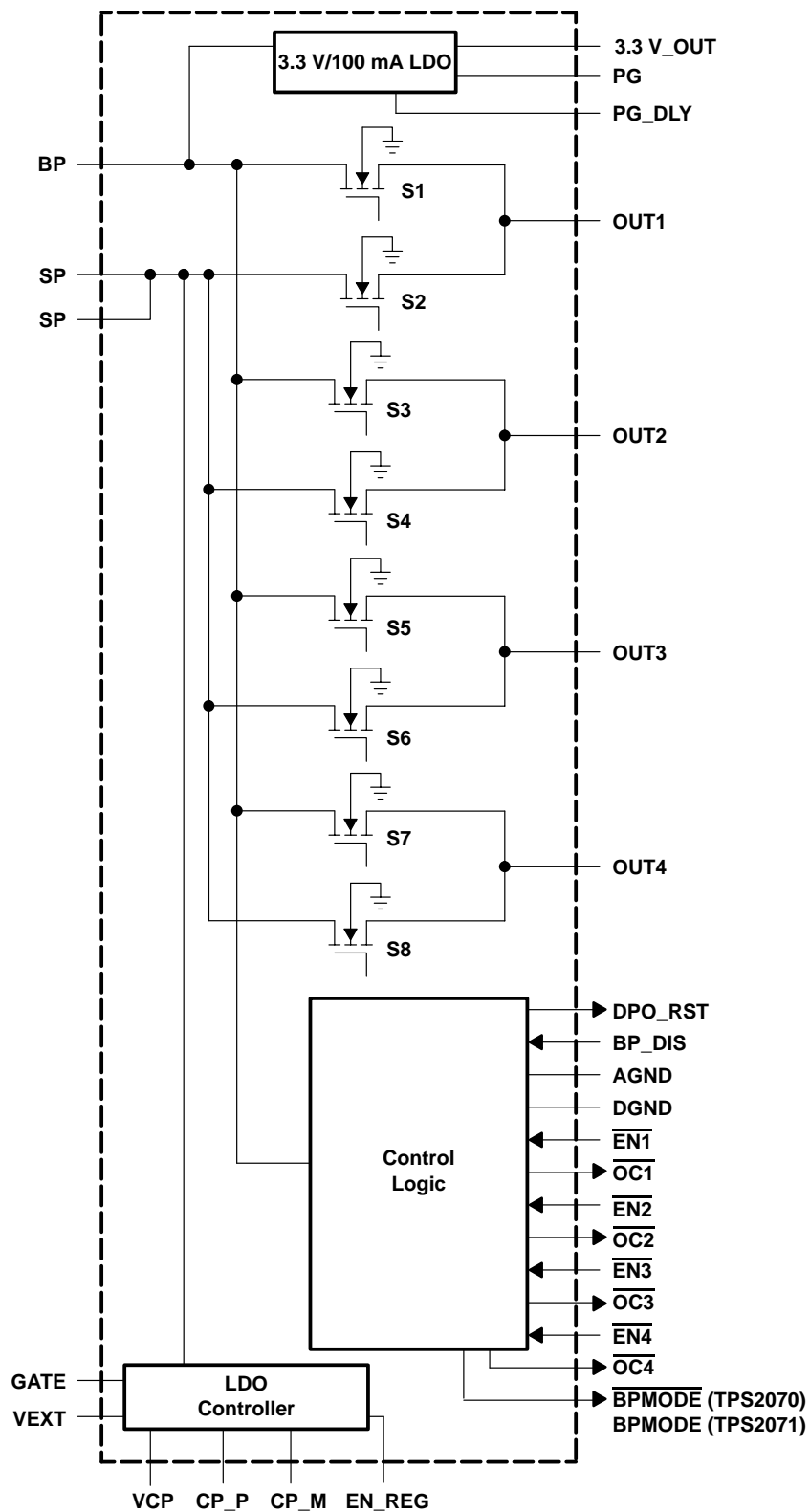
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functional block diagram



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Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|------------------------------------|-----|-----|---|
| NAME | NO. | | |
| NC | 1 | | No internal connection |
| $\overline{\text{EN1}}$ | 2 | I | Active-low enable for OUT1 |
| AGND | 3 | | Analog ground |
| NC | 4 | | No internal connection |
| PG | 5 | O | Logic output, power good |
| SP | 6 | I | Self-power voltage input, connects to local power supply |
| SP | 7 | I | Self-power voltage input, connects to local power supply |
| NC | 8 | | No internal connection |
| VEXT | 9 | I | Input voltage for the external voltage regulator |
| GATE | 10 | O | Output gate drive for an external N-channel MOSFET |
| 3.3V_OUT | 11 | O | 3.3-V internal voltage regulator output |
| $\overline{\text{BPMODE}}^\dagger$ | 12 | O | A logic signal that indicates if the outputs source from the bus-powered supply. $\overline{\text{BPMODE}}$ (TPS2070) or $\overline{\text{BPMODE}}$ (TPS2071) can be used to signal hub controller. |
| DP0_RST | 13 | O | Connects to DP signal from upstream hub/host through an external 1.5-k Ω resistor |
| EN_REG | 14 | I | Active-high enable, enables external voltage regulator. Connect to BP or GND |
| $\overline{\text{EN2}}$ | 15 | I | Active-low enable for OUT2 |
| DGND | 16 | | Digital ground |
| VCP | 17 | | Charge-pump output, source for an external voltage-regulator driver. Recommend 0.1- μF capacitor to DGND. |
| CP_P | 18 | | Charge-pump-capacitor connection from CP_M. Recommend 0.01- μF between CP_P and CP_M. |
| CP_M | 19 | | Charge-pump-capacitor connection from CP_P. Recommend 0.01- μF between CP_P and CP_M. |
| $\overline{\text{EN3}}$ | 20 | I | Active-low enable for OUT3 |
| $\overline{\text{EN4}}$ | 21 | I | Active-low enable for OUT4 |
| $\overline{\text{OC1}}$ | 22 | O | Logic output, overcurrent response for OUT1 |
| $\overline{\text{OC2}}$ | 23 | O | Logic output, overcurrent response for OUT2 |
| $\overline{\text{OC3}}$ | 24 | O | Logic output, overcurrent response for OUT3 |
| $\overline{\text{OC4}}$ | 25 | O | Logic output, overcurrent response for OUT4 |
| OUT4 | 26 | O | Power switch output for downstream ports |
| OUT3 | 27 | O | Power switch output for downstream ports |
| OUT2 | 28 | O | Power switch output for downstream ports |
| OUT1 | 29 | O | Power switch output for downstream ports |
| BP | 30 | I | Bus power voltage input, connect to V_{BUS} |
| BP_DIS | 31 | I | Active-high logic input, disables autoswitch to bus power when self power is disconnected. Connect to BP or GND |
| PG_DLY ‡ | 32 | | Adjusts the PG time delay with a capacitor to ground. Adjust the pulsewidth to fit the application. |

† Pin 12 is active low for TPS2070 and active high for TPS2071.

‡ Use the following formula to calculate the capacitance needed; $C = (\text{desired pulsewidth} \times 3 \times 10^{-6})/1.22$



TPS2070, TPS2071

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detailed description

BP

The bus-powered supply input (BP) serves as the source for the internal 3.3-V LDO and for all logic functions in the device. In bus-powered mode, BP also serves as the source for all the outputs (OUTx). If BP is below the undervoltage threshold, all power switches will turn off and the LDO will be disabled. BP must be connected to a voltage source in order for the device to operate.

SP

The self-powered supply input (SP) serves as the source for all the outputs (OUTx) in self-powered mode. The enable logic for the SP switches requires that BP be connected to a voltage source.

OUT1, OUT2, OUT2, OUT4

OUTx are the outputs of the integrated power switches.

3.3V_OUT

The internal 3.3-V LDO output can be used to supply up to 100 mA current to low-power functions, such as hub controllers.

VEXT

VEXT is used to generate a 5-V source for the SP input by using the internal LDO controller and an external N-channel MOSFET. This pin connects to a 6-V to 9-V power supply and to the drain of the MOSFET if the external LDO is needed.

GATE

GATE is the output of the 5-V LDO controller and connects to the gate of the external MOSFET.

EN_REG

The active-high input, EN_REG, is used to enable the 5-V regulator controller. EN_REG is compatible with TTL and CMOS logic levels.

DP0_RST

DP0_RST functions as a hub reset when a 1.5-k Ω resistor is connected between DP0_RST and the upstream DP0 data line in a hub system. To provide a clean attach signal on DP0 data line, the DP0_RST output goes low momentarily (because of the upstream pulldown resistor) to discharge any parasitic charge on the cable, then goes to 3-state and finally outputs a high signal. The low and Hi-Z pulse widths are adjustable using a capacitor between PG_DLY and ground, and are approximately 50% of the power-good time delay. Detachment is signaled by a Hi-Z on DP0_RST. Both DP0_RST and PG will transition high at the same time.

Power Good (PG)

The power good (PG) function serves as a reset for a USB hub controller. PG is asserted low when the output voltage on the internal voltage regulator is below a fixed threshold. A time delay to ensure a stable output voltage before PG goes high is adjustable using a small-value ceramic capacitor from PG_DLY to ground.

PG_DLY

PG_DLY connects to an external capacitor to adjust the time delay for PG and DP0_RST. For USB applications, a 0.1- μ F capacitor is recommended, however, reference the USB Hub Controller data sheet to determine the needed pulsewidth criteria.



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detailed description (continued)

BP_DIS

BP_DIS is used to enable or disable the autoswitching function between bus-powered mode and self-powered mode. When BP_DIS is connected low and the voltage on SP is greater than the undervoltage-lockout (UVLO) threshold, the device will switch to self-powered operation automatically; if the SP voltage falls lower than the UVLO threshold, the device will switch to bus-powered operation. When BP_DIS is connected high, the autoswitching function is disabled and the device will not autoswitch to bus-powered operation if the SP voltage is below the UVLO threshold.

$\overline{\text{BPMODE}}$ or **BPMODE**

$\overline{\text{BPMODE}}$ (TPS2070) or **BPMODE** (TPS2071) is an output that signals when the device is in bus-powered mode. The logic state is set according to the voltages on BP, SP, and BP_DIS. For the TPS2070, $\overline{\text{BPMODE}}$ outputs a low signal to indicate bus-powered mode or a high signal to indicate self-powered mode. For the TPS2071, **BPMODE** outputs a high signal to indicate bus-powered mode or a low signal to indicate self-powered mode. This output can be used to inform a USB hub controller to configure for bus-powered mode or self-powered mode.

$\overline{\text{OC1}}$, $\overline{\text{OC2}}$, $\overline{\text{OC3}}$, $\overline{\text{OC4}}$

$\overline{\text{OCx}}$ is an output signal that is asserted (active low) when an overcurrent or overtemperature condition is encountered for the corresponding channel. $\overline{\text{OCx}}$ will remain asserted until the overcurrent or overtemperature condition is removed.

$\overline{\text{EN1}}$, $\overline{\text{EN2}}$, $\overline{\text{EN3}}$, $\overline{\text{EN4}}$,

The active-low logic input $\overline{\text{ENx}}$ enables or disables the power switches in the device. The enable input is compatible with both TTL and CMOS logic levels. The switches will not turn on until 3.3V_OUT is above the PG threshold.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|--|--|------------------------------------|
| Input voltage range: | $V_{I(\text{BP})}$, $V_{I(\text{SP})}$, $V_{I(\overline{\text{ENx}})}$, $V_{I(\text{EN_REG})}$, $V_{I(\text{BP_DIS})}$ | -0.3 V to 6 V |
| | $V_{I(\text{VEXT})}$ | -0.3 V to 10 V |
| Output voltage range: | $V_{O(\text{OUTx})}$ | -0.3 V to 6 V |
| | $V_{O(3.3V_OUT)}$, $V_{O(\text{PG_DLY})}$, $V_{O(\overline{\text{OCx}})}$, $V_{O(\overline{\text{BPMODE}})}$, $V_{O(\text{DP0_RST})}$, $V_{O(\text{PG})}$ | -0.3 V to $V_{O(3.3V_OUT)}$ 0.3 V |
| | $V_{O(\text{GATE})}$, $V_{O(\text{CP_M})}$, $V_{O(\text{CP_P})}$, $V_{O(\text{VCP})}$ | -0.3 V to 15 V |
| Continuous output current: | $I_{O(\text{OUTx})}$ | internally limited |
| | $I_{O(3.3V_OUT)}$ | internally limited |
| Maximum output current: | $I_{O(\text{VCP})}$ | ±30 mA |
| | $I_{O(\overline{\text{BPMODE}})}$ or $I_{O(\text{BPMODE})}$, $I_{O(\text{DP0_RST})}$, $I_{O(\text{PG})}$, $I_{O(\overline{\text{OCx}})}$ | ±10 mA |
| | $I_{O(\text{GATE})}$, sourcing | 700 μA |
| | $I_{O(\text{GATE})}$, sinking | -2.2 mA |
| Continuous total power dissipation | See Dissipation Rating Table | |
| Operating virtual junction temperature range, T_J | -40°C to 125°C | |
| Storage temperature range, T_{stg} | -65°C to 150°C | |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | 260°C | |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND.



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DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|---------------------------------------|
| 32-DAP | 1162.8 mW | 11.6 mW/°C | 639.5 mW | 465.1 mW |
| 32-DAP† | 4255.3 mW | 42.5 mW/°C | 2340.4 mW | 1702.1 mW |

† Using PowerPAD as heatsink.

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|-------------------------|-----|-----|------|
| Input voltage | V _{I(BP)} | 4.5 | 5.5 | V |
| | V _{I(SP)} | 0 | 5.5 | |
| | V _{I(VEXT)} | 0 | 9 | |
| | V _{I(BP_DIS)} | 0 | 5.5 | |
| | V _{I(ENx)} | 0 | 5.5 | |
| | V _{I(EN_REG)} | 0 | 5.5 | |
| Continuous output current, I _O | BP to OUTx (per switch) | | 100 | mA |
| | SP to OUTx (per switch) | | 500 | |
| | BP to 3.3V_OUT | | 100 | |
| Operating virtual junction temperature, T _J | | -40 | 125 | °C |

electrical characteristics over recommended operating junction temperature range,
 $4.5\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $4.85\text{ V} \leq V_{I(SP)} \leq 5.5\text{ V}$, $6\text{ V} \leq V_{I(VEXT)} \leq 9\text{ V}$, $\overline{ENx} = 0\text{ V}$, $EN_REG = 0\text{ V}$,
 $BP_DIS = 0\text{ V}$ (unless otherwise noted)

input current

| PARAMETER | | TEST CONDITIONS† | MIN | TYP | MAX | UNIT |
|----------------------|--|--|---------------------------|-----|-----|------|
| I _{I(BP)} | Input current at BP, switches disabled | No load on OUTx and 3.3V_OUT, ENx = V _{I(BP)} | V _{I(SP)} = Hi-Z | 185 | 240 | μA |
| | | | V _{I(SP)} = 0 V | 185 | 240 | |
| | | | V _{I(SP)} = 5 V | 175 | 210 | |
| I _{I(BP)} | Input current at BP, switches enabled | No load on OUTx and 3.3V_OUT, ENx = 0 V | V _{I(SP)} = Hi-Z | 185 | 240 | μA |
| | | | V _{I(SP)} = 0 V | 185 | 240 | |
| | | | V _{I(SP)} = 5 V | 175 | 210 | |
| I _{I(SP)} | Input current at SP, switches disabled | No load on OUTx and 3.3V_OUT, ENx = V _{I(SP)} | V _{I(BP)} = Hi-Z | 90 | 115 | μA |
| | | | V _{I(BP)} = 0 V | 90 | 115 | |
| | | | V _{I(BP)} = 5 V | 115 | 140 | |
| I _{I(SP)} | Input current at SP, switches enabled | No load on OUTx and 3.3V_OUT, ENx = 0 V | V _{I(BP)} = Hi-Z | 90 | 115 | μA |
| | | | V _{I(BP)} = 0 V | 90 | 115 | |
| | | | V _{I(BP)} = 5 V | 115 | 140 | |
| I _{I(VEXT)} | Input current at VEXT, LDO controller disabled | V _{I(EN_REG)} = 0 V or Hi-Z, V _{I(BP)} = 5 V, V _{I(SP)} = Hi-Z | | 200 | 360 | μA |
| | Input current, at VEXT, LDO controller enabled | V _{I(EN_REG)} = 5 V, V _{I(BP)} = 5 V, V _{I(SP)} = Hi-Z | | | 10 | mA |

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.



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**electrical characteristics over recommended operating junction temperature range,
4.5 V ≤ V_{I(BP)} ≤ 5.5 V, 4.85 V ≤ V_{I(SP)} ≤ 5.5 V, 6 V ≤ V_{I(VEXT)} ≤ 9 V, EN_x = 0 V, EN_REG = 0 V,
BP_DIS = 0 V (unless otherwise noted) (continued)**

power switches

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|-------------------------------------|---|--|---|-----------------------|------|-----|------|---|
| r _{DS(on)} | Static drain-source on-state resistance | SP to OUTx | V _{I(SP)} = V _{I(BP)} = 5 V, I _{Ox} = 0.5 A | T _A = 25°C | 107 | | mΩ | |
| | | | | T _A = 70°C | 125 | 160 | | |
| | BP to OUTx | V _{I(BP)} = 4.5 V, V _{I(SP)} = Open, I _{Ox} = 0.1 A | T _A = 25°C | 560 | | | | |
| | | | T _A = 70°C | 630 | 900 | | | |
| I _{lkg(OUTx)} | Leakage current at OUTx (no load on 3.3V_OUT) | | EN _x = V _{I(BP)} = 5.5 V, V _{I(SP)} = Hi-Z, OUTx connected to ground, V _{I(VIN)} = Hi-Z | T _J = 25°C | 0.5 | 10 | μA | |
| | | | EN _x = V _{I(BP)} = V _{I(SP)} = 5.5 V, OUTx connected to ground, V _{I(EXT)} = Hi-Z | T _J = 25°C | 0.5 | 10 | | |
| | | | EN _x = V _{I(BP)} = Hi-Z or 0 V, V _{I(VEXT)} = V _{I(SP)} = V _{I(OUTx)} = 5.5 V | T _J = 25°C | 0.5 | 10 | | |
| | | | EN _x = V _{I(BP)} = V _{I(SP)} = Hi-Z or 0 V, V _{I(VEXT)} = V _{I(OUTx)} = 5.5 V | T _J = 25°C | 0.5 | 10 | | |
| | | | EN _x = V _{I(BP)} = V _{I(SP)} = V _{I(VEXT)} = Hi-Z or 0 V, V _{I(OUTx)} = 5.5 V | T _J = 25°C | 0.5 | 10 | | |
| Short-circuit current (per output)† | | | V _{I(BP)} = V _{I(SP)} = 5 V, OUTx connected to GND, Device enabled into short circuit | | 0.6 | 0.9 | 1.2 | A |
| | | | V _{I(BP)} = 5 V, V _{I(SP)} = open, OUTx connected to GND, device enabled into short circuit | | 0.12 | 0.2 | 0.3 | |

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

input signals (EN_x, EN_REG, BP_DIS)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-----------------|------------------------------|--------------------------------------|-----|-----|------|
| V _{IH} | High-level input voltage | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | | 0.8 | |
| I _I | Input current | Pullup | EN _x (active low) | V _{I(EN_x)} = 0 V | | 5 | μA |
| | | Pulldown | EN_REG (active high) | V _{I(EN_REG)} = 5 V | | 5 | |
| | | | BP_DIS (active high) | V _{I(BP_DIS)} = 5 V | | 5 | |



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electrical characteristics over recommended operating junction temperature range,
 $4.5\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $4.85\text{ V} \leq V_{I(SP)} \leq 5.5\text{ V}$, $6\text{ V} \leq V_{I(VEXT)} \leq 9\text{ V}$, $\overline{EN}_x = 0\text{ V}$, $EN_REG = 0\text{ V}$,
 $BP_DIS = 0\text{ V}$ (unless otherwise noted) (continued)

output signals (BPMODE or \overline{BPMODE} , \overline{OC}_x , DPO_RST)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------|--|---------------------|--|-------------------------|-----------------------------|-----|------|
| V _{OH} | High-level output voltage | \overline{BPMODE} | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{I(SP)} \leq 5.5\text{ V}$ | I _O = 2 mA | | 2.4 | V |
| | | BPMODE | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $V_{I(SP)} < 4\text{ V}$ | | | 2.4 | |
| | | \overline{OC}_x | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $V_{I(EN_x)} = 3.3\text{ V}$ or Hi-Z | | | 2.4 | |
| | | DPO_RST | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $V_{I(PG_DLY)} = 3.3\text{ V}$ | | | 2.4 | |
| V _{OL} | Low-level output voltage | \overline{BPMODE} | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $V_{I(SP)} < 4\text{ V}$ | I _O = 3.2 mA | | 0.4 | V |
| | | BPMODE | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{I(SP)} \leq 5.5\text{ V}$ | | | 0.4 | |
| | | \overline{OC}_x | $4.25\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $OUT_x = 0\text{ V}$ | | I _{O(OC)} = 3.2 mA | | |
| V _{I(BP)} | Minimum input voltage at BP for low-level output | | I _O = 300 μA, V _{O(BPMODE)} ≤ 0.4 V | | | 1.5 | V |
| | | | I _O = 300 μA, V _{O(BPMODE)} ≤ 0.4 V, V _{I(SP)} = 5 V | | | 1.5 | |
| I _{lkg} | Hi-Z leakage current at DPO_RST | | $0\text{ V} \leq V_{I(DPO_RST)} \leq 3.3\text{ V}$, V _{I(SP)} = 0 V, V _{I(BP)} = 5.5 V, V _{I(PG_DLY)} = 0.9 V | | -5 | 5 | μA |
| t _d | Overcurrent response delay time (see Note 1) | | | | 1 | 10 | ms |

NOTE 1: Specified by design, not tested in production.

undervoltage lockout (SP, BP, VEXT)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------|---------------------------|------|-----|------|------|
| Start threshold | SP | | | | 4.5 | V |
| | BP | V _{I(SP)} = Hi-Z | | | 4.25 | |
| | VEXT | | | | 3 | |
| Stop threshold | SP | | 4 | | | V |
| | BP | | 3.75 | | | |
| | VEXT | | 2.50 | | | |
| V _{hys} | Hysteresis voltage (see Note 1) | SP | | | 300 | mV |
| | | BP | | | 300 | |
| | | VEXT | | | 150 | |

NOTE 1: Specified by design, not tested in production.



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**electrical characteristics over recommended operating junction temperature range,
 $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$, $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$, $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$, $\overline{\text{ENx}} = 0\text{ V}$, $\overline{\text{EN_REG}} = 0\text{ V}$,
 $\text{BP_DIS} = 0\text{ V}$, $C_{L(3.3\text{V_OUT})} = 10\text{ }\mu\text{F}$ (unless otherwise noted)**

internal voltage regulator

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|------|------|------|---------------|
| V_O | Output voltage, dc | $V_{I(\text{BP})} = 4.25\text{ V to } 5.5\text{ V}$, $I_O = 5\text{ mA to } 100\text{ mA}$ | 3.2 | 3.3 | 3.4 | V |
| | Dropout voltage | $I_O = 100\text{ mA}$ | | 0.6 | | V |
| | Line regulation | $V_{I(\text{BP})} = 4.25\text{ V to } 5.25\text{ V}$, $I_O = 5\text{ mA}$ | | | 0.1 | %/v |
| | Load regulation | $V_{I(\text{BP})} = 4.25\text{ V}$, $I_O = 5\text{ mA to } 100\text{ mA}$ | | | 0.6% | |
| I_{OS} | Short-circuit current limit† | $V_{I(\text{BP})} = 4.25\text{ V}$, 3.3V_OUT connected to GND | 0.12 | 0.2 | 0.3 | A |
| | Pulldown transistor at 3.3V_OUTPUT (see Note 1) | $V_{I(3.3\text{V_OUT})} = 3.3\text{ V}$ | 10 | | | mA |
| | | $V_{I(3.3\text{V_OUT})} = 1\text{ V}$ | 5 | | | |
| PSRR | Power-supply ripple rejection (see Note 1) | $F = 1\text{ kHz}$, $C_{L(3.3\text{V_OUT})} = 4.7\text{ }\mu\text{F}$, $\text{ESR} = 0.25\text{ }\Omega$, $I_O = 5\text{ mA}$, $V_{I(\text{BP})\text{PP}} = 100\text{ mV}$ | 40 | | | dB |
| | Low-level trip threshold voltage at PG | | 2.88 | 2.94 | 3 | V |
| V_{hys} | Hysteresis voltage at PG (see Note 1) | | 50 | | 100 | mV |
| V_{OH} | High-level output voltage at PG | $4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.25\text{ V}$, $I_O = 2\text{ mA}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage at PG | $4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.25\text{ V}$, $I_O = 3.2\text{ mA}$ | | | 0.4 | V |
| V_{ref} | Reference voltage at PG_DLY | | | 1.22 | | V |
| | Charge current at PG_DLY | | | 3 | | μA |
| t_d | Delay time at PG (see Notes 1 and 2) | $C_{L(\text{PG_DLY})} = 0.47\text{ }\mu\text{F}$ | | 190 | | ms |

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTES: 1. Specified by design, not tested in production.

2. The PG delay time (t_d) is calculated using the PG_DLY reference voltage and charge current:

$$t_d = \frac{C_{L(\text{PG_DLY})} \times V_{\text{ref}}}{\text{Charge Current}}$$

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**electrical characteristics over recommended operating junction temperature range,
 $4.5\text{ V} \leq V_{I(BP)} \leq 5.5\text{ V}$, $4.85\text{ V} \leq V_{I(SP)} \leq 5.5\text{ V}$, $6\text{ V} \leq V_{I(VEXT)} \leq 9\text{ V}$, $\overline{EN}_x = 0\text{ V}$, $EN_REG = 3.3\text{ V}$,
 $BP_DIS = 0\text{ V}$, $C_{L(SP)} = 220\text{ }\mu\text{F}$ (unless otherwise noted)**

voltage regulator controller

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------------------------|---|------|-----|------|---------------|
| $V_{O(CP)}$ | Output voltage, charge pump | $V_{I(VEXT)} = 6\text{ V}$, $I_{O(VCP)} = 5\text{ mA}$ $C_{(CP_P)} = 10\text{ nF}$, $C_{(VCP)} = 100\text{ nF}$ | 10 | | | V |
| f_{osc} | Oscillator frequency (see Note 1) | $6\text{ V} \leq V_{I(VEXT)} \leq 9\text{ V}$, $I_{O(VCP)} = 5\text{ mA}$, $V_{O(VCP)} = 10\text{ V}$ | | 850 | | kHz |
| Gate drive current | Sourcing | $V_{I(VCP)} = 9\text{ V}$, $V_{O(GATE)} = 7.5\text{ V}$, $V_{I(SP)} = 4.5\text{ V}$ | 500 | | | μA |
| | Sinking | $V_{I(VCP)} = 9\text{ V}$, $V_{O(GATE)} = 5.5\text{ V}$, $V_{I(SP)} = 5.5\text{ V}$ | 1.5 | | | mA |
| Open-loop gain (see Note 1) | | $V_{I(VEXT)} = 6\text{ V}$, $0.5\text{ V} \leq V_{O(GATE)} \leq 9\text{ V}$ | | 80 | | dB |
| Reference voltage at $V_{I(SP)}$, using external regulator | | $V_{I(VEXT)} = 6\text{ V to }9\text{ V}$, IRLZ24N FET | 4.90 | 5.1 | 5.25 | V |
| Gate clamp voltage | | Gate to SP | | 10 | | V |

NOTE 1: Specified by design, not tested in production.

power switch timing requirements

| PARAMETER | | TEST CONDITION [†] | MIN | TYP | MAX | UNIT |
|-----------|---|---|-----|-----|-----|------|
| t_{on} | Turnon time (see Note 1) | BP to OUTx switch $V_{I(BP)} = 5\text{ V}$, $V_{I(SP)} = \text{open}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 50\text{ }\Omega$ | | 4.5 | | ms |
| | SP to OUTx switch $V_{I(SP)} = V_{I(BP)} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | 4.5 | | | |
| t_{off} | Turnoff time (see Note 1) | BP to OUTx switch $V_{I(BP)} = 5\text{ V}$, $V_{I(SP)} = \text{open}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 50\text{ }\Omega$ | | 15 | | ms |
| | SP to OUTx switch $V_{I(SP)} = V_{I(BP)} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | 10 | | | |
| t_r | Rise time, output (see Note 1) | BP to OUTx switch $V_{I(BP)} = 5\text{ V}$, $V_{I(SP)} = \text{open}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 50\text{ }\Omega$ | | 4 | | ms |
| | SP to OUTx switch $V_{I(SP)} = V_{I(BP)} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | 3 | | | |
| t_f | Fall time, output (see Note 1) | BP to OUTx switch $V_{I(BP)} = 5\text{ V}$, $V_{I(SP)} = \text{open}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 50\text{ }\Omega$ | | 10 | | ms |
| | SP to OUTx switch $V_{I(SP)} = V_{I(BP)} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | 3 | | | |

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTE 1. Specified by design, not tested in production.

thermal shutdown

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------|------------------|-------|-----|-----|------------------|
| T_J | Thermal shutdown | First | 140 | | $^\circ\text{C}$ |
| | Second | | 150 | | |
| Hysteresis | First | | 15 | | $^\circ\text{C}$ |
| | Second | | 25 | | |



PARAMETER MEASUREMENT INFORMATION

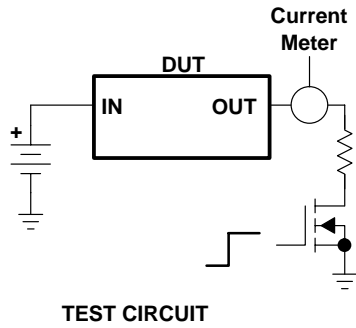
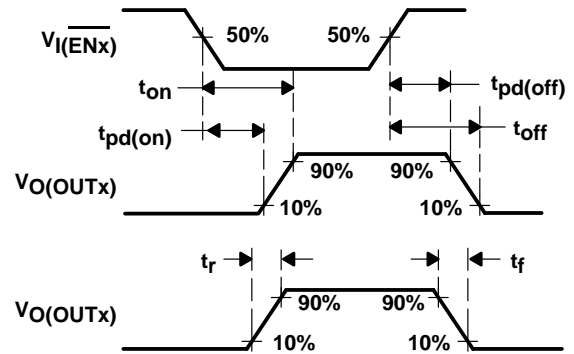


Figure 1. Current Limit Response



TIMING

Figure 2. Timing and Internal Voltage Regulator Transition Waveforms

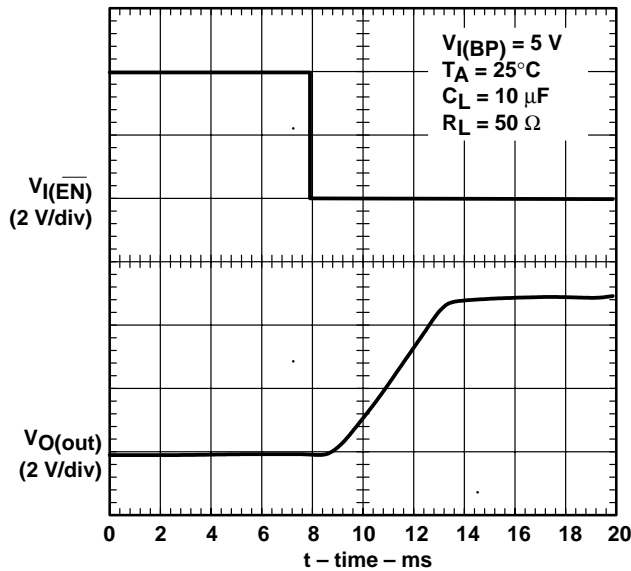


Figure 3. Turnon Delay and Rise Time (BP Switch)

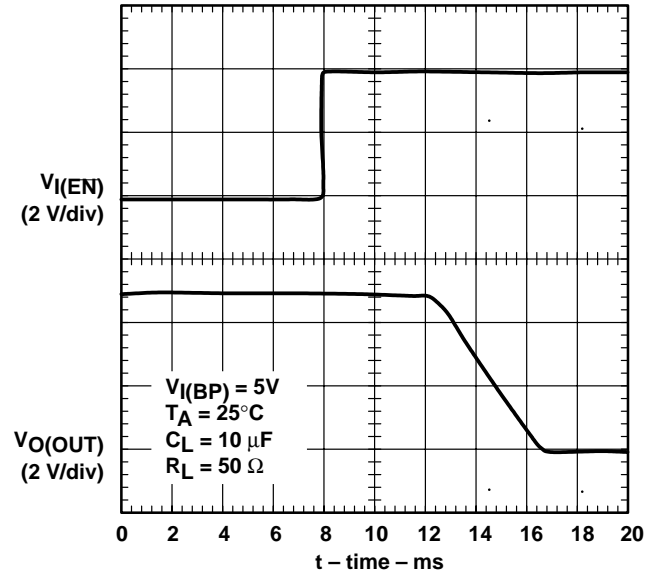


Figure 4. Turnoff Delay and Fall Time (BP Switch)

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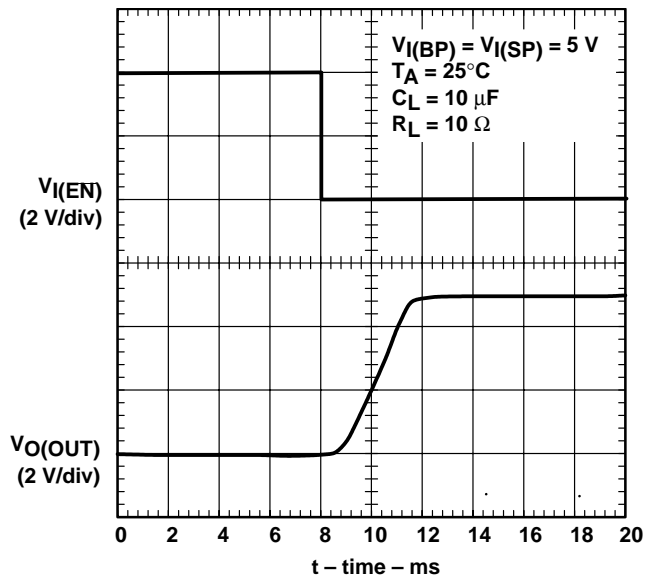


Figure 5. Turnon Delay and Rise Time (SP Switch)

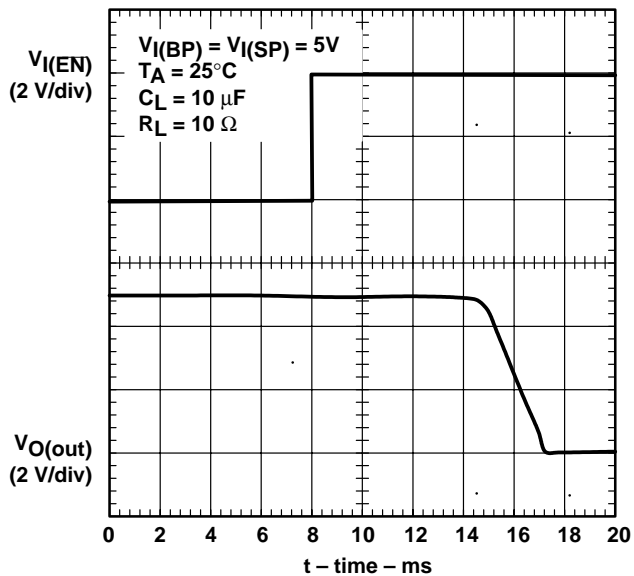


Figure 6. Turnoff Delay and Fall Time (SP Switch)

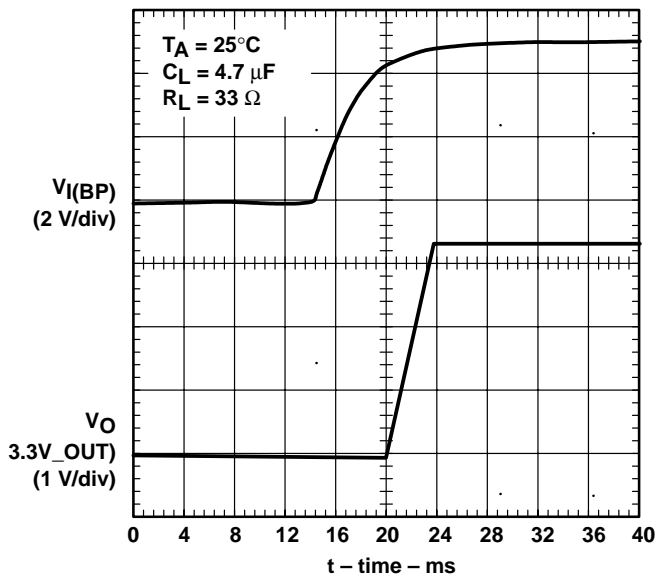


Figure 7. Turnon Delay and Rise Time (3.3V_OUT)

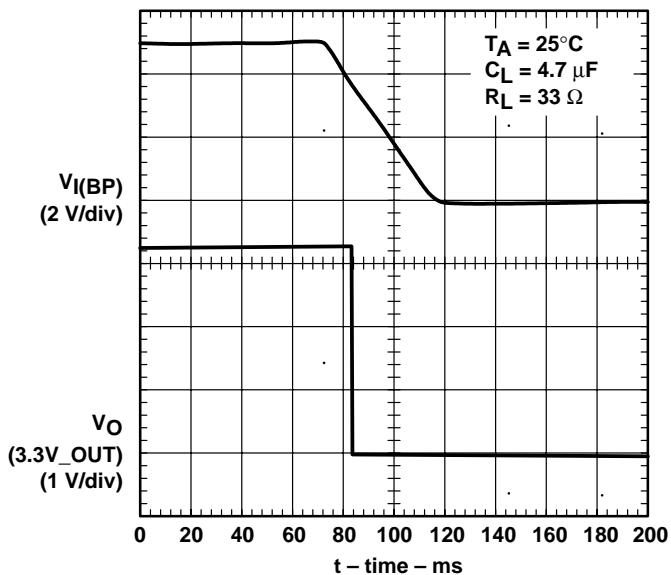


Figure 8. Turnoff Delay and Fall Time (3.3V_OUT)

PARAMETER MEASUREMENT INFORMATION

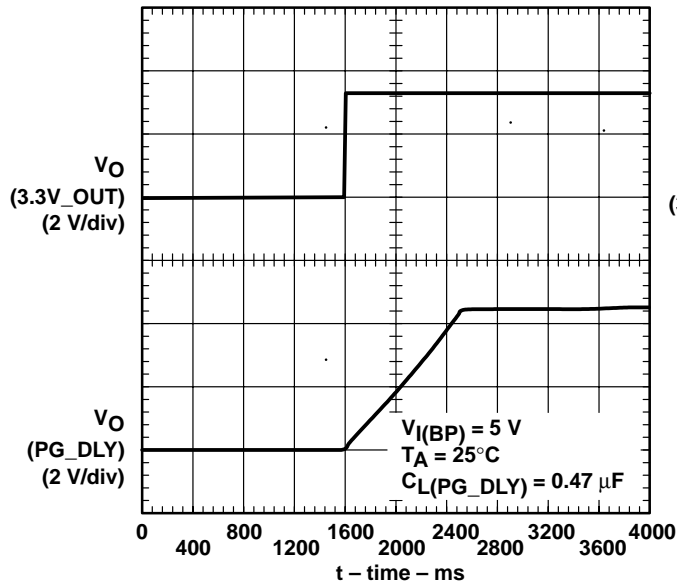


Figure 9. PG_DLY Rise Time With a 0.47- μ F Capacitor

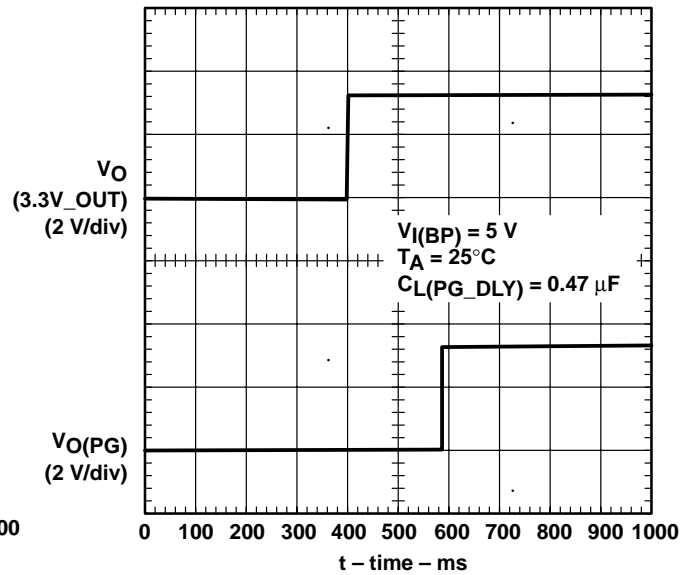


Figure 10. Turnon Delay (3.3V_OUT to PG)

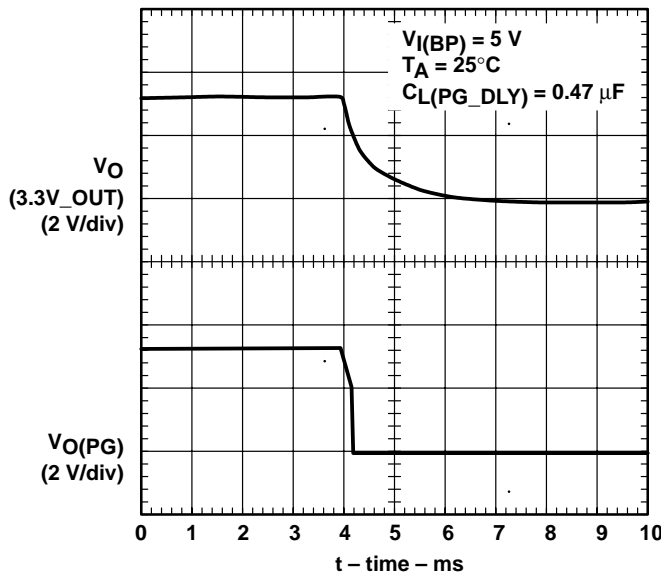


Figure 11. Turnoff Time (3.3V_OUT to PG)

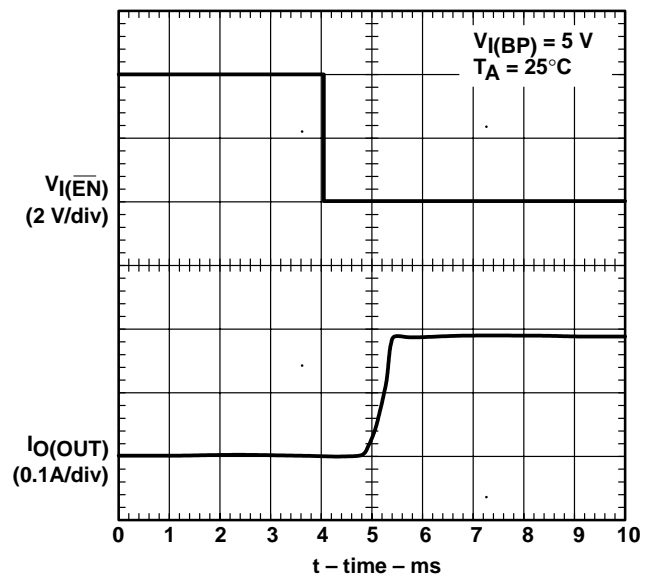


Figure 12. Short-Circuit Current (BP Switch), Device Enabled Into Short

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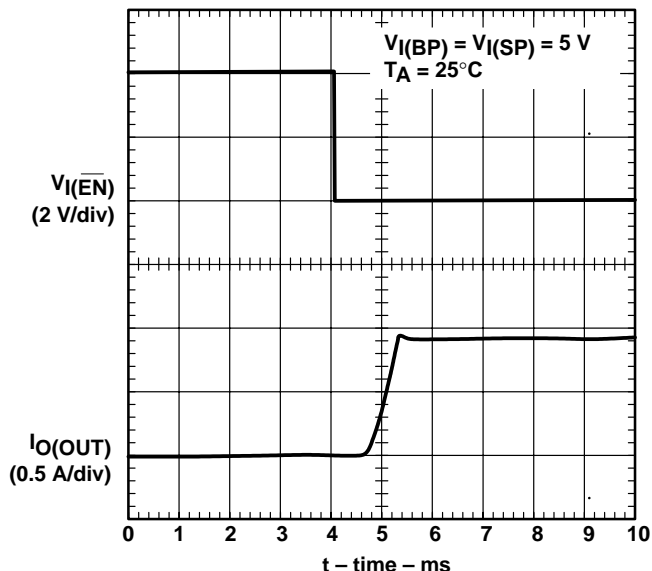


Figure 13. Short-Circuit Current (SP Switch), Device Enabled Into Short

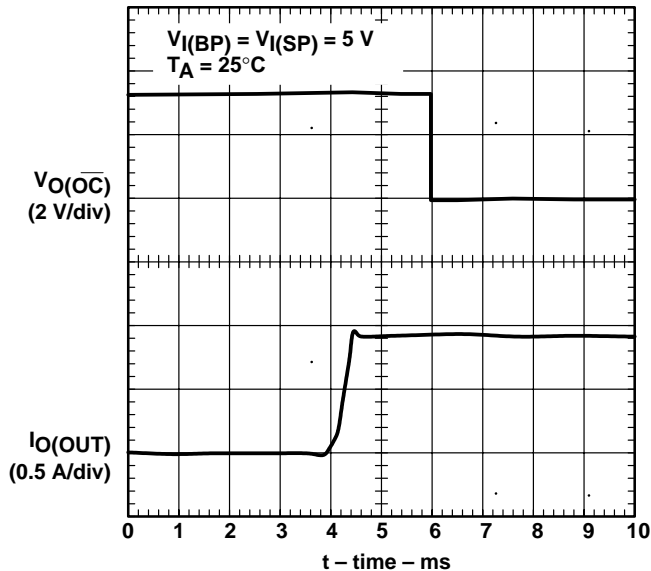


Figure 14. \overline{OC} Response (SP Switch), Device Enabled Into Short

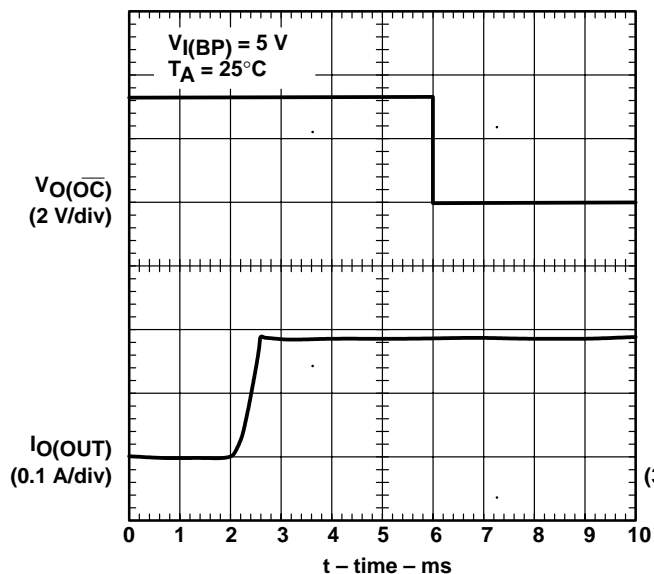


Figure 15. \overline{OC} Response (BP Switch), Device Enabled Into Short

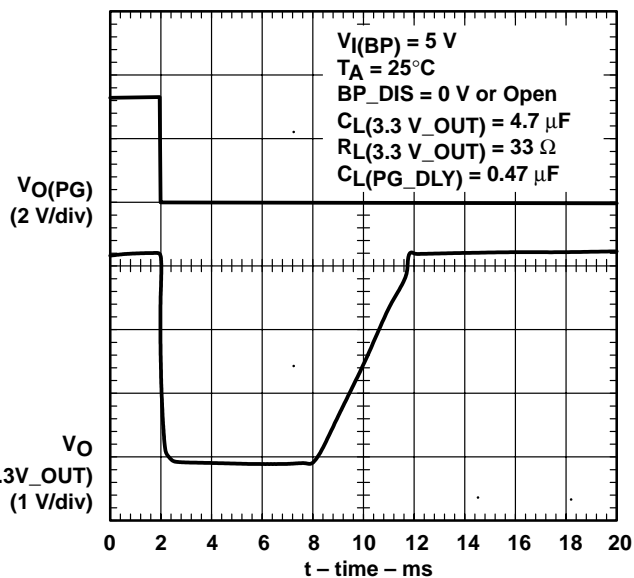


Figure 16. SP to BP Automatic Switchover Enabled

PARAMETER MEASUREMENT INFORMATION

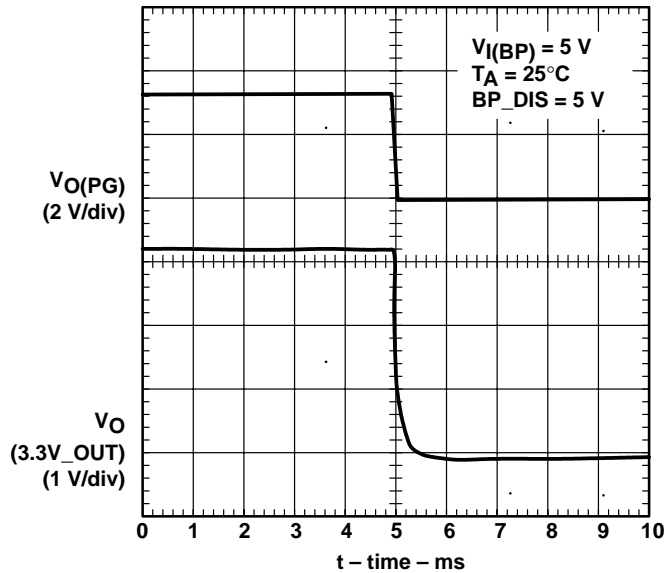


Figure 17. SP to BP Automatic Swiclover Disabled

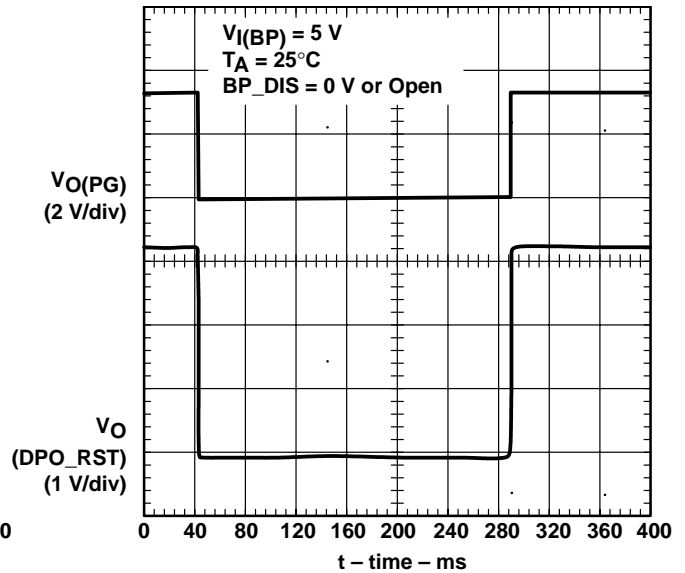


Figure 18. SP to BP Automatic Swiclover Enabled

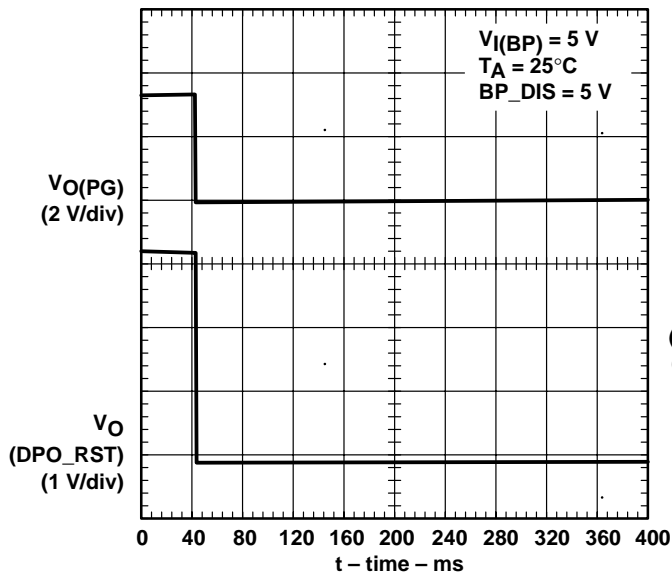


Figure 19. SP to BP Automatic Swiclover Disabled

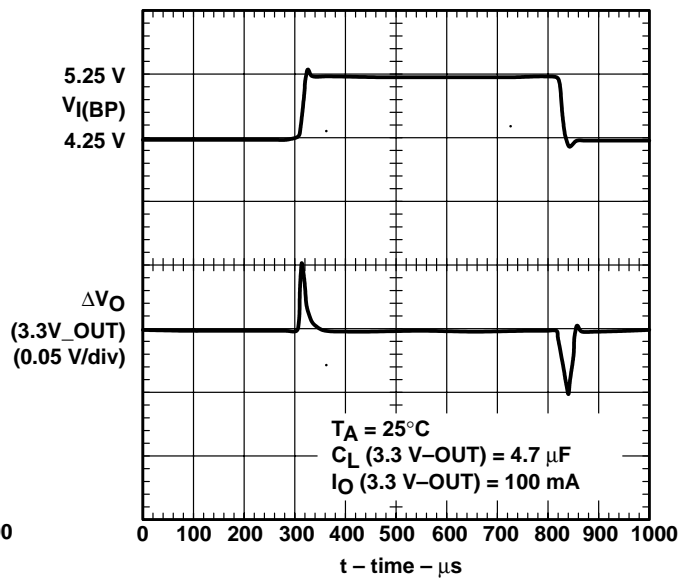


Figure 20. Line Transient Response

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PARAMETER MEASUREMENT INFORMATION

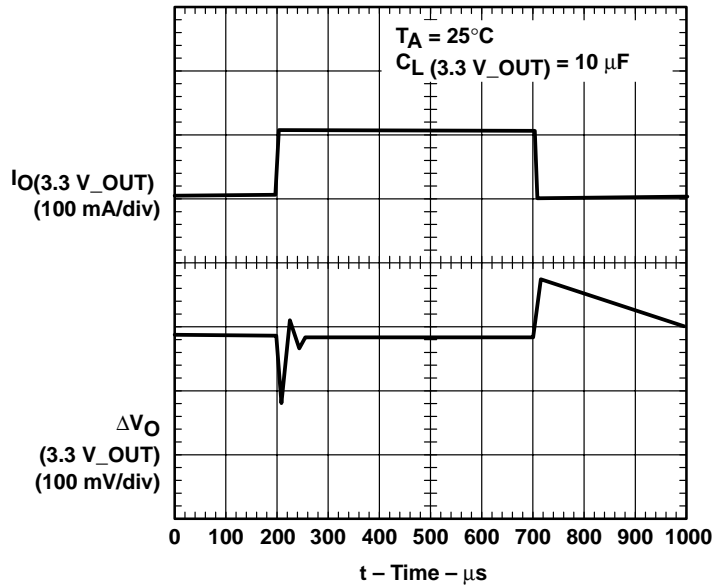


Figure 21. Load Transient Response

TYPICAL CHARACTERISTICS

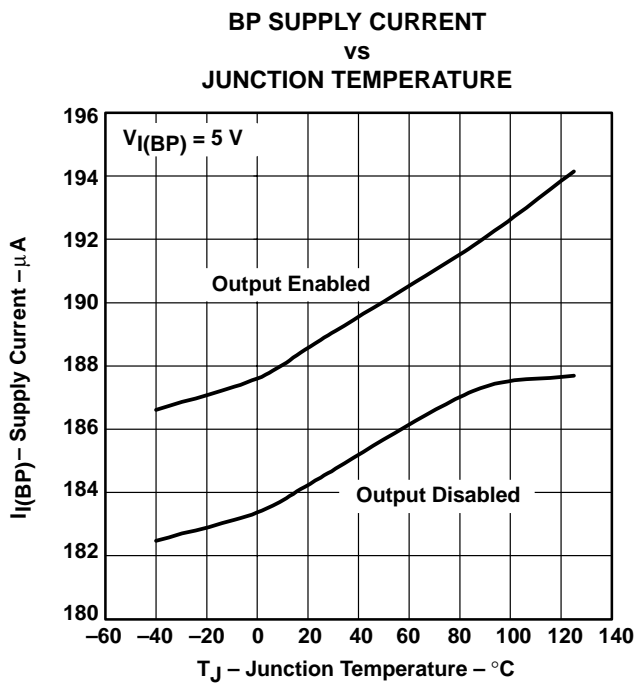


Figure 22

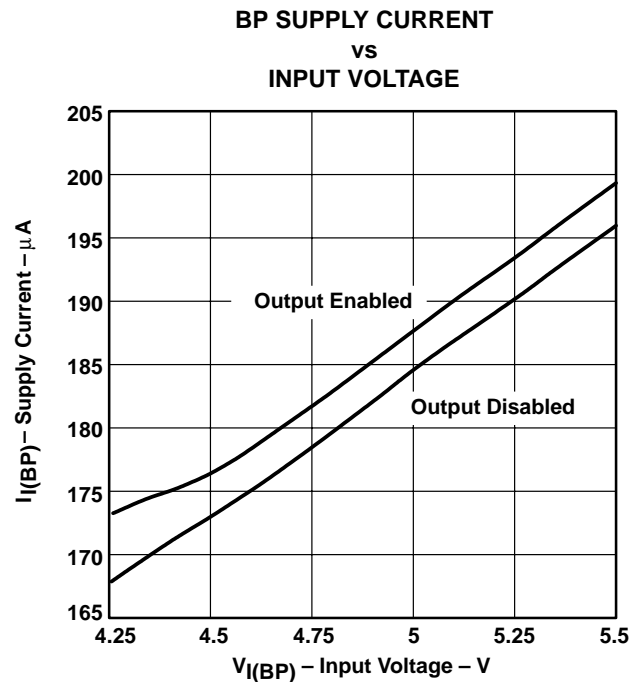


Figure 23

TYPICAL CHARACTERISTICS

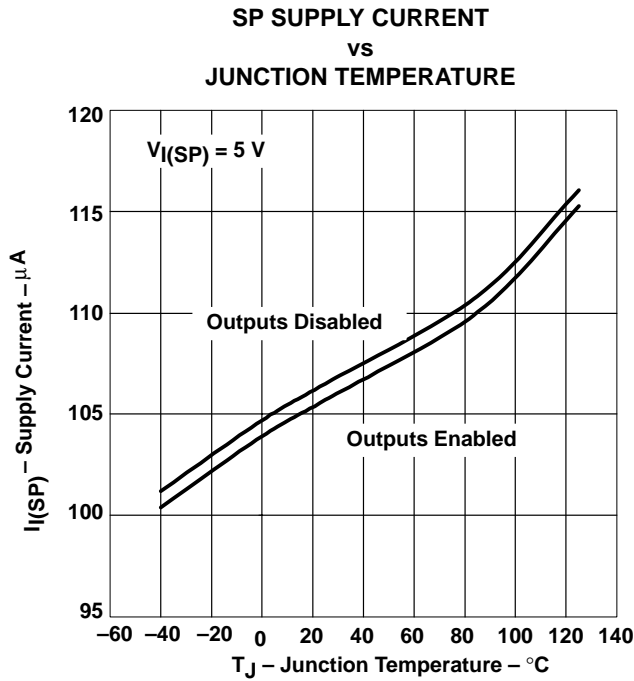


Figure 24

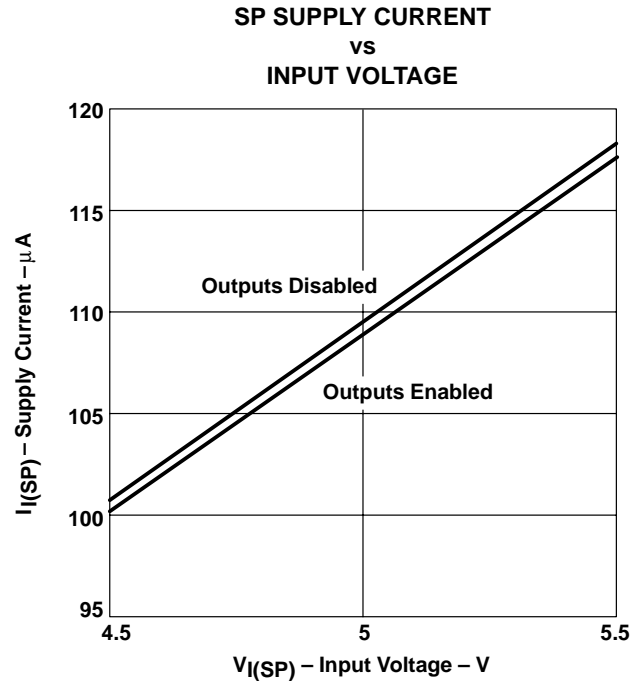


Figure 25

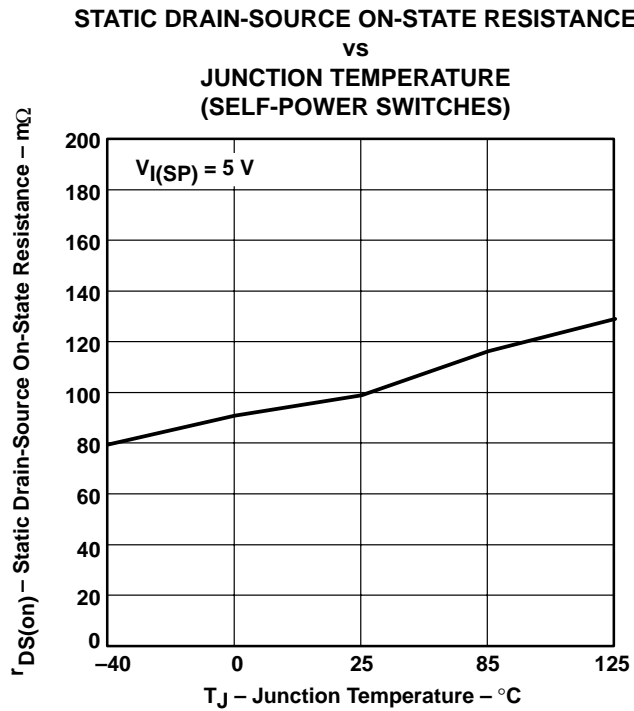


Figure 26

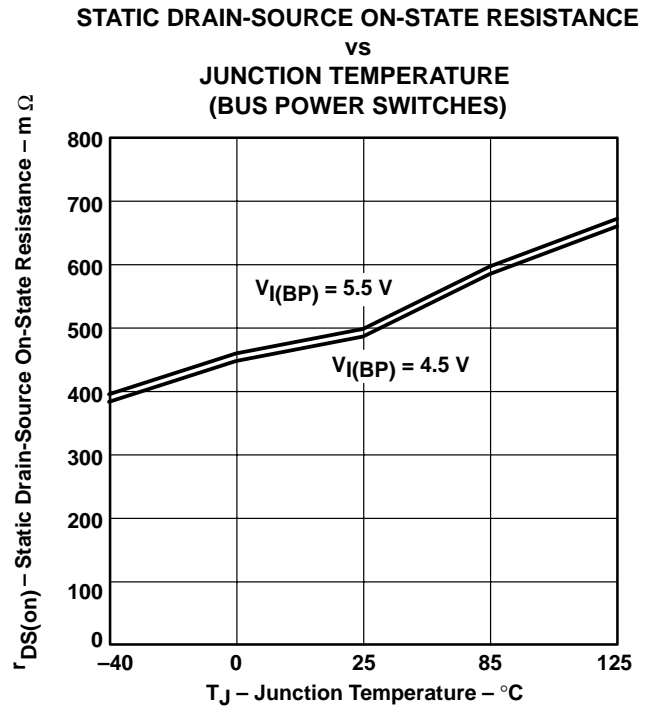


Figure 27

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TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE
(BUS-POWER SWITCHES)

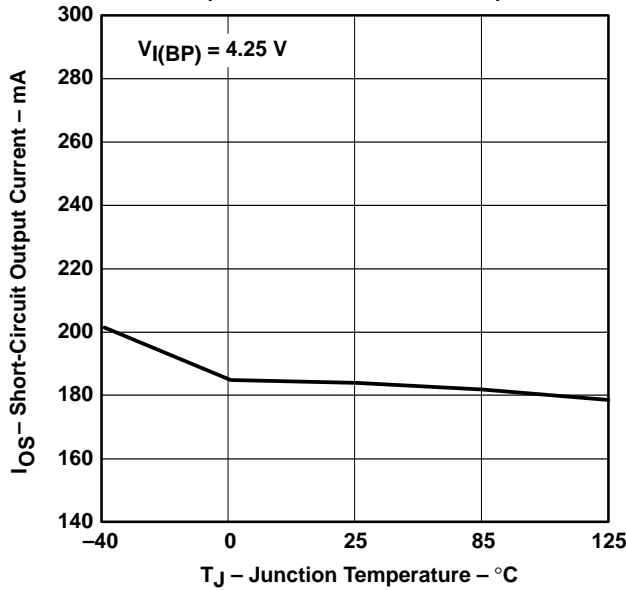


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE
(BUS-POWER SWITCHES)

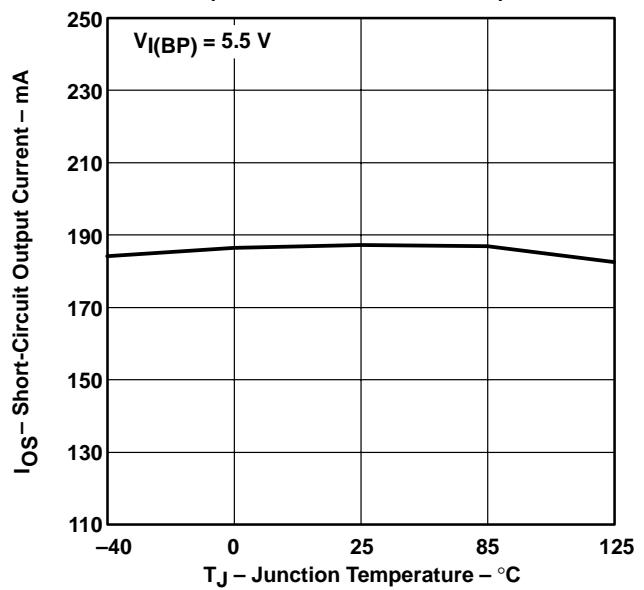


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE
(SELF-POWER SWITCHES)

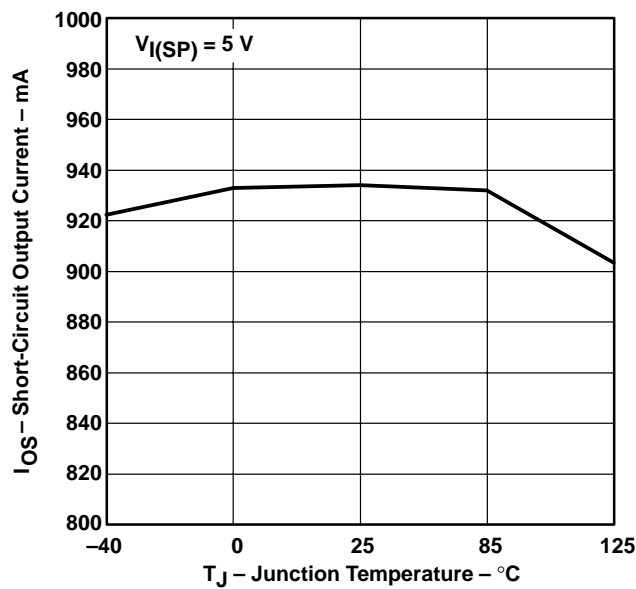


Figure 30

INPUT VOLTAGE (BP UNDERVOLTAGE LOCKOUT)
vs
JUNCTION TEMPERATURE

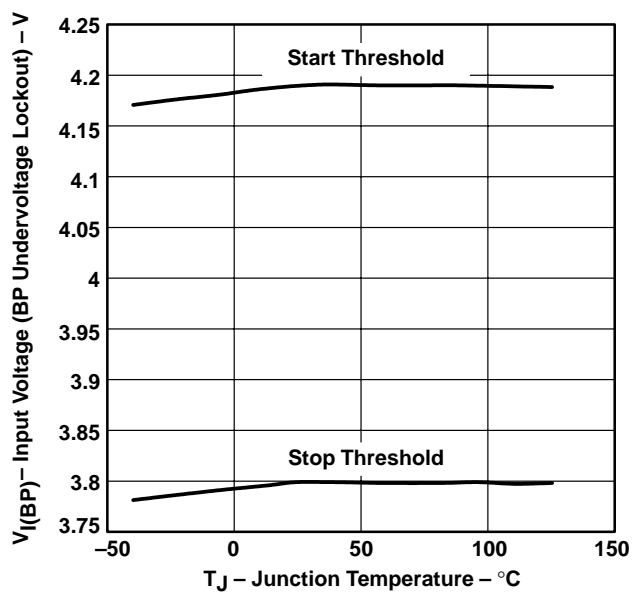


Figure 31



TYPICAL CHARACTERISTICS

INPUT VOLTAGE (SP UNDERVOLTAGE LOCKOUT)
 vs
 JUNCTION TEMPERATURE

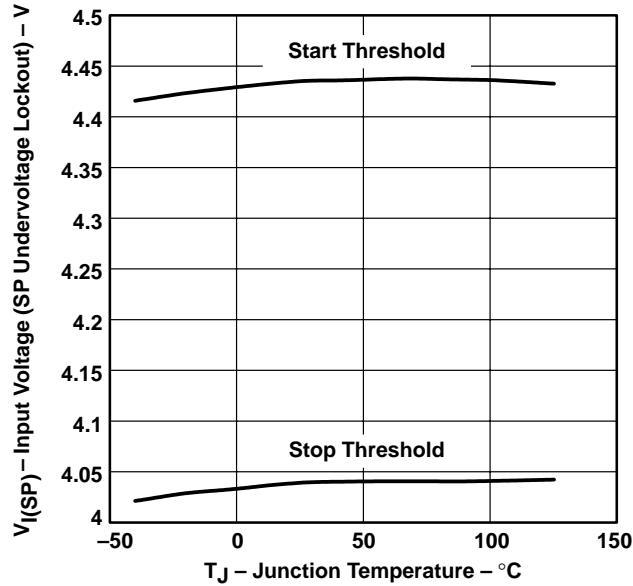


Figure 32

INPUT CURRENT
 vs
 JUNCTION TEMPERATURE

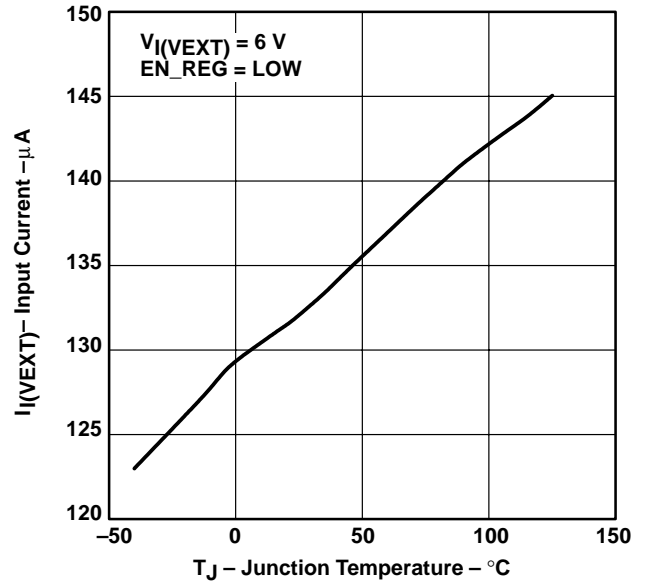


Figure 33

INPUT CURRENT
 vs
 JUNCTION TEMPERATURE

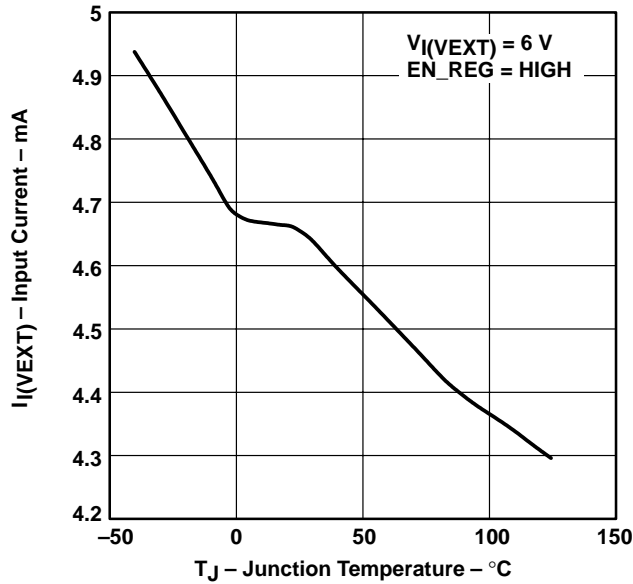


Figure 34

INPUT CURRENT
 vs
 INPUT VOLTAGE

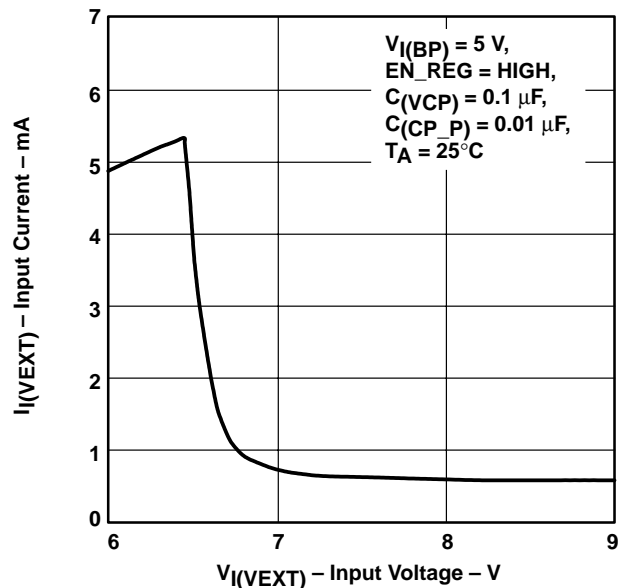


Figure 35

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TYPICAL CHARACTERISTICS

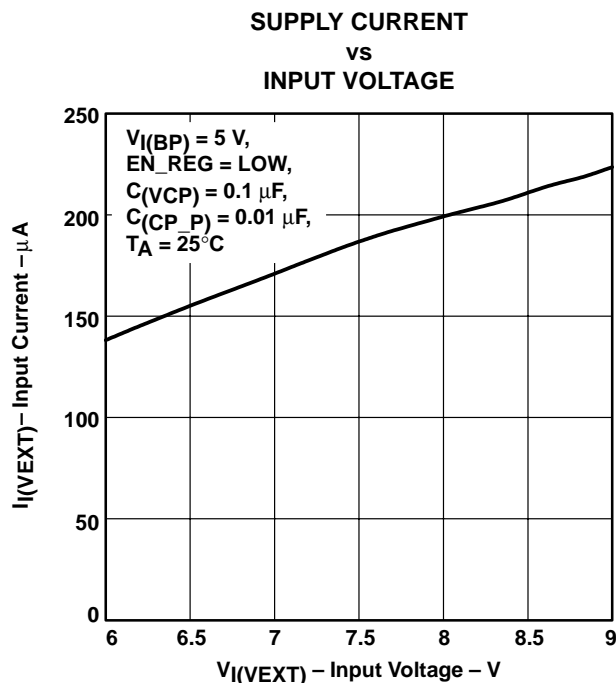


Figure 36

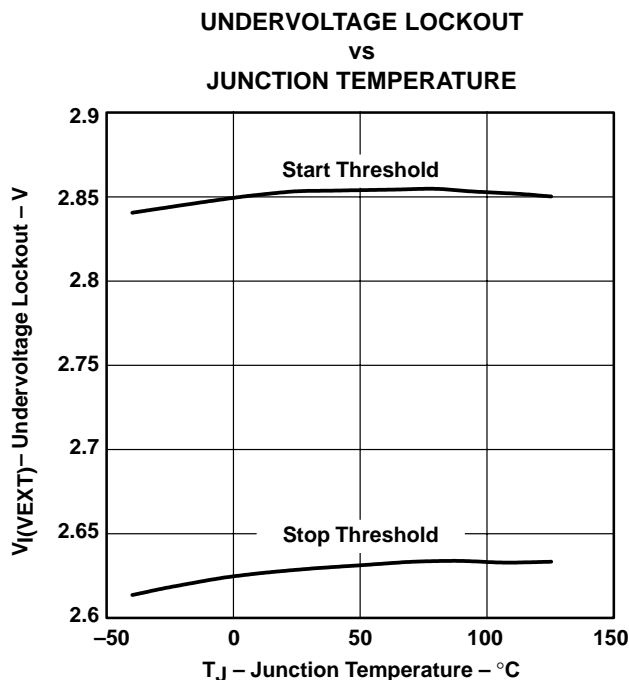


Figure 37

APPLICATION INFORMATION

external capacitor requirements

A 0.1-μF ceramic bypass capacitor and a 10-μF bulk capacitor between BP and AGND, close to the device, are recommended. Similarly, a 0.1-μF ceramic and a 68-μF bulk capacitor, from SP to AGND, and from VEXT to AGND if an external 5-V LDO is required, are recommended because of much higher current in the self-powered mode.

From each of the outputs (OUTx) to ground, a 33-μF or higher valued bulk capacitor is recommended when the output load is heavy. This precaution reduces power-supply transients. Additionally, bypassing the outputs with a 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

An output capacitor connected between 3.3V_OUT and GND is required to stabilize the internal control loop. The internal LDO is designed for a capacitor range of 4.7 μF to 33 μF with an ESR of 0.2 Ω to 10 Ω. Solid tantalum-electrolytic, aluminum-electrolytic and multilayer ceramic capacitors are all suitable.

Ceramic capacitors have different types of dielectric material, each exhibiting different temperature and voltage variations. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable for use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature. For this reason, the Y5U and Z5U are not generally recommended.

APPLICATION INFORMATION

external capacitor requirements (continued)

A transient condition occurs because of a sudden increase in output current. The output capacitor reduces the transient effect by providing the additional current needed by the load. Depending on the current demand at the output, a voltage drop will occur across the internal resistance, ESR, of the capacitor. Using a low ESR capacitor will help minimize this voltage drop. A larger capacitor will also reduce the voltage drop by supplying the current demand for a longer time, versus that provided by a smaller capacitor.

overcurrent

An internal sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before BP and SP have been applied. The TPS2070 and TPS2071 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2070 and TPS2071 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OCx}}$ output is asserted (active low) when an overcurrent or overtemperature condition is encountered and will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device and charging the downstream capacitor. The TPS2070 and TPS2071 are designed to reduce false overcurrent reporting by implementing an internal deglitch circuit. This circuit eliminates the need for an external filter, which requires extra components. Also, using low-ESR electrolytic capacitors on the outputs can reduce erroneous overcurrent reporting by providing a low-impedance energy source to lower the inrush current flow through the device during hot-plug events. The $\overline{\text{OCx}}$ outputs are logic outputs thereby requiring no pullup or pulldown resistors.

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APPLICATION INFORMATION

power dissipation and junction temperature

The major source of power dissipation for the TPS2070 and TPS2071 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown under the typical characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by four to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = (V_{I(BP)} - V_{O(min)}) \times I_{O(OUT)}$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(voltage\ regulator)} + (4 \times P_{D(switch)})$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = ambient temperature °C

$R_{\theta JA}$ = Thermal resistance °C/W, equal to inverting of derating factor found on the power dissipation table in this data sheet.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods. The faults force the TPS2070 and TPS2071 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2070 and TPS2071 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. Once the die temperature rises to approximately 140°C, the internal thermal-sense circuitry determines which power switch is in an overcurrent condition and turns only that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. If the die temperature exceeds the first thermal trip point of 140°C and reaches 150°C, the device turns off. The \overline{OC} output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO will also keep the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO will activate whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

self-power to bus-power or bus-power to self-power transition

An autoswitching function between bus-powered mode and self-powered mode is a feature of the TPS2070 and TPS2071. When this feature is enabled (BP_DIS is inactive) and SP is removed or applied, a transition will be initiated. The transition sequence begins with the internal LDO being turned off and its external capacitance discharged. Any enabled switches are also turned off and the external capacitors discharged. Once the LDO and switch outputs are low, the internal logic will turn the LDO back on. This entire sequence occurs whenever power to the SP input is removed or applied, regardless of the source of power, i.e., an external power supply or the use of the external regulator.

TPS2070, TPS2071 FOUR-PORT USB HUB POWER CONTROLLERS

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APPLICATION INFORMATION

universal serial bus (USB) applications

The universal serial bus (USB 1.1) interface is a 12-Mb/s, 1.5-Mb/s, or 480 Mb/s (USB 2.0), multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V-level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub or across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2070 and TPS2071 can provide power-distribution solutions for hybrid hubs that need switching between BPH and SPH according to power availability and application requirements.

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
 - Current-limit downstream ports
 - Report overcurrent conditions on USB V_{BUS}
 - Output 5.25 V to 4.75 at 500 mA
- Bus-powered hubs must:
 - Enable/disable power to downstream ports
 - Power up at <100 mA
 - Limit inrush current (<44 Ω and 10 μ F)
 - Output 5.25 V to 4.4 at 100 mA
 - Not send power back upstream
- Functions must:
 - Limit inrush currents
 - Power up at <100 mA
 - Not send power back upstream (SP functions)

The feature set of the TPS2070 and TPS2071 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the needs of both input and output ports on hubs, as well as the input ports for bus-powered functions



APPLICATION INFORMATION

USB hybrid hub

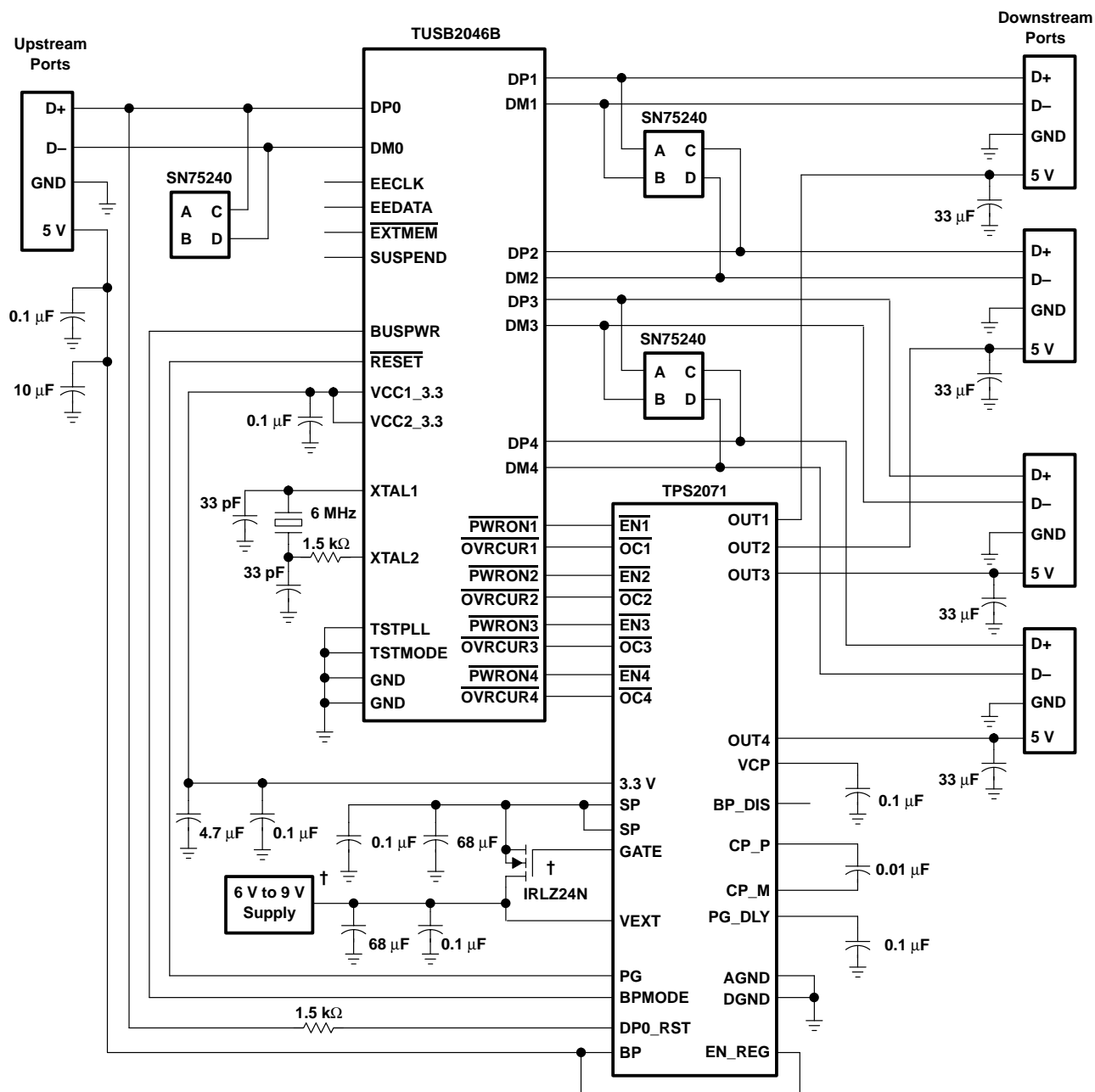
A USB hybrid hub can be simply implemented using the TPS2071 USB power controller and a TUSB2046 USB hub controller as shown in Figure 38. The TPS2071 USB power controller provides all the power needs to the four downstream ports and meets all the USB power specifications for both self-powered hubs and bus-powered hubs. The power controllers integrated 3.3-V LDO is used to provide power for the hub controller and any other local functions (e.g. transient suppressor SN75240), which saves board space and cost. The TPS2071 also provides the hub controller with a power good (PG) signal that connects to the $\overline{\text{RESET}}$ input of the hub controller to automatically reinitialize the hub when switching between self-powered mode and bus-powered mode whenever the self-power supply is connected or disconnected. The amount of time in which the hub controller is kept in a reset state is controlled by a capacitor connected between the PG_DLY pin of the power controller and ground.

By using an external N-channel MOSFET and the TPS2071 internal voltage-regulator controller, a regulated 5-V self-powered source can be generated from an input voltage range of 6 V to 9 V (see Figure 38). In this configuration, the internal voltage regulator controller is enabled by connecting the EN_REG input to the BP input. Using the internal voltage regulator controller also requires connecting a 0.01 μF capacitor between CP_P and CP_M of the TPS2071 power controller. Also, a 0.1- μF capacitor is needed between VCP of the power controller and ground.

TPS2070, TPS2071 FOUR-PORT USB HUB POWER CONTROLLERS

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APPLICATION INFORMATION



† This hybrid hub can also be implemented by connecting a 5-V power supply to the SP input of the TPS2071 and eliminating the external FET. However, this type of implementation is best suited for the TPS2074/75 (refer to the TPS2074, TPS2075 data sheet for details).

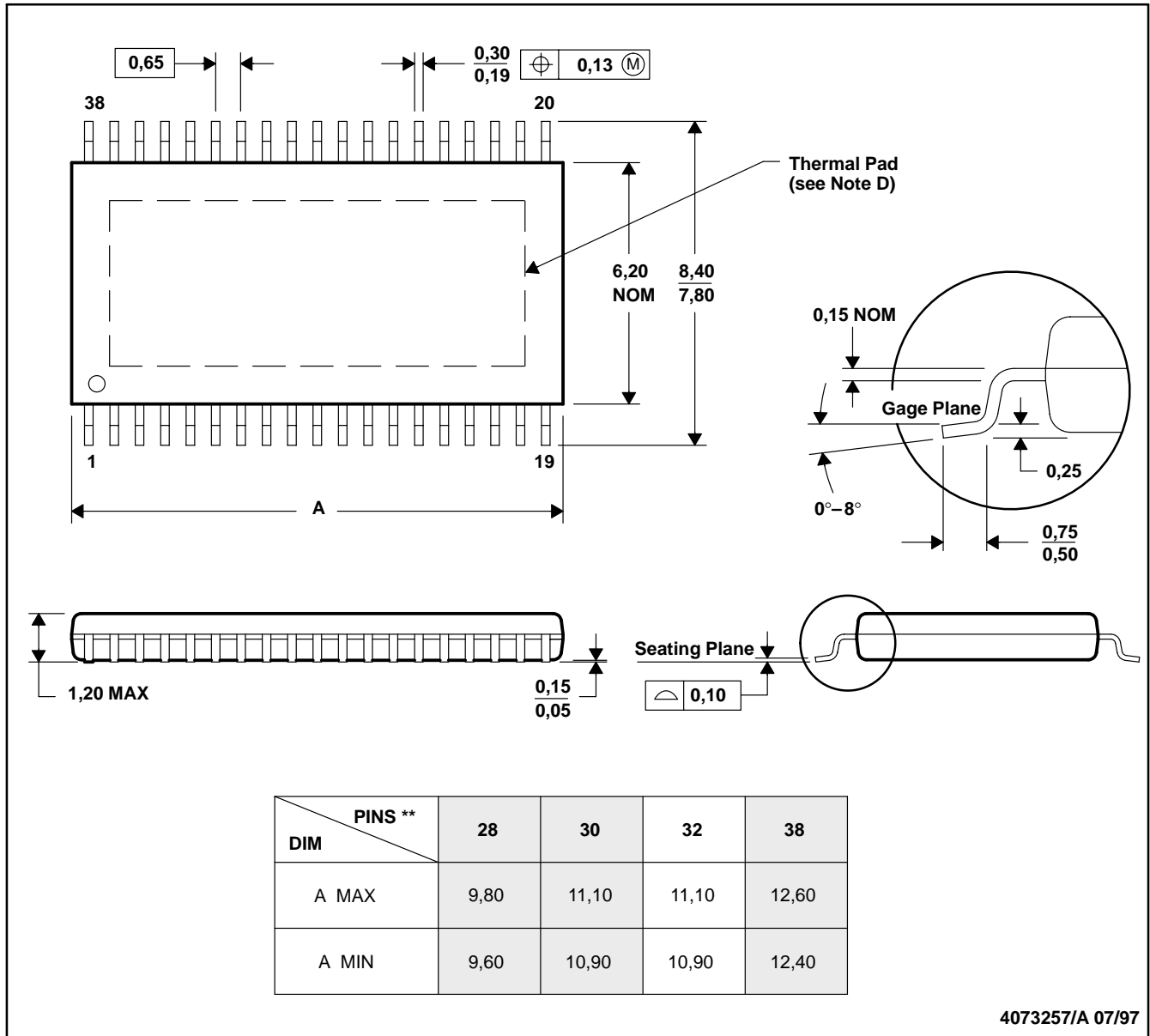
Figure 38. USB Hybrid Hub Using TPS2071 Power Controller and TUSB2046 Hub Controller

MECHANICAL DATA

DAP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

38 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS2070DAP | ACTIVE | HTSSOP | DAP | 32 | 46 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TPS2071DAP | ACTIVE | HTSSOP | DAP | 32 | 46 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TPS2071DAPR | ACTIVE | HTSSOP | DAP | 32 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TPS2071DAPRG4 | ACTIVE | HTSSOP | DAP | 32 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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