HIGH-EFFICIENCY, MIDRANGE-INPUT, SYNCHRONOUS BUCK CONTROLLER WITH VOLTAGE FEED-FORWARD

FEATURES

- **Operation Over 4.5-V to 28-V Input Range**
- **Programmable, Fixed-Frequency, up to 1-MHz, Voltage-Mode Controller**
- **Predictive Gate Drive™ Anti-Cross-Conduction Circuitry**
- **<1% Internal 700-mV Reference**
- **Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs**
- **16-Pin PowerPAD™ Package**
- **Thermal Shutdown Protection**
- **Pre-Bias Compatible**
- **Power-Stage Shutdown Capability**
- **Programmable High-Side Sense Short-Circuit Protection**

APPLICATIONS

- **Power Modules**
- **Networking/Telecom**
- **PCI Express**
- **Industrial**
- **Servers**

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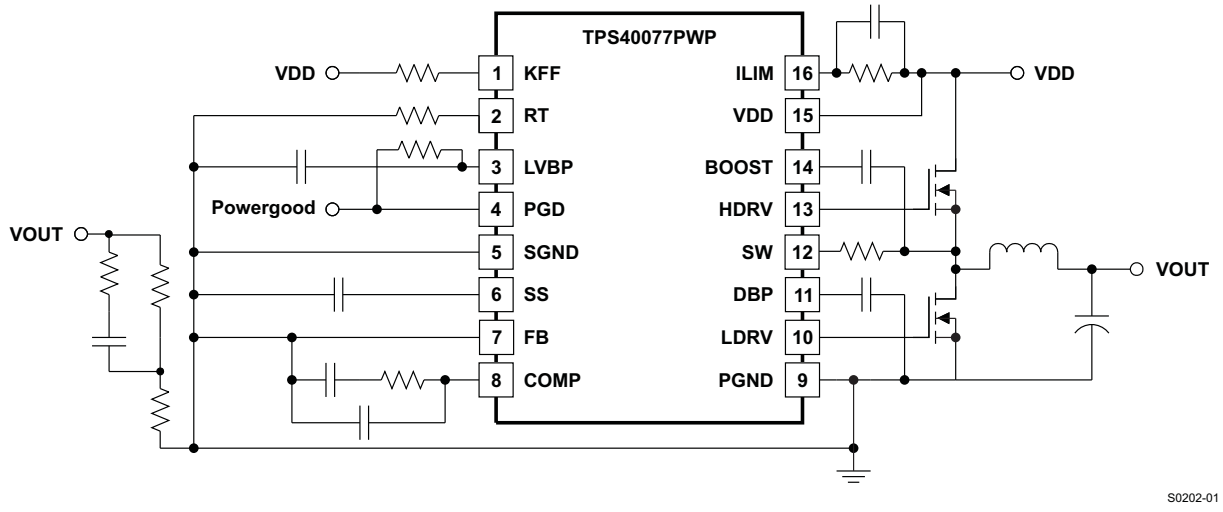
DESCRIPTION

The TPS40077 is a midvoltage, wide-input (4.5-V to 28-V), synchronous, step-down controller, offering design flexibility for a variety of user-programmable functions, including soft start, UVLO, operating frequency, voltage feed-forward, and high-side, FET-sensed, short-circuit protection.

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION (CONTINUED)

The TPS40077 drives external N-channel MOSFETs using second-generation, predictive-gate drive to minimize conduction in the body diode of the low-side FET and maximize efficiency. Pre-biased outputs are supported by not allowing the low-side FET to turn on until the voltage commanded by the closed-loop soft start is greater than the pre-bias voltage. Voltage feed-forward provides good response to input transients and provides a constant PWM gain over a wide input-voltage operating range to ease compensation requirements. Programmable short-circuit protection provides fault-current limiting and hiccup recovery to minimize power dissipation with a shorted output. The 16-pin PowerPAD package gives good thermal performance and a compact footprint.

ORDERING INFORMATION

PACKAGE		ORDERABLE PART NUMBER
Plastic HTSSOP (PWP)	Tube	TPS40077PWP
Plastic HTSSOP (PWP)	Tape and reel	TPS40077PWPR

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS40077	UNIT
V_{VDD}	Input voltage range	VDD, ILIM	30	V
		COMP, FB, KFF, PGD, LVBP	–0.3 to 6	
		SW	–0.3 to 40	
		SW, transient < 50 ns	–2.5	
V_{OUT}	Output voltage range	COMP, KFF, RT, SS	–0.3 to 6	V
		VBOOST	50	
		DBP	10.5	
		LVBP	6	
I_{OUT}	Output current source	LDRV, HDRV	1.5	A
	Output current sink	LDRV, HDRV	2	
		KFF	10	
	Output current	RT	1	mA
		LVBP	1.5	
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		28	V
T_A	Operating free-air temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

		UNIT
Human body model (HBM)	2000	V
Charged device model (CDM)	1500	V

PACKAGE DISSIPATION RATINGS

	Thermal Impedance, Junction-to-Ambient(1)	T_A = 25°C Power Rating	T_A = 85°C Power Rating
Natural convection	37°C/W	2.7 W	1.08 W
150 LFM airflow	30°C/W	3.33 W	1.33 W
250 LFM airflow	28°C/W	3.57 W	1.42 W
500 LFM airflow	26°C/W	3.84 W	1.52 W

(1) For more information on the board and the methods used to determine ratings, see the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input voltage range, VIN		4.5		28	V
OPERATING CURRENT						
I_{VDD}	Quiescent current	Output drivers not switching		2.5	3.5	mA
LVBP						
V_{LVBP}	Output voltage	$T_A = T_J$ = 25°C	3.9	4.2	4.5	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy		450	500	550	kHz
V_{RAMP}	PWM ramp voltage(1)	$V_{PEAK} – V_{VAL}$		2		V
V_{RT}	RT voltage		2.23	2.4	2.58	V
t_{ON}	Minimum output pulse time(1)	C_{HDRV} = 0 nF			150	ns
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW} ≤ 500 kHz	84%		93%	
		V_{FB} = 0 V, f_{SW} = 1 MHz	76%		93%	
V_{KFF}	Feed-forward voltage		0.35	0.4	0.45	V
I_{KFF}	Feed-forward current operating range(1)		20		1100	µA
SOFT START						
I_{SS}	Charge current		7	12	17	µA
t_{DSCH}	Discharge time	C_{SS} = 3.9 nF	25		75	µs
t_{SS}	Soft-start time	C_{SS} = 3.9 nF, V_{SS} rising from 0.7 V to 1.6 V	210	290	500	µs
V_{SSSD}	Turn on threshold		310	365	420	mV
	Shutdown threshold		225	275	325	
V_{SSSDH}	Shutdown threshold hysteresis		35		150	
DBP						
V_{DBP}	Output voltage	V_{DD} > 10 V	7	8	9	V
		V_{DD} = 4.5 V, I_{OUT} = 25 mA	4.0	4.3		
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage total variation	T_J = 25°C	0.698	0.7	0.704	V
		0°C ≤ T_J ≤ 85°C	0.69	0.7	0.707	
		-40°C ≤ T_J ≤ 85°C	0.69	0.7	0.715	
V_{SS}	Soft-start offset from VSS	Offset from V_{SS} to error amplifier		1		V
G_{BW}	Gain bandwidth		5	10		MHz
A_{VOL}	Open loop gain		50			dB
I_{SRC}	Output source current		2.5	4.5		mA
I_{SINK}	Output sink current		2.5	6		
I_{BIAS}	Input bias current	V_{FB} = 0.7 V	–250		0	nA

(1) Assured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORT-CIRCUIT CURRENT PROTECTION						
I_{ILIM}	Current sink into current limit		80	105	125	µA
$V_{ILIM(ofst)}$	Current limit offset voltage (V_{SW} – V_{ILIM})	V_{ILIM} = 11.5 V, V_{VDD} = 12 V	–75	–50	–30	mV
t_{HSC}	Minimum HDRV pulse duration	During short circuit		135	225	ns
	Propagation delay to output (2)			50		ns
t_{BLANK}	Blanking time(2)			50		ns
t_{OFF}	Off time during a fault (SS cycle times)			7		cycles
V_{SW}	Switching level to end precondition (V_{VDD} – V_{SW})(2)			2		V
t_{PC}	Precondition time(2)				100	ns
V_{ILIM}	Current limit precondition voltage threshold(2)			6.8		V
OUTPUT DRIVERS						
t_{HFALL}	High-side driver fall time (HDRV – SW)(2)	C_{HDRV} = 2200 pF		36		ns
t_{HRISE}	High-side driver rise time (HDRV – SW)(2)			48		ns
t_{HFALL}	High-side driver fall time (HDRV – SW)(2)	C_{HDRV} = 2200 pF, V_{VDD} = 4.5 V, 0.2 V ≤ V_{SS} ≤ 4 V		72		ns
t_{HRISE}	High-side driver rise time (HDRV – SW)(2)			96		ns
t_{LFALL}	Low-side driver fall time(2)	C_{LDRV} = 2200 pF		24		ns
t_{LRISE}	Low-side driver rise time(2)			48		ns
t_{LFALL}	Low-side driver fall time(2)	C_{LDRV} = 2200 pF, V_{VDD} = 4.5 V, 0.2 V ≤ V_{SS} ≤ 4 V		48		ns
t_{LRISE}	Low-side driver rise time(2)			96		ns
V_{OH}	High-level output voltage, HDRV (V_{BOOST} – V_{HDRV})	I_{HDRV} = –0.01 A		0.7	1	V
		I_{HDRV} = –0.1 A		0.95	1.3	
V_{OL}	Low-level output voltage, HDRV (V_{HDRV} – V_{SW})	I_{HDRV} = 0.01A		0.06	0.1	V
		I_{HDRV} = 0.1 A		0.65	1	
V_{OH}	High-level output voltage, LDRV (V_{DBP} – V_{LDRV})	I_{LDRV}= –0.01A		0.65	1	V
		I_{LDRV} = –0.1 A		0.875	1.2	
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.01 A		0.03	0.05	V
		I_{LDRV} = 0.1 A		0.3	0.5	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{DD} = 12 V	15.2	17		V
UVLO						
V_{UVLO}	Programmable UVLO threshold voltage	R_{KFF} = 90.9 kΩ, turn-on, V_{VDD} rising	6.2	7.2	8.2	V
	Programmable UVLO hysteresis	R_{KFF} = 90.9 kΩ	1.1	1.55	2	
	Fixed UVLO threshold voltage	Turn-on, V_{VDD} rising	4.15	4.3	4.45	
	Fixed UVLO hysteresis		275	365		mV
POWER GOOD						
V_{PG}	Power-good voltage	I_{PG} = 1 mA		370	500	mV
V_{OH}	High-level output voltage, FB			770		
V_{OL}	Low-level output voltage, FB			630		
THERMAL SHUTDOWN						
	Shutdown temperature threshold(2)			165		°C
	Hysteresis(2)			15		

(2) Assured by design. Not production tested.

TYPICAL CHARACTERISTICS

LVBP VOLTAGE
vs
JUNCTION TEMPERATURE

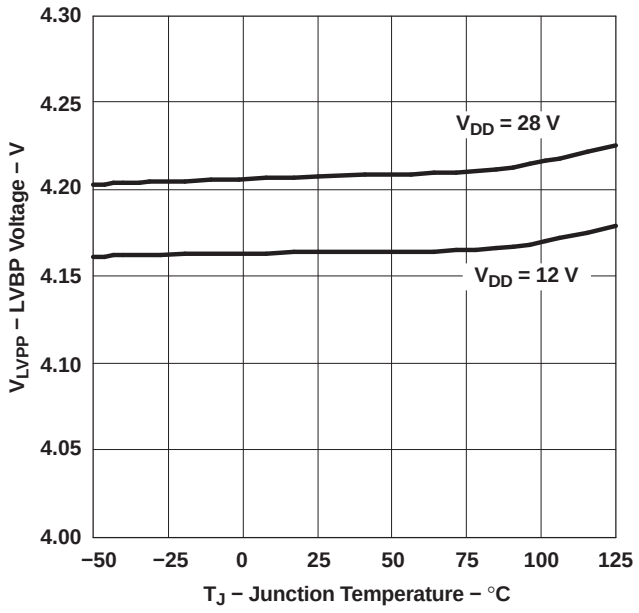


Figure 1.

DBP VOLTAGE
vs
JUNCTION TEMPERATURE

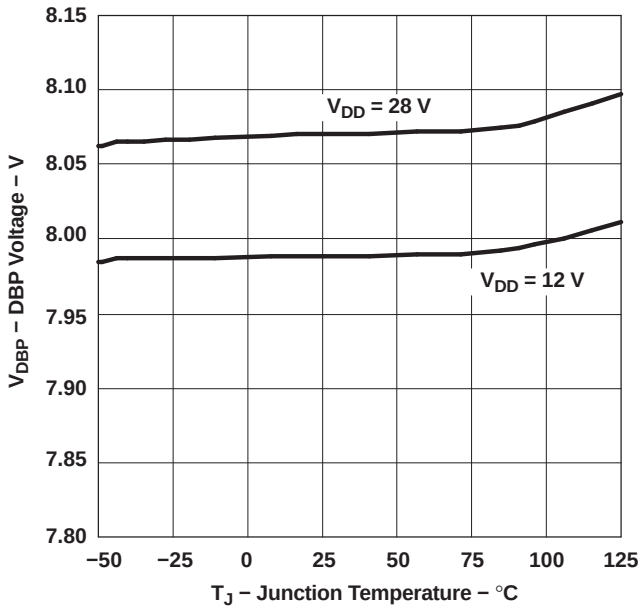


Figure 2.

DBP VOLTAGE
vs
JUNCTION TEMPERATURE

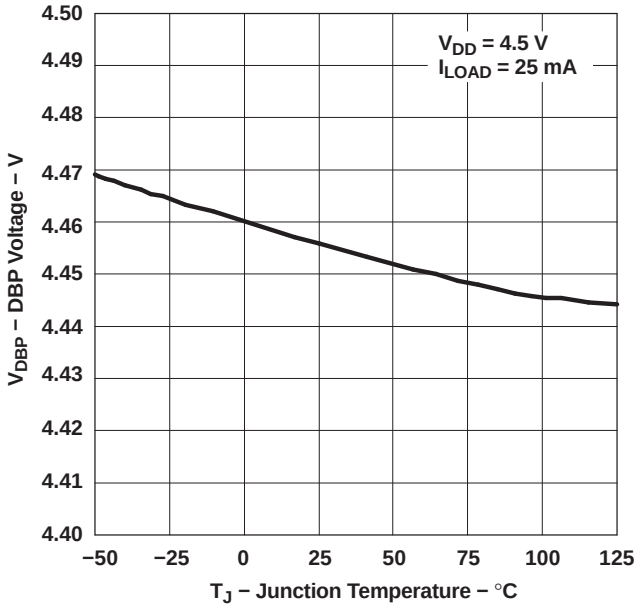


Figure 3.

BOOTSTRAP DIODE VOLTAGE
vs
JUNCTION TEMPERATURE

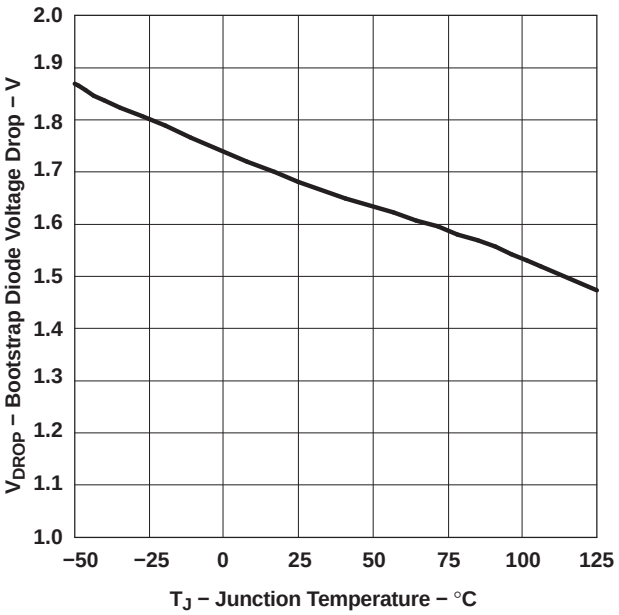


Figure 4.

TYPICAL CHARACTERISTICS (continued)

CURRENT LIMIT OFFSET VOLTAGE vs JUNCTION TEMPERATURE

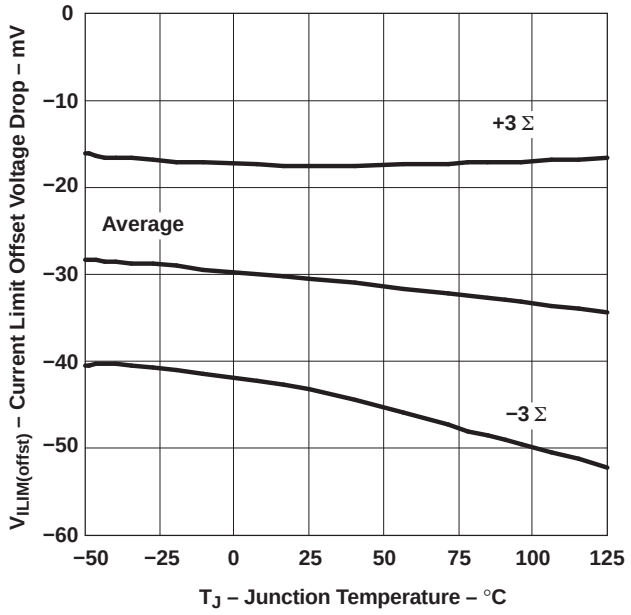


Figure 5.

CURRENT LIMIT SINK CURRENT vs JUNCTION TEMPERATURE

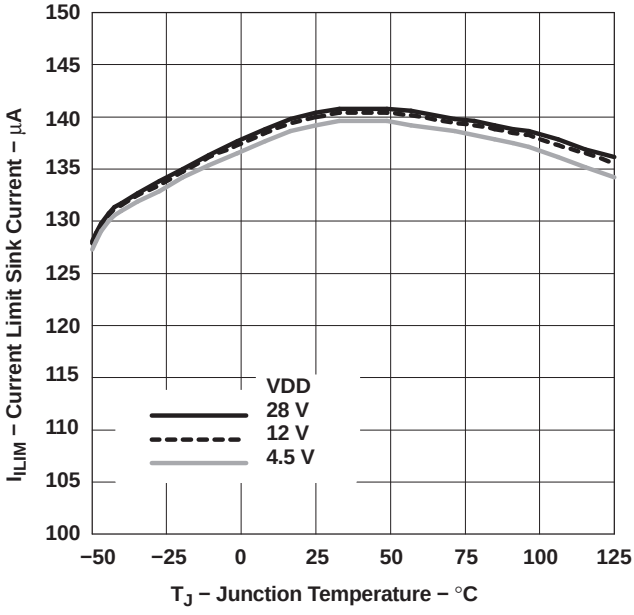


Figure 6.

FEEDBACK REGULATION VOLTAGE vs JUNCTION TEMPERATURE

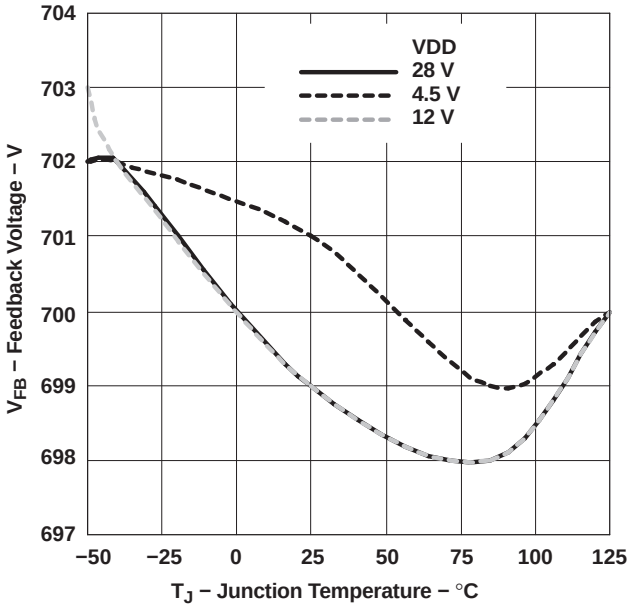


Figure 7.

SWITCHING FREQUENCY vs INPUT VOLTAGE

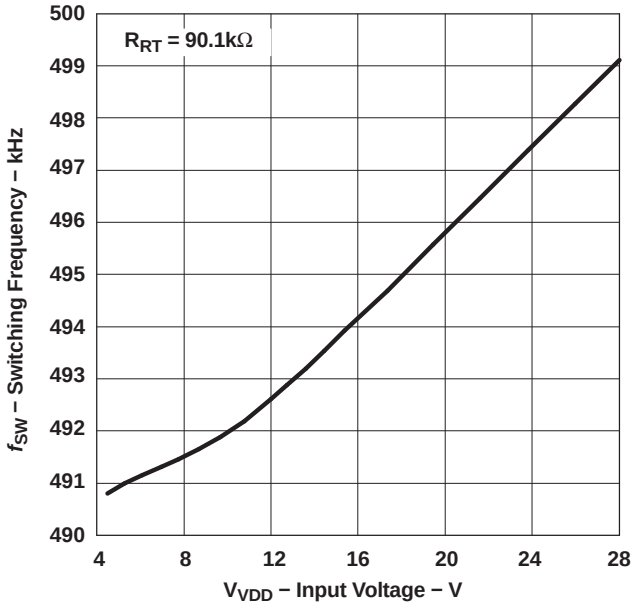


Figure 8.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM DUTY CYCLE
vs
JUNCTION TEMPERATURE

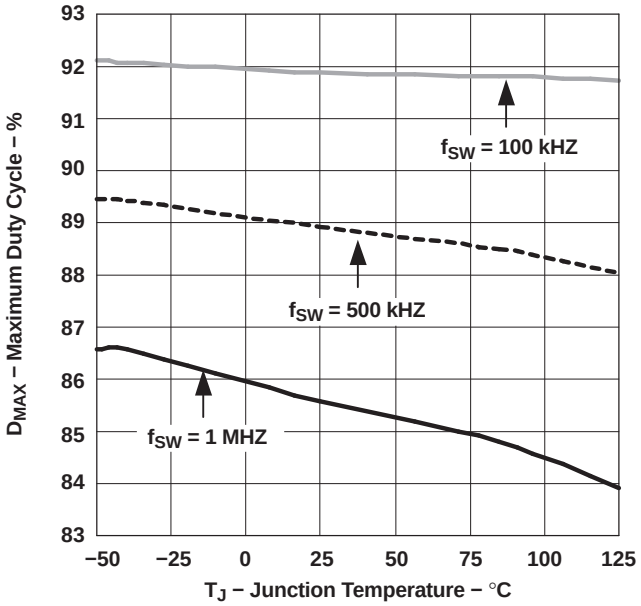


Figure 9.

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

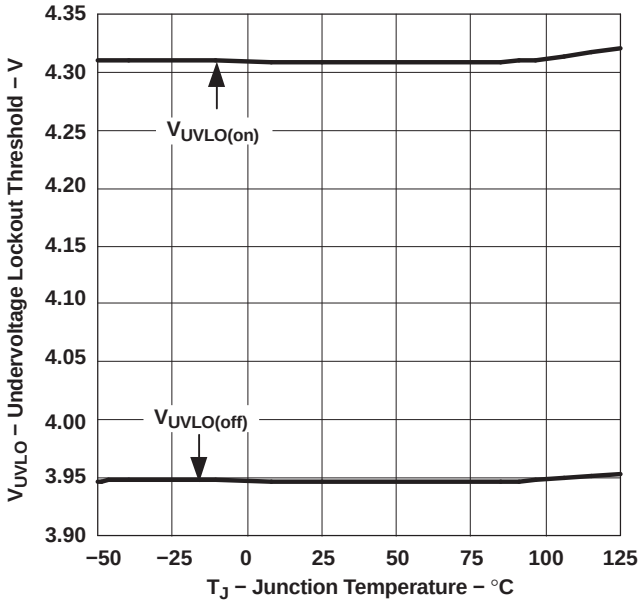


Figure 10.

PROGRAMMABLE UVLO THRESHOLD
vs
JUNCTION TEMPERATURE

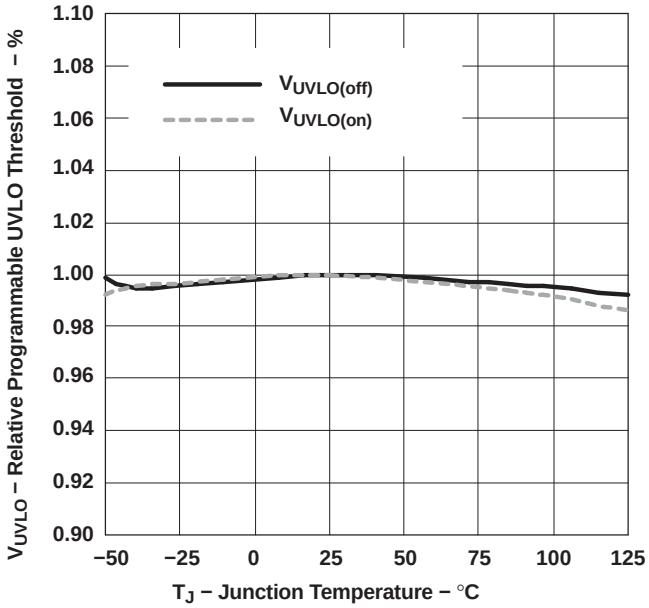


Figure 11.

SOFT-START CHARGING CURRENT
vs
JUNCTION TEMPERATURE

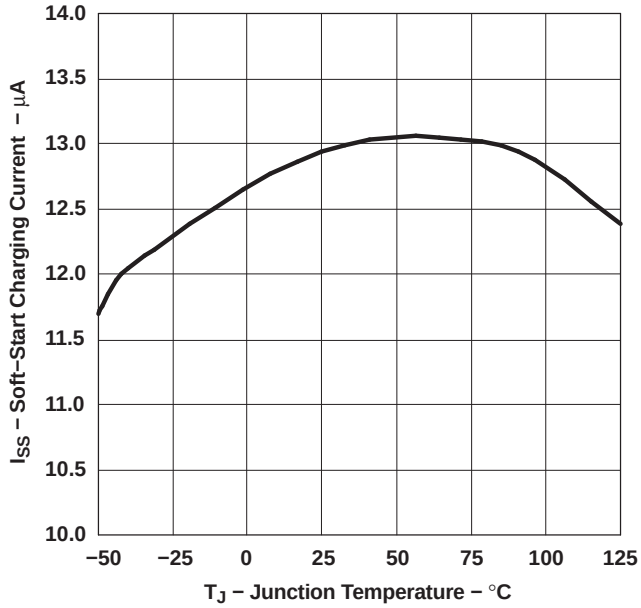


Figure 12.

TYPICAL CHARACTERISTICS (continued)

ERROR AMPLIFIER INPUT BIAS CURRENT vs JUNCTION TEMPERATURE

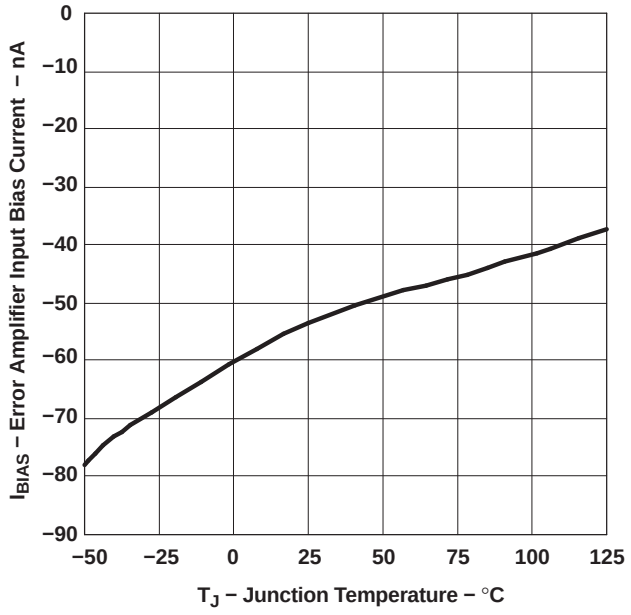


Figure 13.

MINIMUM OUTPUT VOLTAGE vs FREQUENCY

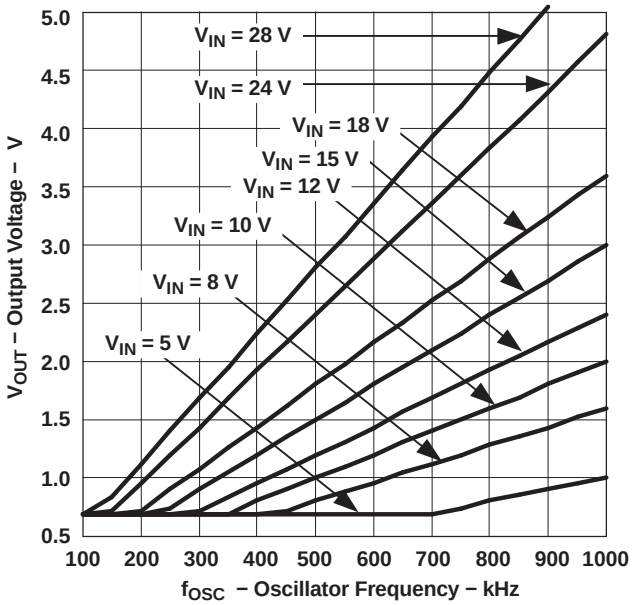


Figure 14.

SWITCHING FREQUENCY vs TIMING RESISTANCE

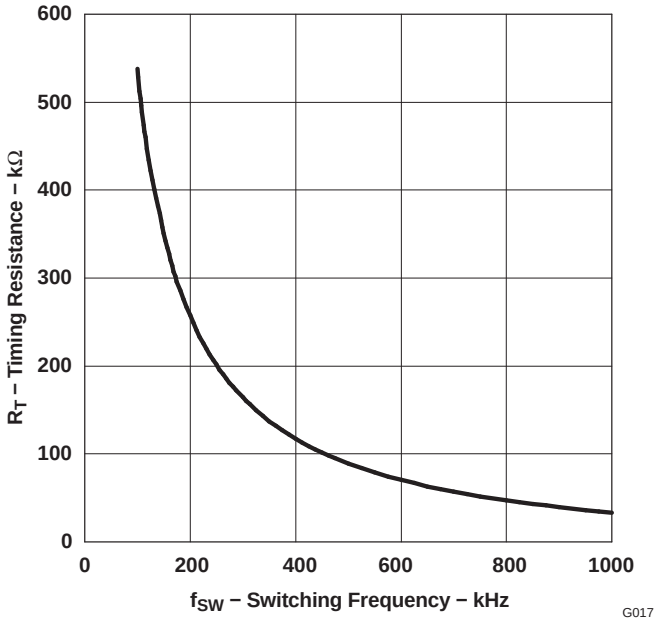


Figure 15.

UNDERVOLTAGE LOCKOUT THRESHOLD vs FEED-FORWARD IMPEDANCE

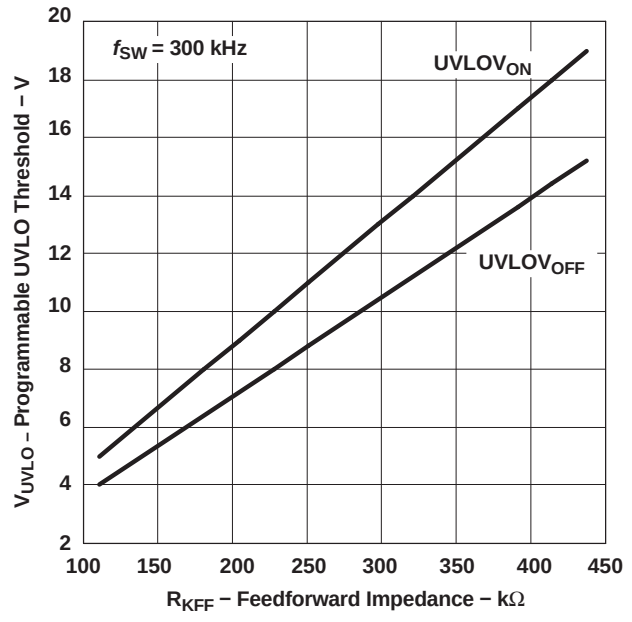


Figure 16.

TYPICAL CHARACTERISTICS (continued)

UNDERVOLTAGE LOCKOUT THRESHOLD vs FEED-FORWARD IMPEDANCE

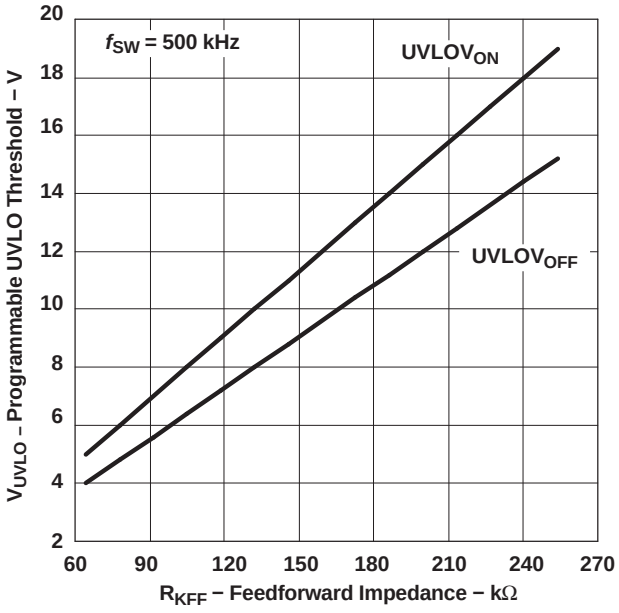


Figure 17.

UNDERVOLTAGE LOCKOUT THRESHOLD vs FEED-FORWARD IMPEDANCE

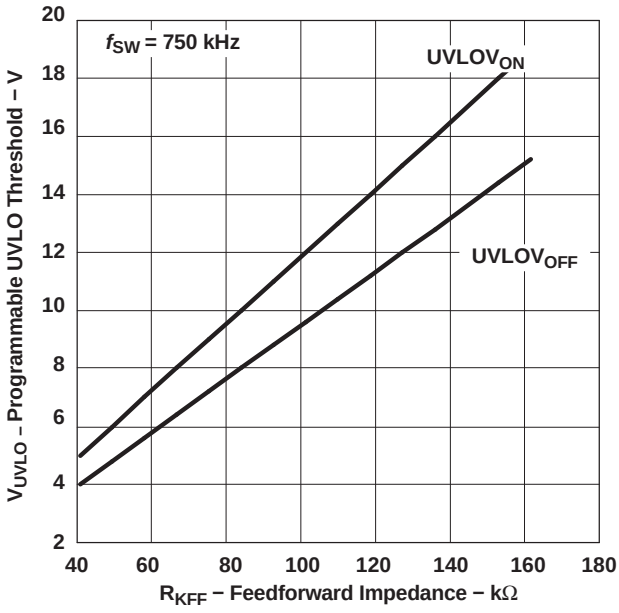


Figure 18.

TYPICAL MAXIMUM DUTY CYCLE vs INPUT VOLTAGE

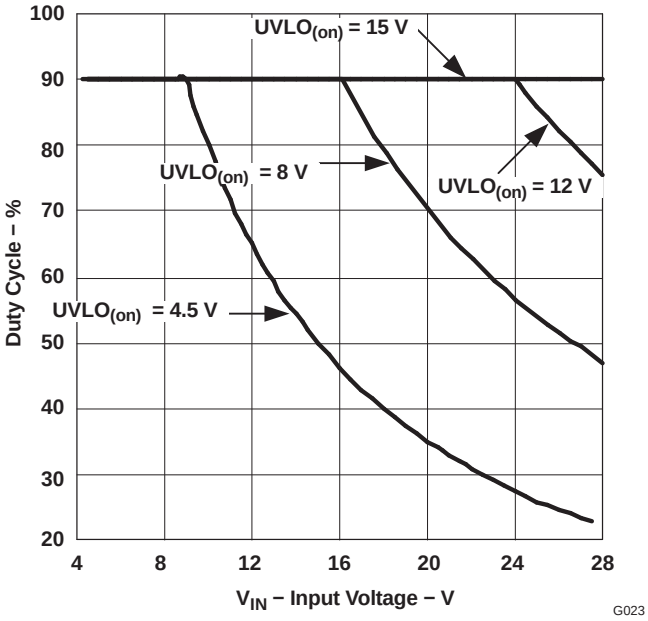


Figure 19.

DBP VOLTAGE vs INPUT VOLTAGE

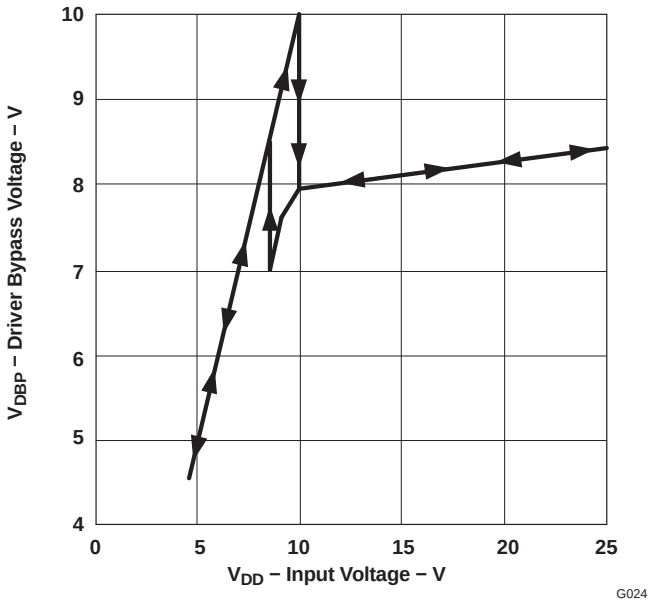


Figure 20.

TYPICAL CHARACTERISTICS (continued)

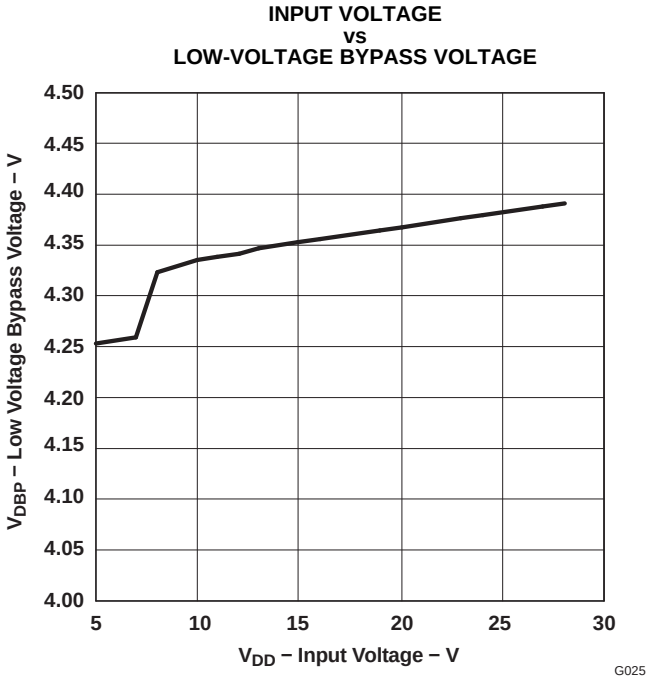
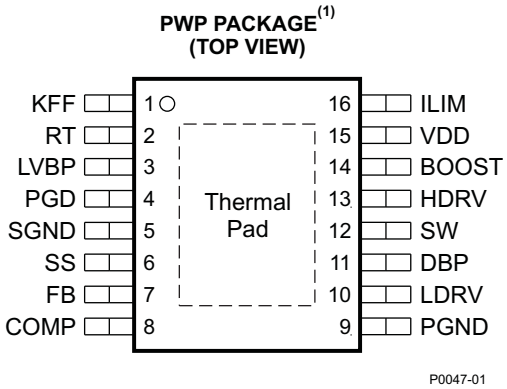


Figure 21.

DEVICE INFORMATION

Terminal Configuration



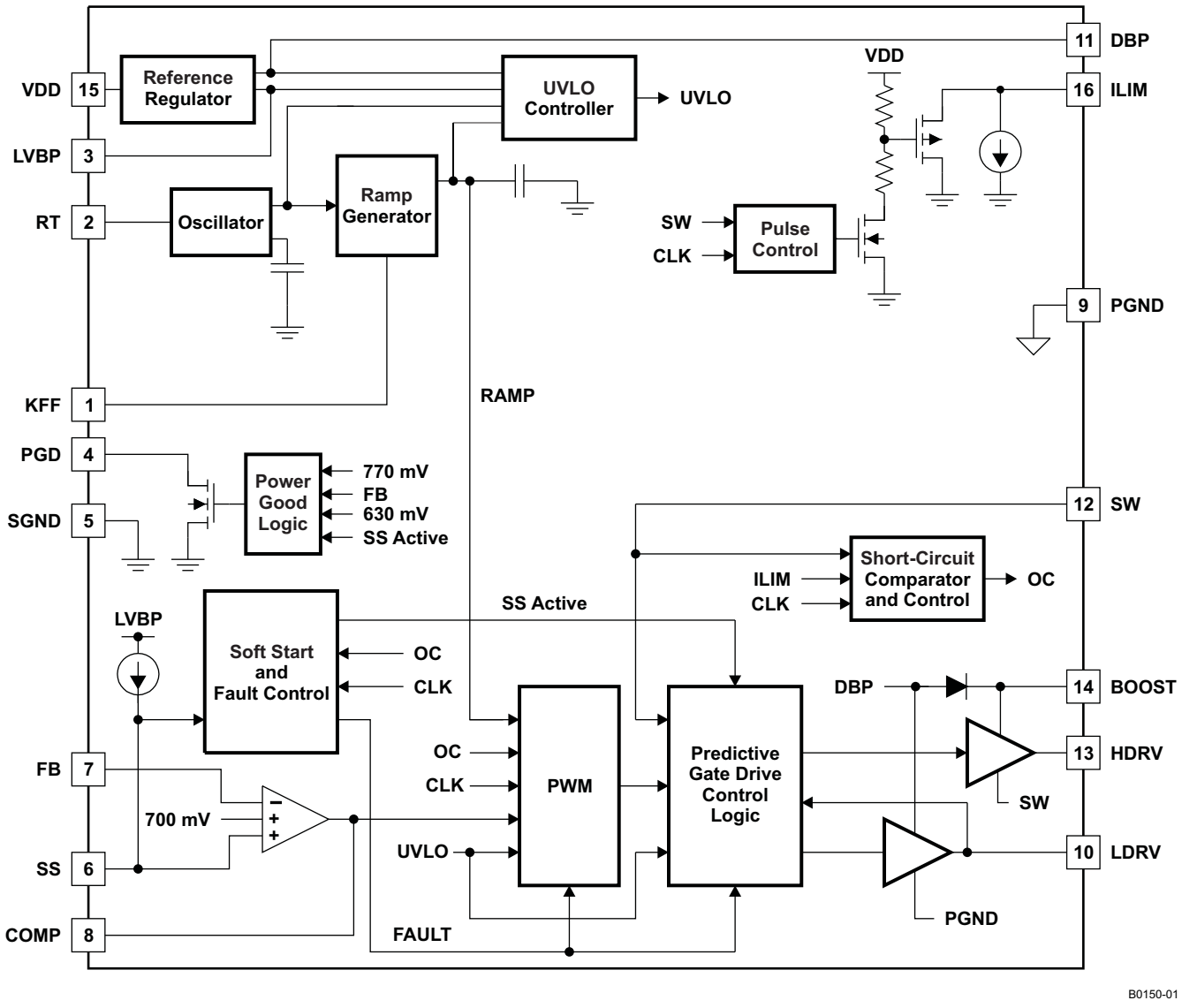
(1) For more information on the PWP package, see the *PowerPAD Thermally Enhanced Package* technical brief (SLMA002).

DEVICE INFORMATION (continued)

Table 1. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOST	14	I	The peak voltage on BOOST is equal to the SW node voltage plus the voltage present at DBP less the bootstrap diode drop. This drop can be 1.4 V for the internal bootstrap diode or 300 mV for an external Schottky diode. The voltage differential between this pin and SW is the available drive voltage for the high-side FET.
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the FB pin to compensate the overall loop. The COMP pin is internally clamped to 3.4 V.
DBP	11	O	8-V reference used for the gate drive of the N-channel synchronous rectifier. This pin should be bypassed to ground with a 1-μF ceramic capacitor.
FB	7	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage, 0.7 V.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Short-circuit-protection programming pin. This pin is used to set the short circuit detection threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VDD. The voltage on this pin is compared to the voltage drop ($V_{VDD} – V_{SW}$) across the high side N-channel MOSFET during conduction. Just prior to the beginning of a switching cycle this pin is pulled to approximately VDD/2 and released when SW is within 2 V of V_{DD} or after a timeout (the precondition time), whichever occurs first. Placing a capacitor across the resistor from ILIM to VDD allows the ILIM threshold to decrease during the switch-on time, effectively programming the ILIM blanking time. See *Application Information*.
KFF	1	I	A resistor is connected from this pin to VIN programs the amount of feed-forward voltage. The current fed into this pin is internally divided by 25 and used to control the slope of the PWM ramp and program undervoltage lockout. Nominal voltage at this pin is maintained at 400 mV.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from DBP (MOSFET on) to ground (MOSFET off). For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50 nC.
LVBP	3	O	4.2-V reference used for internal device logic only. This pin should be bypassed by a 0.1-μF ceramic capacitor. External loads that are less than 1 mA and electrically quiet may be applied.
PGD	4	O	This is an open drain output that pulls to ground when soft start is active, or when the FB pin is outside a ±10% band around VREF.
PGND	9		Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5		Signal ground reference for the device. Low-level quiet circuitry around the IC should connect to this pin. This pin should be connected to the thermal pad under the IC, and that thermal pad should connect to the PGND pin. Do not allow power currents to flow in the thermal pad or in the SGND part of the ground for best results.
SS	6	I	Soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 12 μA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The voltage at this error amplifier input is approximately 1 V less than that on the SS pin. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal offset voltage of 1 V plus the internal reference voltage of 700 mV. I fSS is pulled below 225mV, the device goes into a shutdown state where the power FETSs are turned off and the prebias circuitry is reset. If the programmed UVLO voltage is below 6V, connect a 330kΩ resistor in parallel with the SS capacitor. Also provides timing for fault recovery attempts.
SW	12	I	This pin is connected to the switched node of the converter. It is used for short-circuit sensing and gate-drive timing information and is the return for the high side driver. A 1.5-Ω resistor is required in series with this pin for protection against substrate current issues.
VDD	15	I	Supply voltage for the device.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40077 allows the user to construct synchronous voltage-mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive gate-drive circuitry optimizes switching delays for increased efficiency and improved converter output-power capability. Voltage feed-forward is employed to ease loop compensation for wide-input-range designs and provide better line transient response.

The TPS40077 incorporates circuitry to allow startup into a preexisting output voltage without sinking current from the source of the preexisting output voltage. This avoids damaging sensitive loads at start-up. The controller can be synchronized to an external clock source or can free-run at a user-programmable frequency. An integrated power-good indicator is available for logic (open-drain) output of the condition of the output of the converter.

MINIMUM PULSE DURATION

The TPS40077 devices have limitations on the minimum pulse duration that can be used to design a converter. Reliable operation is assured for nominal pulse durations of 150 ns and above. This places some restrictions on the conversion ratio that can be achieved at a given switching frequency. Figure 14 shows minimum output voltage for a given input voltage and frequency.

SLEW RATE LIMIT ON VDD

The regulator that supplies power for the drivers on the TPS40077 requires a limited rising slew rate on VDD for proper operation if the input voltage is above 10 V. If the slew rate is too great, this regulator can overshoot and damage to the part can occur. To ensure that the part operates properly, limit the slew rate to no more than 0.12 V/µs as the voltage at VDD crosses 8 V. If necessary, an R-C filter can be used on the VDD pin of the device. Connect the resistor from the VDD pin to the input supply of the converter. Connect the capacitor from the VDD pin to PGND. There should not be excessive (more than a 200-mV) voltage drop across the resistor in normal operation. This places some constraints on the R-C values that can be used. Figure 22 is a schematic fragment that shows the connection of the R-C slew rate limit circuit. Equation 1 and Equation 2 give values for R and C that limits the slew rate in the worst case condition.

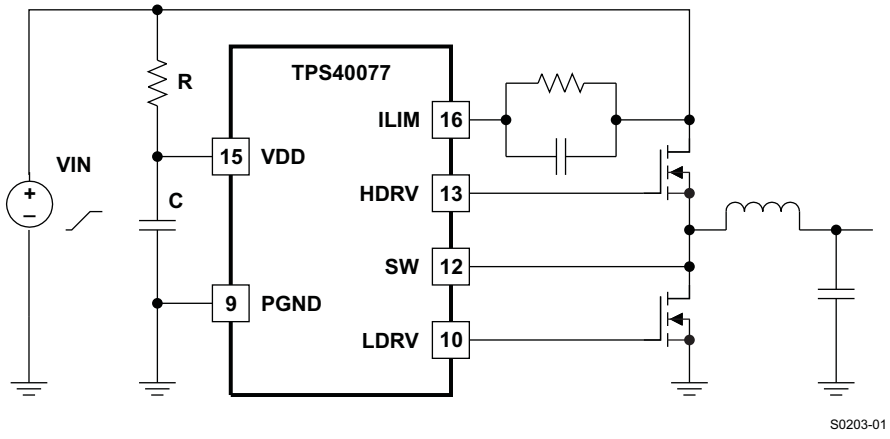


Figure 22. Limiting the Slew Rate

APPLICATION INFORMATION (continued)

$$C > \frac{V_{IN} - 8\ V}{R \times SR} \quad (1)$$

$$R < \frac{0.2\ V}{f_{SW} \times Q_{g(TOT)} + I_{DD}} \quad (2)$$

where

- V_{VIN} is the final value of the input voltage ramp
- f_{SW} is the switching frequency
- $Q_{g(TOT)}$ is the combined total gate charge for both upper and lower MOSFETs (from MOSFET data sheet)
- I_{IDD} is the TPS40077 input current (3.5 mA maximum)
- SR is the maximum allowed slew rate [12×10^4] (V/s)

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40077 has independent clock oscillator and PWM ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. Connecting a single resistor from RT to ground sets the switching frequency of the clock oscillator. The clock frequency is related to R_T by:

$$R_T = \left(\frac{1}{f_{SW}(kHz) \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \quad (3)$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT AND UVLO

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations, because the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 23).

The PWM ramp must reach approximately 1 V in amplitude during a clock cycle, or the PWM is not allowed to start. The PWM ramp time is programmed via a single resistor (R_{KFF}) connected from KFF VDD. R_{KFF}, V_{START}, and R_T are related by (approximately):

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^{\ 2} + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2 \quad (4)$$

where

- R_T and R_{KFF} are in kΩ
- $V_{UVLO(on)}$ is in V

This yields typical numbers for the programmed startup voltage. The minimum and maximum values may vary up ±15% from this number. Figure 16 through Figure 18 show the typical relationship of $V_{UVLO(on)}$, $V_{UVLO(off)}$ and R_{KFF} at three common frequencies.

The programmable UVLO circuit incorporates 20% hysteresis from the start voltage to the shutdown voltage. For example, if the startup voltage is programmed to be 10 V, the controller starts when V_{DD} reaches 10 V and shuts down when V_{DD} falls below 8 V. The maximum duty cycle begins to decrease as the input voltage rises to twice the startup voltage. Below this point, the maximum duty cycle is as specified in the electrical table. Note that with this scheme, the theoretical maximum output voltage that the converter can produce is approximately two times the programmed startup voltage. For design, set the programmed startup voltage equal to or greater than the desired output voltage divided by maximum duty cycle (85% for frequencies 500 kHz and below). For example, a 5-V output converter should not have a programmed startup voltage below 5.9 V. Figure 23 shows the theoretical maximum duty cycle (typical) for various programmed startup voltages

APPLICATION INFORMATION (continued)

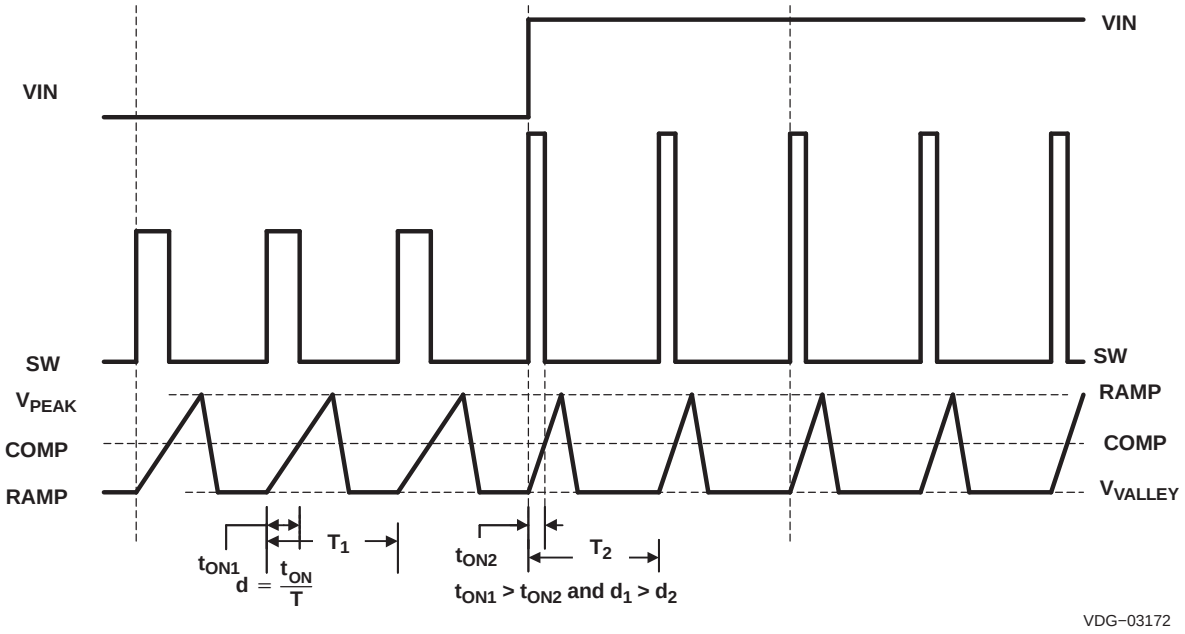


Figure 23. Voltage Feed-Forward and PWM Duty Cycle Waveforms

PROGRAMMING SOFT START

TPS40077 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by connecting an external capacitor (C_{SS}) from the SS pin to GND. This capacitor is charged by a fixed current, generating a ramp signal. The voltage on SS is level-shifted down approximately 1 V and fed into a separate noninverting input to the error amplifier. The loop is closed on the lower of the level shifted SS voltage or the 700-mV internal reference voltage. Once the level-shifted SS voltage rises above the internal reference voltage, output-voltage regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage, the soft-start time should be greater than the L-C_{OUT} time constant or:

$$t_{START} \geq 2\pi \times \sqrt{L \times C_{OUT}} \quad (5)$$

Note that there is a direct correlation between t_{START} and the input current required during start-up. The lower t_{START} is, the higher the input current required during start-up, because the output capacitance must be charged faster. For a desired soft-start time, the soft-start capacitance, C_{SS}, can be found from:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{FB}} \quad (6)$$

APPLICATION INFORMATION (continued)

PROGRAMMING SHORT-CIRCUIT PROTECTION

The TPS40077 uses a two-tier approach for short-circuit protection. The first tier is a pulse-by-pulse protection scheme. Short-circuit protection is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when its gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor (R_{ILIM}) connected from V_{VDD} to the ILIM pin when driven by a constant-current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated. This is illustrated in Figure 24.

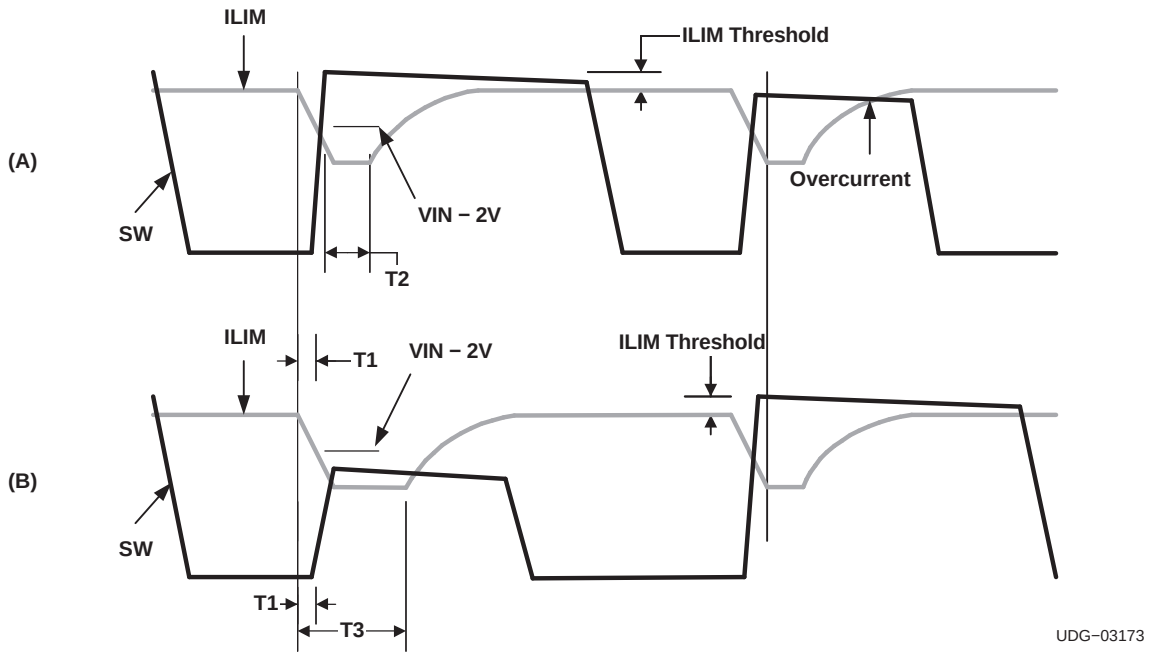


Figure 24. Switching and Current Limit Waveforms and Timing Relationship

In addition, just prior to the high-side MOSFET turning on, the ILIM pin is pulled down to approximately half of V_{VDD}. The ILIM pin is allowed to return to its nominal value after one of two events occur. If the SW node rises to within approximately 2 V of V_{VDD}, the device allows ILIM to go back to its nominal value. This is illustrated in Figure 24(A). T1 is the delay time from the internal PWM signal being asserted and the rise of SW. This includes a driver delay of 50 ns, typical. T2 is the reaction time of the sensing circuit that allows ILIM to start to return to its nominal value, typically 20 ns. The second event that can cause ILIM to return to its nominal value is for an internal timeout to expire. This is illustrated in Figure 24(B) as T3. Here SW never rises to V_{VDD} – 2 V, for whatever reason, and the internal timer times out, releasing the ILIM pin.

Prior to ILIM starting back to its nominal value, overcurrent sensing is not enabled. In normal operation, this ensures that the SW node is at a higher voltage than ILIM when overcurrent sensing starts, avoiding false trips while allowing for a quicker blanking delay than would ordinarily be possible. Placing a capacitor across R_{ILIM} sets an exponential approach to the normal voltage at the ILIM pin. This exponential decay of the overcurrent threshold can be used to compensate for ringing on the SW node after its rising edge and to help compensate for slower turn-on FETs. Choosing the proper capacitance requires care. If the capacitance is too large, the voltage at ILIM does not approach the desired overcurrent level quickly enough, resulting in an apparent shift in overcurrent threshold as pulse duration changes. As a general rule, it is best to make the time constant of the R-C at the ILIM pin 0.2 times or less of the nominal pulse duration of the converter as shown in Equation 11.

Also, the comparator that uses ILIM and SW to determine if an overcurrent condition exists has a clamp on its SW input. This clamp makes the SW node never appear to fall more than 1.4 V (approximately, could be as much as 2 V at –40°C) below V_{VDD}. When ILIM is more than 1.4 V below V_{VDD}, the overcurrent circuit is effectively disabled.

APPLICATION INFORMATION (continued)

The second-tier protection incorporates a fault counter. The fault counter is incremented on each cycle with an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7), a fault condition is declared by the controller. When this happens, the outputs are placed in a state defined in Table 2. Seven soft-start cycles are initiated (without activity on the HDRV and LDRV outputs) and the PWM is disabled during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled and the controller attempts to restart. If the fault has been removed, the output starts up normally. If the output is still present, the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. Refer to Figure 25 for typical fault-protection waveforms.

The minimum short-circuit limit setpoint ($I_{SCP(min)}$) depends on t_{START}, C_{OUT}, V_{OUT}, ripple current in inductor (I_{RIPPLE}) and the load current at turn-on (I_{LOAD}).

$$I_{SCP(min)} > \left(\frac{C_{OUT} \times V_{OUT}}{t_{START}}\right) + I_{LOAD} + \left(\frac{I_{RIPPLE}}{2}\right) \quad (7)$$

The short-circuit limit programming resistor (R_{ILIM}) is calculated from:

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(onMAX)} + V_{ILIM\ (offset)}}{I_{ILIM}}\ \Omega \quad (8)$$

where

- I_{ILIM} is the current into the ILIM pin (110 μA, typical)
- $V_{ILIM(offset)}$ is the offset voltage of the ILIM comparator (–50 mV, typical)
- I_{SCP} is the short-circuit protection current

To find the range of the overcurrent values, use the following equations:

$$I_{SCP(max)} = \frac{1.09 \times I_{ILIM(max)} \times R_{ILIM} - 0.09 \times R_{VDD} \times I_{R_{VDD}} - 0.045\ V + 75\ mV}{R_{DS(ON)min}}\ (A) \quad (9)$$

$$I_{SCP(min)} = \frac{1.09 \times I_{ILIM(min)} \times R_{ILIM} - 0.09 \times R_{VDD} \times I_{R_{VDD}} - 0.045\ V + 30\ mV}{R_{DS(ON)max}}\ (A) \quad (10)$$

The TPS40077 provides short-circuit protection only. Therefore, it is recommended that the minimum short-circuit protection level be placed at least 20% above the maximum output current required from the converter. The maximum output of the converter should be the steady state maximum output plus any transient specification that may exist.

The ILIM capacitor maximum value can be found from:

$$C_{ILIM(max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_{SW}}\ (Farads) \quad (11)$$

Note that this is a recommended maximum value. If a smaller value can be used, it should be. For most applications, consider using half the maximum value above.

APPLICATION INFORMATION (continued)

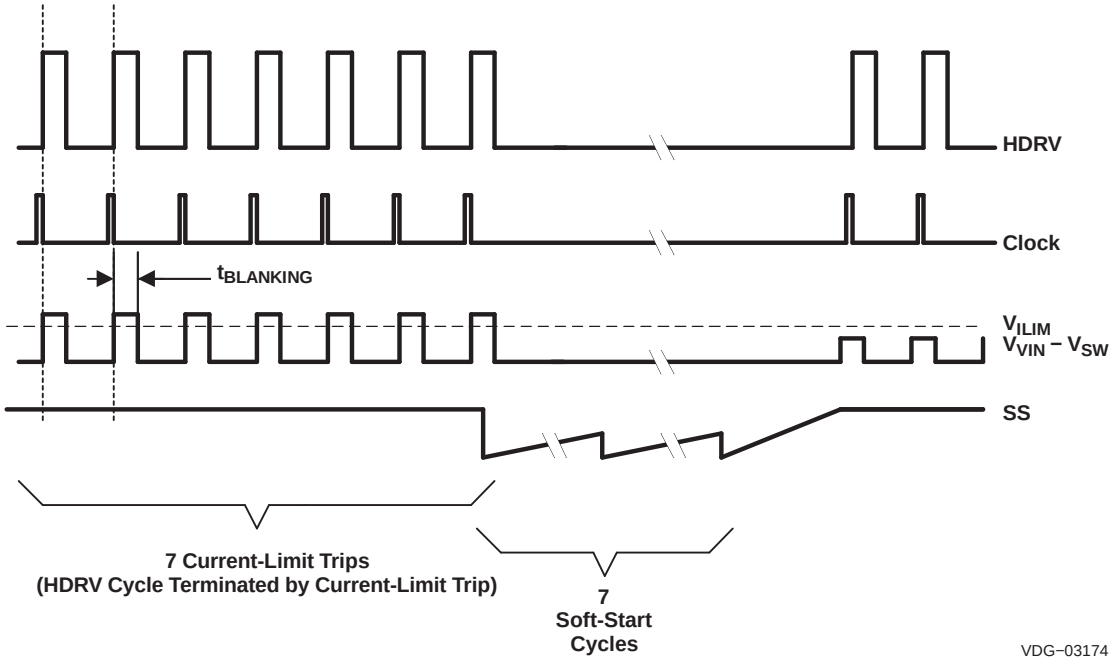


Figure 25. Typical Fault Protection Waveforms

LOOP COMPENSATION

Voltage-mode, buck-type converters are typically compensated using Type III networks. Becausce the TPS40077 uses voltage feed-forward control, the gain of the voltage feed-forward circuit must be included in the PWM gain. The gain of the voltage feed-forward circuit, combined with the PWM circuit and power stage for the TPS40077 is:

$$K_{PWM} \cong V_{UVLO(on)}$$

The remainder of the loop compensation is performed as in a normal buck converter. Note that the voltage feed-forward circuitry removes the input voltage term from the expression for PWM gain. PWM gain is strictly a function of the programmed startup voltage.

SHUTDOWN AND SEQUENCING

The TPS40077 can be shut down by pulling the SS pin below 250 mV. In this state, both of the output drivers are in the low-output state, turning off both of the power FETs. This places the output of the converter in a high-impedance state. When shutting down the converter, a crisp pulldown of the SS pin is preferred to a slow pulldown. A slow pulldown could allow the output to be pulled low, possibly sinking current from the load. As a general rule of thumb, the fall time of SS when shutting down the converter should be no more than 1/10th of the control loop crossover frequency. An example of a shutdown interface is shown in Figure 26.

APPLICATION INFORMATION (continued)

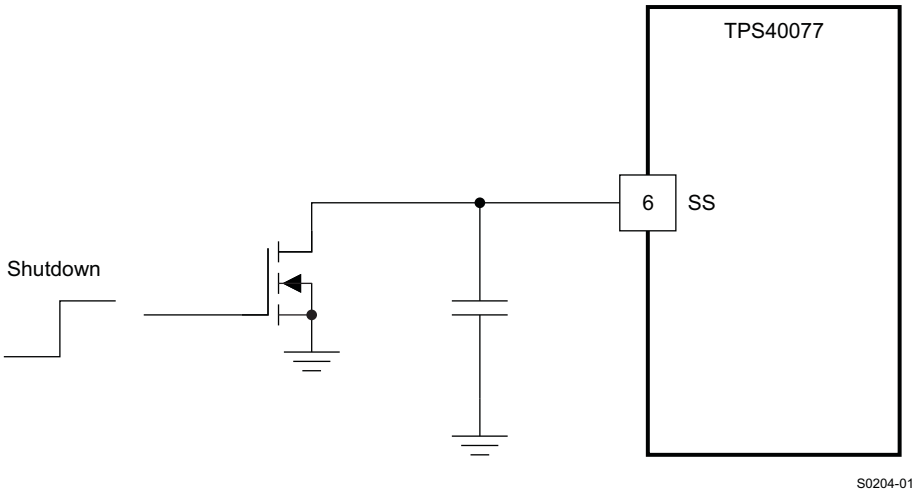


Figure 26. TPS40077 Shutdown

In a similar manner, power supplies based on the TPS40077 can be sequenced by connecting the PGD pin of the first supply to come up to the SS pin of the second supply as shown in Figure 27.

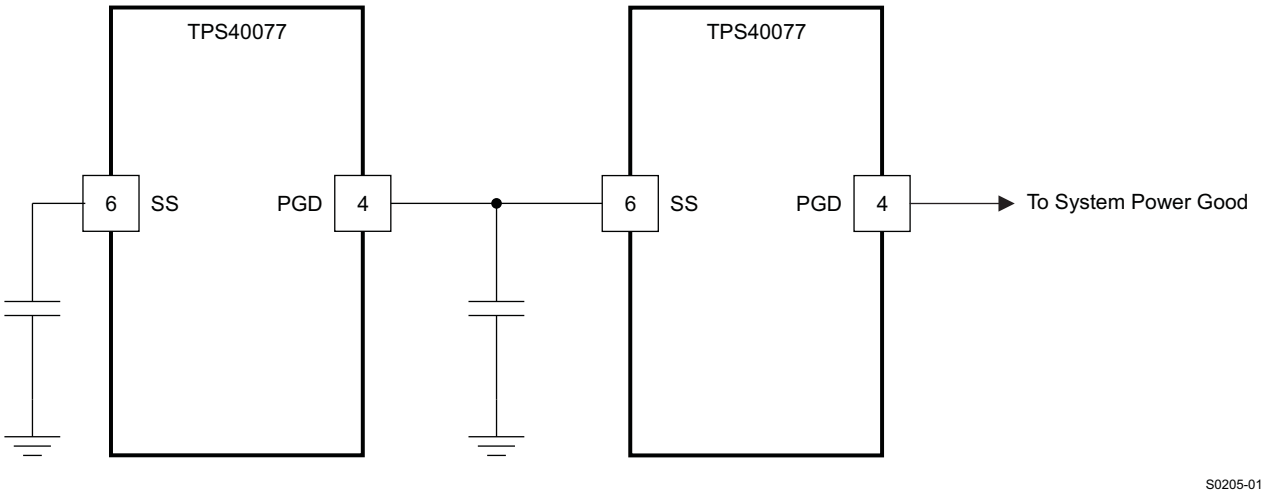


Figure 27. TPS40077 Sequencing

BOOST AND LVBP BYPASS CAPACITANCE

The BOOST capacitance provides a local, low-impedance flying source for the high-side driver. The BOOST capacitor should be a good-quality, high-frequency capacitor. A capacitor with a minimum value of 100-nF is suggested.

The LVBP pin must provide energy for both the synchronous MOSFET and the high-side MOSFET (via the BOOST capacitor). The suggested value for this capacitor is 1-µF ceramic, minimum.

APPLICATION INFORMATION (continued)

INTERNAL REGULATORS

The internal regulators are linear regulators that provide controlled voltages for the drivers and the internal circuitry to operate from. The DBP pin is connected to a nominal 8-V regulator that provides power for the driver circuits to operate from. This regulator has two modes of operation. At V_{DD} voltages below 8.5 V, the regulator is in a low-dropout mode of operation and tries to provide as little impedance as possible from VDD to DBP. Above 10 V at V_{DD}, the regulator regulates DBP to 8 V. Between these two voltages, the regulator remains in the state it was in when V_{DD} entered this region (see Figure 20). Small amounts of current can be drawn from this pin for other circuit functions, as long as power dissipation in the controller device remains at acceptable levels and junction temperature does not exceed 125°C.

The LVBP pin is connected to another internal regulator that provides 4.2-V (nom) for the operation of low-voltage circuitry in the controller. This pin can be used for other circuit purposes, but extreme care must be taken to ensure that no extra noise is coupled onto this pin, since controller performance suffers. Current draw is not to exceed 1 mA. See Figure 21 for typical output voltage at this pin.

TPS40077 POWER DISSIPATION

The power dissipation in the TPS40077 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance) can be calculated from:

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts/driver)}$$

where V_{DR} is the driver output voltage

The total power dissipation in the TPS40077, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in Equation 14 or Equation 15.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{14}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{15}$$

where I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the TPS40077 PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air assuming 2-oz. copper trace and thermal pad with solder and no air flow is 37°C/W. See the application report titled *PowerPAD Thermally Enhanced Package* (SLMA002) for detailed information on PowerPAD package mounting and usage.

The maximum allowable package power dissipation is related to ambient temperature by Equation 16. For θ_{JA}, see the Package Dissipation Ratings table.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad \text{(Watts)} \tag{16}$$

Substituting Equation 16 into Equation 15 and solving for f_{SW} yields the maximum operating frequency for the TPS40077. The result is described in Equation 17.

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})}\right] - I_Q\right)}{(2 \times Q_g)} \quad \text{(Hz)} \tag{17}$$

APPLICATION INFORMATION (continued)

BOOST DIODE

The TPS40077 series has internal diodes to charge the boost capacitor connected from SW to BOOST. The drop across these diodes is rather large, 1.4 V nominal, at room temperature. If this drop is too large for a particular application, an external diode may be connected from DBP (anode) to BOOST (cathode). This provides significantly improved gate drive for the high-side FET, especially at lower input voltages.

GROUNDING AND BOARD LAYOUT

The TPS40077 provides separate signal ground (SGND) and power ground (PGND) pins. Care should be given to proper separation of the circuit grounds. Each ground should consist of a plane to minimize its impedance, if possible. The high-power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (DBP), and the input capacitor should be connected to PGND plane.

Sensitive nodes such as the FB resistor divider and RT should be connected to the SGND plane. The SGND plane should only make a single-point connection to the PGND plane. It is suggested that the SGND pin be tied to the copper area for the thermal pad underneath the chip. Tie the PGND to the thermal-pad copper area as well, and make the connection to the power circuit ground from the PGND pin. Reference the output voltage divider to the SGND pin.

Component placement should ensure that bypass capacitors (LVPB and DBP) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW). Failure to follow careful layout practices results in suboptimal operation. More detailed information can be found in the TPS40077EVM User's Guide (SLUUxxx).

SYNCHRONOUS RECTIFIER CONTROL

Table 2 describes the state of the rectifier MOSFET control under various operating conditions.

Table 2. Synchronous Rectifier MOSFET States

SYNCHRONOUS RECTIFIER OPERATION DURING			
SOFT-START	**NORMAL**	**FAULT (FAULT RECOVERY IS SAME AS SOFT-START)**	**OVERVOLTAGE**
Off until first high-side pulse is detected, then on when high-side MOSFET is off	Turns off at the start of a new cycle. Turns on when the high-side MOSFET is turned off	OFF	Turns OFF only at start of next cycle only if the pulse width modulator duty cycle is greater than zero. Otherwise, stays ON

For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50 nC.

APPLICATION 1: BUCK REGULATOR 8-V TO 16-V INPUT, 1.8-V OUTPUT AT 10 A

Table 3. Specifications

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNITS
INPUT CHARACTERSTICS						
V_{IN}	Input voltage		8	12	16	V
I_{IN}	Input current	V_{IN} = NOM, I_{OUT} = MAX		1.8	2	A
	No-load input current	V_{IN} = NOM, I_{OUT} = 0 A		62.6	3.6	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = MIN to MAX	5.4	6	6.6	V
V_{IN_ONV}	Input ONV	I_{OUT} = MIN to MAX	6.3	7	7.7	V
OUTPUT CHARACTERSTICS						
V_{OUT}	Output voltage	V_{IN} = NOM, I_{OUT} = NOM	1.75	1.8	1.85	V
	Line regulation(1)	V_{IN} = MIN to MAX, I_{OUT} = NOM			0.5%	
	Load regulation(1)	V_{IN} = NOM, I_{OUT} = MIN to MAX			0.5%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = NOM, I_{OUT} = MAX			100	mVpp
I_{OUT}	Output current	V_{IN} = MIN to MAX	0	5	10	A
I_{OCP}	Output overcurrent inception point	V_{IN} = NOM, V_{OUT} = V_{OUT} – 5%	12.25	19.4	34	A
V_{OVP}	Output OVP	I_{OUT} = MIN to MAX	NA	NA	NA	
Transient response						
ΔI	Load step	I_{OUT_Max} to 0.2 × I_{OUT_Max}		8		A
	Load slew rate			10		A/µs
	Overshoot			200		mV
	Settling time			1		ms
SYSTEM CHARACTERSTICS						
f_{SW}	Switching frequency		240	300	360	kHz
η_{pk}	Peak efficiency	V_{IN} = NOM, I_{OUT} = MIN to MAX		90%		
η	Full-load efficiency	V_{IN} = NOM, I_{OUT} = MAX		90%		
T_{op}	Operating temperature range	V_{IN} = MIN to MAX, I_{OUT} = MIN to MAX	–40	25	85	°C
MECHANICAL CHARACTERSTICS						
L	Width			2		Inches
W	Length			3		Inches
h	Component height			0.41		Inch

(1) Voltage accuracy is dependent on resistor tolerance and reference accuracy. Line and load regulation are calculated with respect to the actual set point voltage.

Schematic and Performance Curves

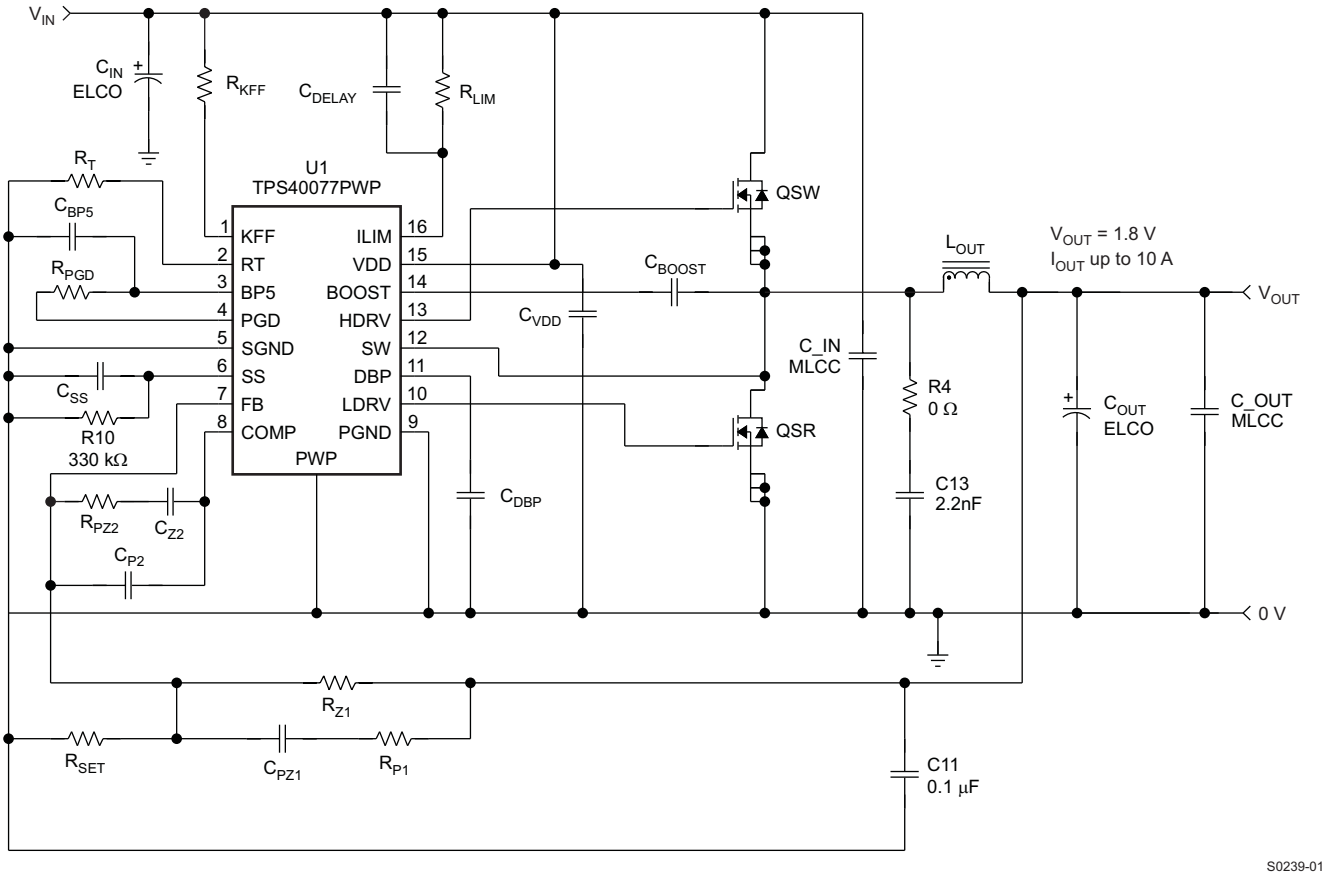


Figure 28. Schematic Diagram

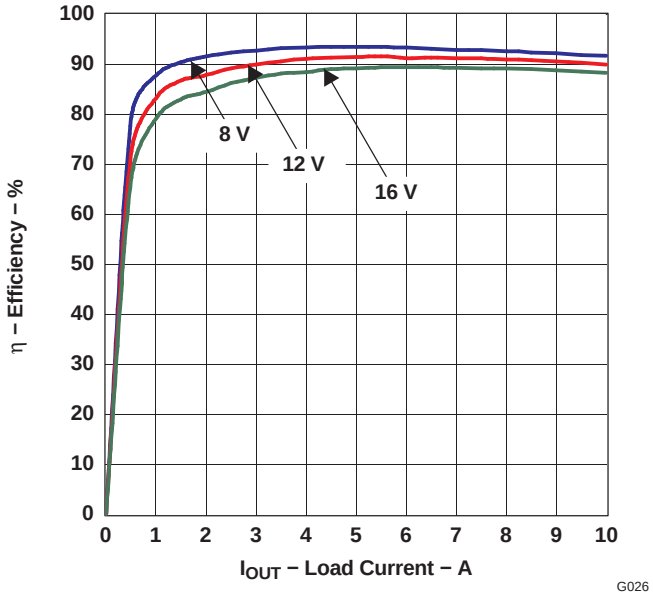


Figure 29. Module Efficiency, 8 V, 12 V, and 16 V In, 0 to 10 A Out

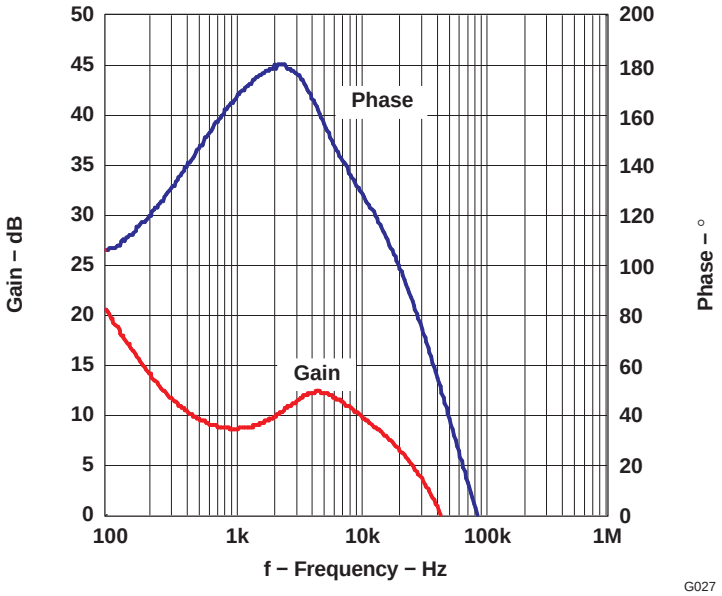


Figure 30. Bode Plot Showing 57° Phase Margin at Crossover Frequency of 54 kHz

Component Selection

Power Train Components

Output Inductor, LOUT

The output inductor is one of the most important components to select. It stores the energy necessary to keep the output regulated when the switch FET is turned off. The value of the output inductor dictates the peak and RMS currents in the converter. These currents are important when selecting other components. Equation (1) can be used to calculate a value for LOUT for this module which operates at a switching frequency (f) of 300 kHz.

$$LOUT = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{f_s \times I_{RIPPLE}} \quad (18)$$

I_{RIPPLE} is the allowable ripple in the inductor.. Select I_{RIPPLE} to be between 20% and 30% of maximum I_{OUT}. For this design I_{RIPPLE} of 2.5A was selected. Calculated LOUT is 2.13µ H. A standard inductor with value of 2.5 H was chosen. This will reduce I_{RIPPLE} by about 17% to 2.07 A.

This I_{RIPPLE} value can be used calculate the rms and peak current flowing in LOUT. Note that this peak current is also seen by the switching FET and synchronous rectifier.

$$I_{LOUT\_RMS} = \sqrt{I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}} = 10.02 \text{ A} \quad (19)$$

The power loss from the selected inductor DCR is 357 mW. The ac core loss for this Coilcraft inductor may be found from the Coilcraft web site, where there is a loss calculator. The loss is 179 mW.

$$I_{PK} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 11.03 \text{ A} \quad (20)$$

The inductor is selected with a saturation current higher than this current plus the current that is developed charging the output capacitance during the soft-start interval.

Output Capacitor, COUT, ELCO and MLCC

Several parameters must be considered when selecting the output capacitor. The capacitance value should be selected based on the output overshoot, V_{OVER}, and undershoot, V_{UNDER}, during a transient load, I_{STEP}, on the converter. The equivalent series resistance (ESR) is chosen to allow the converter meet the output ripple specification, V_{RIPPLE}. The voltage rating must be greater than the maximum output voltage. Another parameter to consider is equivalent series inductance, which is important in fast-transient load situations. Also, size and technology can be factors when choosing the output capacitor. In this design, a large-capacitance electrolytic type capacitor, COUT ELCO, is used to meet the overshoot and undershoot specifications. Its ESR is chosen to meet the output ripple specification. Smaller multiple-layer ceramic capacitors, COUT MLCC, are used to filter high-frequency noise.

The minimum required capacitance and maximum ESR can be calculated using the following equations.

$$COUT = \frac{LOUT \times I_{STEP}^{2}}{2 \times V_{UNDER} \times D_{max} \times (V_{IN} - V_{OUT})} \quad (21)$$

$$COUT = \frac{LOUT \times I_{STEP}^{2}}{2 \times V_{OVER} \times V_{OUT}} \quad (22)$$

$$ESR = \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (23)$$

From Equation 21, Equation 22, and Equation 23, the capacitance for COUT should be greater than 444 µF, and its ESR should be less than 12 mΩ. The 470-µF/6.3-V capacitor from Panasonic's FC series was chosen. Its ESR is 160 mΩ. MLCCs of 47 µF and 22 µF/16 V are also added in parallel to achieve the required ESR and to reduce high-frequency noise.

Input Capacitor, CIN ELCO and MLCC

The input capacitor is selected to handle the ripple current of the buck stage. Also a relatively large capacitance is used to keep the ripple voltage on the supply line low. This is especially important where the supply line has high impedance. It is recommended however, that the supply line impedance be kept as low as possible.

The input capacitor ripple current can be calculated using Equation 24.

$$I_{CAP(RMS)} = \sqrt{\left[\left(I_{OUT} - I_{IN(AVG)}\right)^{2} + \frac{I_{RIPPLE}^{2}}{12}\right] \times D + I_{IN(AVG)}^{2} \times (1 - D)} \quad (24)$$

$I_{IN(AVG)}$ is the average input current. This is calculated simply by multiplying the output dc current by the duty cycle. The ripple current in the input capacitor is 3.3 A. An 1812 MLCC using X5R material has a typical dissipation factor of 5%. For a 22 µF capacitor at 300 kHz, the ESR is approximately 4 mΩ. Two capacitors are used in parallel, so the power dissipation in each capacitor is less than 11 mW.

A 470-µF/16-V electrolytic is added to maintain the voltage on the input rail.

Switching MOSFET, QSW

The following key parameters must be met by the selected MOSFET.

- Drain source voltage, V_{ds}, must be able to withstand the input voltage plus spikes that may be on the switching node. For this design a V_{ds} rating of 30 volts is recommended.
- Drain current, I_D, at 25 C, must be greater than that calculated using Equation 25.

$$I_{QSW(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \left[I_{OUT(MAX)}^{2} + \frac{I_{RIPPLE}^{2}}{12}\right]} \quad (25)$$

- With the parameters specified the calculation of I_{qsw}(RMS) should be greater than 5 A.
- Gate source voltage, V_{gs}, must be able to withstand the gate voltage from the control IC. For the TPS40077 this is 11V.

Once the above boundary parameters are defined the next step in selecting the switching MOSFET is to select the key performance parameters. Efficiency will be the performance characteristic which will drive the other selection criteria. Target efficiency for this design is 90%. Based on 1.8V output and 10A this equates to a power loss in the converter of 1.8W. Based on this figure a target of 0.6W dissipated in the switching FET was chosen.

The following equations can be used to calculate the power loss, P_{QSW}, in the switching MOSFET.

$$P_{QSW} = P_{CON} + P_{SW} + P_{GATE} \tag{26}$$

$$P_{CON} = R_{DS(on)} \times I_{QSW(RMS)}^{2} = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left[I_{out}^{2} + \frac{I_{RIPPLE}^{2}}{12} \right] \tag{27}$$

$$P_{SW} = V_{IN} \times f_S \times \left[\frac{\left(I_{OUT} + \frac{I_{RIPPLE}}{2} \right) \times \left(Q_{gs1} + Q_{gd} \right)}{I_g} + \frac{Q_{OSS(SW)} + Q_{OSS(SR)}}{12} \right] \tag{28}$$

$$P_{GATE} = Q_{g(TOT)} \times V_g \times f_{SW} \tag{29}$$

where

P_{CON} = conduction losses
P_{SW} = switching losses
P_{GATE} = gate-drive losses
Q_{gd} = drain-source charge or Miller charge
Q_{gs1} = gate-source post-threshold charge
I_g = gate-drive current
$Q_{OSS(SW)}$ = switching MOSFET output charge
$Q_{OSS(SR)}$ = synchronous MOSFET output charge
$Q_{g(TOT)}$ = total gate charge from zero volts to the gate voltage
V_g = gate voltage

If the total estimated loss is split evenly between conduction and switching losses, Equation 27 and Equation 28 yield preliminary values for $R_{DS(on)}$ and (Q_{gs1} + Q_{gd}). Note output losses due to Q_{OSS} and gate losses have been ignored here. Once a MOSFET is selected these parameters can be added.

The switching MOSFET for this design should have an $R_{DS(on)}$ of less than 8 mμ. The sum of Q_{gd} and Q_{gs} should be approximately 4 nC.

It may not always be possible to get a MOSFET which meets both these criteria, so a compromise may be necessary. Also, by selecting different MOSFETs close to these criteria and calculating power loss, the final selection can be made. It was found that the Si7860DP MOSFET from Vishay semiconductor gave reasonable results. This device has an $R_{DS(on)}$ of 8 mΩ and a (Q_{gs1} + Q_{gd}) of 5 nC. The estimated conduction losses are 0.115 W and the switching losses are 0.276 W. This gives a total estimated power loss of 0.391 W versus 0.6 W for our initial boundary condition. Note this does not include gate losses of approximately 71 mW and output losses of 20 mW.

Rectifier MOSFET, QSR

Similar criteria to the foregoing can be used for the rectifier MOSFET. There is one significant difference, due to the body diode conducting the rectifier MOSFET switches with zero voltage across its drain and source, so effectively with zero switching losses. However, there are some losses in the body diode. These are minimized by reducing the delay time between the transition from the switching MOSFET turnoff to rectifier MOSFET turnon and vice-versa. The TPS40077 incorporates TI's proprietary predictive gate drive (PGD), which helps reduce these delays to around 10 ns.

The equations used to calculate the losses in the rectifier MOSFET are:

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE} \tag{30}$$

$$P_{CON} = R_{DS(on)} \times \left[1 - \frac{V_{OUT}}{V_{IN}} - (t_1 + t_2) \times f_S\right] \times \left[I_{out}^2 + \frac{I_{RIPPLE}^2}{12}\right] \quad (31)$$

$$P_{BD} = V_f \times I_{OUT} \times (t_1 + t_2) \times f_S \quad (32)$$

$$P_{GATE} = Q_{g(TOTAL)} \times V_g \times \times f_S \quad (33)$$

where

P_{BD} = body diode losses

t_1 = body diode conduction prior to turnon of channel = 12 ns for PGD

t_2 = body diode conduction after turnoff of channel = 12 ns for PGD

V_f = body diode forward voltage

Estimating the body diode losses based on a forward voltage of 1 V gives 0.072 W. The gate losses are unknown at this time, so assume 0.1-W gate losses. This leaves 0.428 W for conduction losses. Using this figure a target $R_{DS(on)}$ of 5 mΩ was calculated.

The Si7336ADP from Vishay was chosen. Using the parameters from its data sheet, the actual expected power losses are calculated. Conduction loss is 0.317 W, body diode loss is 0.072 W and the gate loss is 0.136W. This totals 0.525 W associated with the rectifier MOSFET.

Two other criteria should be verified before finalizing on the rectifier MOSFET. One is the requirement to ensure that predictive gate drive functions correctly. The turnoff delay of the Si7336ADP is 97 ns. The minimum turnoff delay of the Si7860DP is 25 ns. Together these devices meet the 130 ns requirement.

Secondly, the ratio between C_{gs} and C_{gd} should be greater than 1. The SI7836ADP easily meet this criterion. This helps reduce the risk of dv/dt-induced turnon of the rectifier MOSFET. If this is likely to be a problem, a small resistor may be added in series with the boost capacitor, CBOOST.

Component Selection for TPS40077

Timing Resistor, R_T

The timing resistor is calculated using the following equation.

$$R_T = \frac{1}{f_S \times 17.82 \times 10^{-6}} - 23 \quad (34)$$

This gives a resistor value of 165 kΩ. The nominal frequency using this resistor is 300 kHz.

Feed-Forward and UVLO Resistor, R_{KFF}

A resistor connected to the KFF pin of the IC feeds into the ramp generator. This resistor provides current into the ramp generator proportional to the input voltage. The ramp is then adjusted to compensate for different input voltages. This provides the voltage feed-forward feature of the TPS40077.

The same resistor also sets the undervoltage lockout point. The input start voltage should be used to calculate a value for R_{KFF}. For this module, the minimum input voltage is 8 V; however, due to tolerances in the IC, a start voltage of 10% less than the minimum input voltage is selected. The start voltage for R_{KFF} calculation is 7.2 V. Using Equation 35, R_{KFF} can be selected.

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^2 + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2 \quad (35)$$

where R_{KFF} and R_T are in kΩ.

This equation gives an R_{KFF} value of 156 kΩ. The closest lower standard value of 154 kΩ should be selected. This gives a minimum start voltage of 7.1 V.

Soft-Start Capacitor, CSS

It is good practice to limit the rise time of the output voltage. This helps prevent output overshoot and possible damage to the load. The selection of the soft-start time is arbitrary. It must meet one condition: it should be greater than the time constant of the output filter, LOUT and COUT. This time is given by

$$t_{START} \geq 2\pi \times \sqrt{LOUT \times COUT} \tag{36}$$

The soft-start time must be greater than 0.23 ms. A time of 0.750 ms was chosen. This time also helps limit the initial input current during start-up so that the peak current plus the capacitor start-up current is less than the minimum sort circuit current. The value of CSS can be calculated using Equation 37equation (20).

$$C_{SS} = \frac{I_{SS}}{V_{FB}} \times t_{START} \tag{37}$$

A standard 15-nF MLCC capacitor was chosen. The calculated start time using this capacitor is 0.875 ms.

Short-Circuit Protection, R_{ILIM} and C_{ILIM}

Short-circuit protection is programmed using the R_{ILIM} resistor. Selection of this resistor depends on the $R_{DS(on)}$ of the switching MOSFET selected and the required short-circuit current trip point, I_{SCP}. The minimum I_{SCP} is limited by the inductor peak current, the output voltage, the output capacitor, and the soft-start time. Their relationship is given by Equation 38. A short-circuit current trip point greater than that calculated by this equation should be used.

$$I_{SCP} \geq \frac{COUT \times V_{OUT}}{t_{START}} + I_{PK} \tag{38}$$

The minimum short-circuit current trip point for this design is 12.25 A. This value is used in Equation 39 to calculate the minimum R_{ILIM} value.

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(on)MAX} + V_{ILIM(Max)}}{I_{LIM(Min)}} \tag{39}$$

R_{ILIM} is calculated to be 1.17 kΩ, and a 1.2-kΩ resistor is used to verify that the short circuit current requirements are met. The minimum and maximum short-circuit current can be calculated using Equation 40 and Equation 41.

$$I_{SCP(MIN)} = \frac{I_{ILIM(MIN)} \times R_{ILIM(MIN)} - V_{ILIM(MAX)}}{R_{DS(on)MAX}} \tag{40}$$

$$I_{SCP(MAX)} = \frac{I_{ILIM(MAX)} \times R_{ILIM(MAX)} - V_{ILIM(MIN)}}{R_{DS(on)MIN}} \tag{41}$$

where: $V_{ILIM(MAX)}$ and $V_{ILIM(MIN)}$ are maximum and minimum voltages across the high side FET when it is turned on, taking into account temperature variations.

The minimum I_{SCP} is 12.25 A, and the maximum is 34 A.

It is also recommended to add a small capacitor, C_{ILIM}, across R_{ILIM}. The value of this capacitor should be about half the value calculated in Equation 42.

$$C_{ILIM(Max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_S} \tag{42}$$

This equation yields a maximum C_{ILIM} as 55 pF. A smaller value of 27 pF is chosen is chosen.

Boost Voltage, CBOOST and DBOOST (Optional)

To be able to drive an N-channel MOSFET in the switch location of a buck converter, a capacitor charge pump or boost circuit is required. The TPS40077 contains the elements for this boost circuit. The designer must only add a capacitor, CBOOST, from the switch node of the buck power stage to the BOOST pin of the IC. Selection of this capacitor is based on the total gate charge of the switching MOSFET and the allowable ripple on the boost voltage, ΔV_{BOOST}. A ripple of 0.2 V is assumed for this design. Using these two parameters and Equation 43, the minimum value for CBOOST can be calculated.

$$CBOOST > \frac{Q_{g(TOTAL)}}{\Delta V_{BOOST}} \tag{43}$$

The total gate charge of the switching MOSFET is 23 nC. A minimum CBOOST of 0.092 µF is required. A 0.1 µF capacitor was chosen. This capacitor must be able to withstand the maximum input voltage plus the maximum voltage on DBP. This is 13.2 V plus 9.0 V, which is 22.2 V. A 50-V capacitor is used.

To reduce losses in the TPS40077 and to increase the available gate voltage for the switching MOSFET, an external diode can be added between the DBP pin and the BOOST pin of the IC. A small-signal Schottky diode should be used here, such as the BAT54.

Closing the Feedback Loop, R_{Z1}, R_{P1}, R_{PZ2}, R_{SET1}, R_{SET2}, C_{Z2}, C_{P2}, and C_{PZ1}

A graphical method is used to select the compensation components. This is a standard feed-forward buck converter. Its PWM gain is given by Equation 44.

$$K_{PWM} \cong \frac{V_{UVLO}}{1\ V} \tag{44}$$

The ramp voltage is 1 V at the UVLO voltage. Because of the feed-forward compensation, the programmed UVLO voltage is the voltage that sets the PWM gain.

The gain of the output LC filter is given by Equation 45.

$$K_{LC} = \frac{1 + s \times ESR \times COUT}{1 + s \times \frac{LOUT}{ROUT} + s^2 \times LOUT \times COUT} \tag{45}$$

The PWM and LC gain is

$$G_c(s) = K_{PWM} \times K_{LC} \times \frac{V_{UVLO}}{1\ V} \times \frac{1 + s \times ESR \times COUT}{1 + s \times \frac{LOUT}{ROUT} + s^2 \times LOUT \times COUT} \tag{46}$$

To plot this on a Bode plot, the dc gain must be expressed in dB. The dc gain is equal to KPWM. To express this in dB, take its logarithm and multiply by 20. For this converter, the dc gain is

$$DCGAIN = 20 \times \log\left[\frac{V_{UVLO}}{V_{RAMP}}\right] = 20 \times \log(7) = 16.9\ dB \tag{47}$$

Also, the pole and zero frequencies should be calculated. A double pole is associated with the LC and a zero is associated with the ESR of the output capacitor. The frequencies where these occur can be calculated using equations,

$$f_{LC\_Pole} = \frac{1}{2\pi \times \sqrt{LOUT \times COUT}} = 4.3\ kHz \tag{48}$$

$$f_{ESR\_Zero} = \frac{1}{2\pi \times ESR \times COUT} = 2.1\ kHz \tag{49}$$

Plotting these on a Bode plot to get

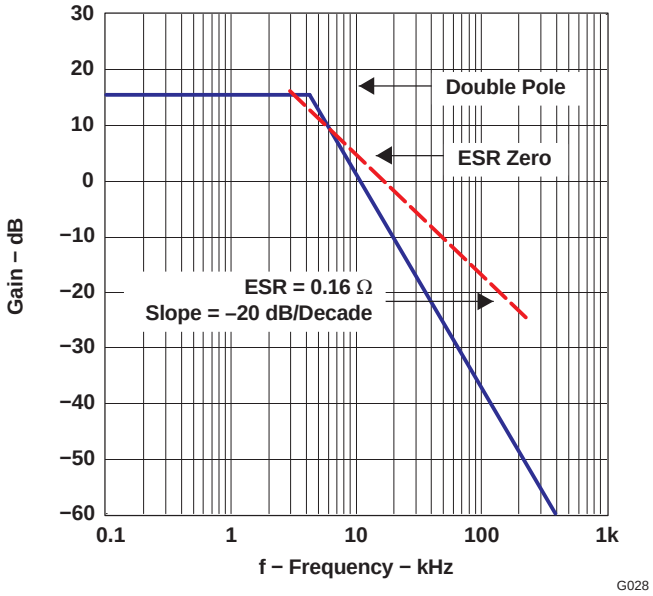


Figure 31. PWM and LC Filter Gain

The next step is to establish the required compensation gain to achieve the desired overall system response. The target response is to have the crossover frequency between 1/9 to 1/5 times the switching frequency, in order to have a phase margin greater than 45° and a gain margin greater than 6 dB.

A type-III compensation network, shown in Figure 32, was used for this design. This network gives the best overall flexibility for compensating the converter.

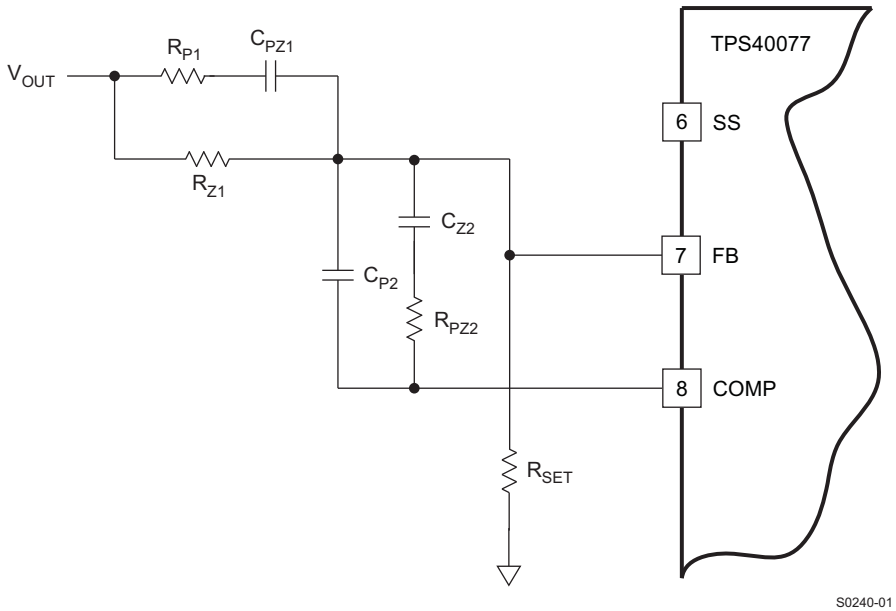


Figure 32. Type-III Compensation With the TPS40077

A typical bode plot for this type of compensation network is shown in Figure 33.

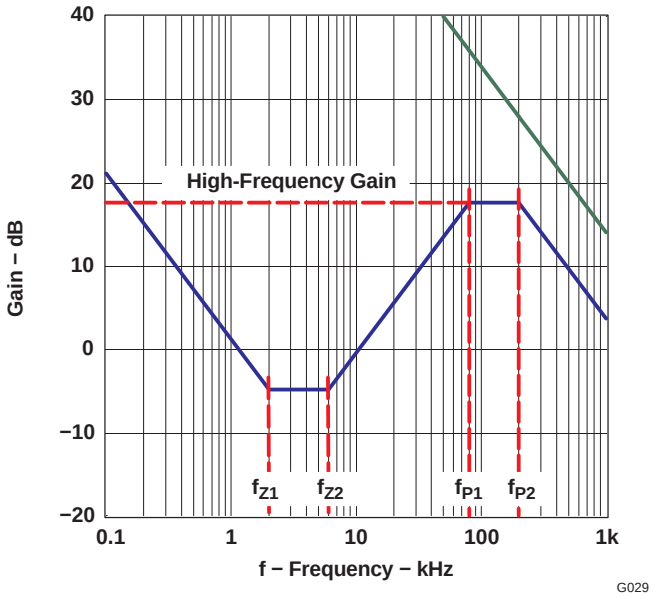


Figure 33. Type-III Compensation Typical Bode Plot

The high-frequency gain and the break (pole and zero) frequencies are calculated using the following equations.

$$VOUT = VREF \times \frac{R_{Z1} + R_{SET}}{R_{SET}} \quad (50)$$

$$GAIN = R_{PZ2} \times \frac{R_{Z1} + R_{P1}}{R_{Z1} \times R_{P1}} \quad (51)$$

$$f_{P1} = \frac{1}{2\pi \times R_{P1} \times C_{PZ1}} \quad (52)$$

$$f_{P2} = \frac{C_{P2} + C_{Z2}}{2\pi \times R_{PZ2} \times C_{P2} \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{P2}} \quad (53)$$

$$f_{Z1} = \frac{1}{2\pi \times R_{Z1} \times C_{PZ1}} \quad (54)$$

$$f_{Z2} = \frac{1}{2\pi \times \left(R_{PZ2} + R_{P1}\right) \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{Z2}} \quad (55)$$

Looking at the PWM and LC bode plot, there are a few things which must be done to achieve stability.

1. Place two zeros close to the double pole, e.g. $f_{Z1} = f_{Z2} = 4.3$ kHz
2. Place both poles well above the crossover frequency. The crossover frequency was selected as one sixth the switching frequency, $f_{co1} = 50$ kHz, $f_{P1} = 66$ kHz
3. Place the second pole at three times f_{co1}. This ensures that the overall system gain falls off quickly to give good gain margin, $f_{p2} = 150$ kHz
4. The high-frequency gain should be sufficient to ensure 0 dB at the required crossover frequency, GAIN = –1 × gain of PWM and LC at the crossover frequency, GAIN = 16.9 dB

Using these values and Equation 50 through Equation 55, the Rs and Cs around the compensation network can be calculated.

1. Set $R_{Z1} = 51$ kΩ
2. Calculate R_{SET} using Equation 50, $R_{SET} = 32.4$ kΩ
3. Using Equation 54 and $f_{z1} = 4.3$ kHz, C_{PZ1} can be calculated to be 726 pF, C_{PZ1}= 680 pF
4. F_{P1} and Equation 52 yields R_{P1} to be a standard value of 3.3 kΩ.

5. The required gain of 16.9 dB and Equation 51 sets the value for R_{PZ2}. R_{PZ2} = 21.5 kΩ.
6. C_{Z2} is calculated using Equation 55 and the desired frequency for the second zero, C_{Z2} = 1.7 nF, or using standard values, 1.8 nF.
7. Finally, C_{P2} is calculated using the second pole frequency and Equation 53; C_{P2} = 47 pF.

Using these values, the simulated results are 57° of phase margin at 54 kHz.

Table 4. Bill of Materials

RefDes	Count	Value	Description	Size	Part Number	Mfr
C1	1	470 µF	Capacitor, aluminum, 470-µF, 25-V, 20%	0.457 x 0.406	EEVFK1E471P	Panasonic
C2, C10	2	0.1 µF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C3	1	15 nF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C4	1	47 pF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C5	1	1.8 nF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C6	1	680 pF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C7	1	51 pF	Capacitor, ceramic, 25-V, COG 20%	0603	Std	Vishay
C8, C11	2	0.1 µF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C9	1	1 µF	Capacitor, ceramic, 25-V, X7R, 20%	0805	Std	Vishay
C12, C14, C15	3	22 µF	Capacitor, ceramic, 22-µF, 16-V, X5R, 20%	1812	C4532X5R1C226MT	TDK
C13	1	2.2 nF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C16	1	470 µF	Capacitor, aluminum, SM, 6.3-V, 300-mΩ (FC series)	8 mm × 10 mm	Std	Panasonic
C17	1	47 µF	Capacitor, ceramic, 47-uF, 6.3-V, X5R, 20%	1812	C4532X5R0J476MT	TDK
D1	1	BAT54	Diode, Schottky, 200-mA, 30-V	SOT23	BAT54	Vishay
J1, J2	2	ED1609-ND	Terminal block, 2-pin, 15-A, 5,1-mm	0.40 × 0.35	ED1609	OST
J3	1	PTC36SAAN	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
L1	1	2.5 µH	Inductor, SMT, 2.5 µH, 16.5-A, 3.4- mΩ	0.515 × 0.516	MLC1550-252ML	Coilcraft
Q1	1	Si7860DP	MOSFET, N-channel, 30-V, 18-A, 8.0-mΩ	PWRPAK S0-8	Si7860DP	Vishay
Q2	1	Si7336ADP	MOSFET, N-channel, 30-V, 18-A, 40-mΩ	PWRPAK S0-8	Si7886ADP	Vishay
Q3	1	FDV301N	MOSFET, N-channel, 25-V, 220-mA, 5-Ω	SOT23	FDV301N	Fairchild
R1	1	10 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R2, R6	2	165 kΩ	Resistor, Chip, 1/16-W, 20%	0603	Std	Std
R3	1	32.4 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std

Table 4. Bill of Materials (continued)

RefDes	Count	Value	Description	Size	Part Number	Mfr
R4, R11	2	0 Ω	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R5	1	21.5k	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R7	1	51.0k	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R8	1	3.3 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R9	1	1.8 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R10	1	330 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R12	1	51 Ω	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R13	1	1 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
U1	1	TPS40077 PWP	IC, Texas Instruments	PWP16	TPS40077PWP	TI

EXAMPLE APPLICATIONS

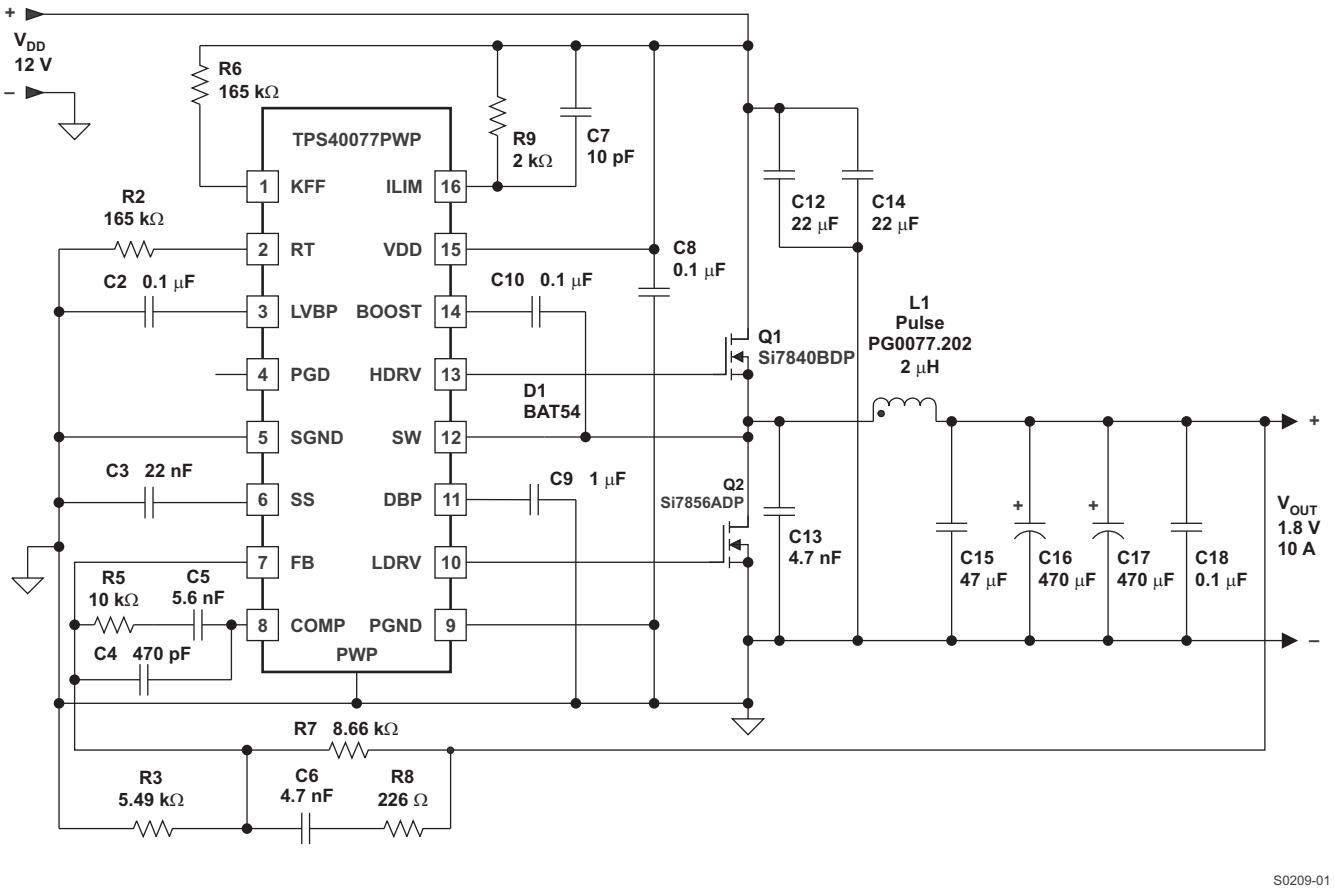
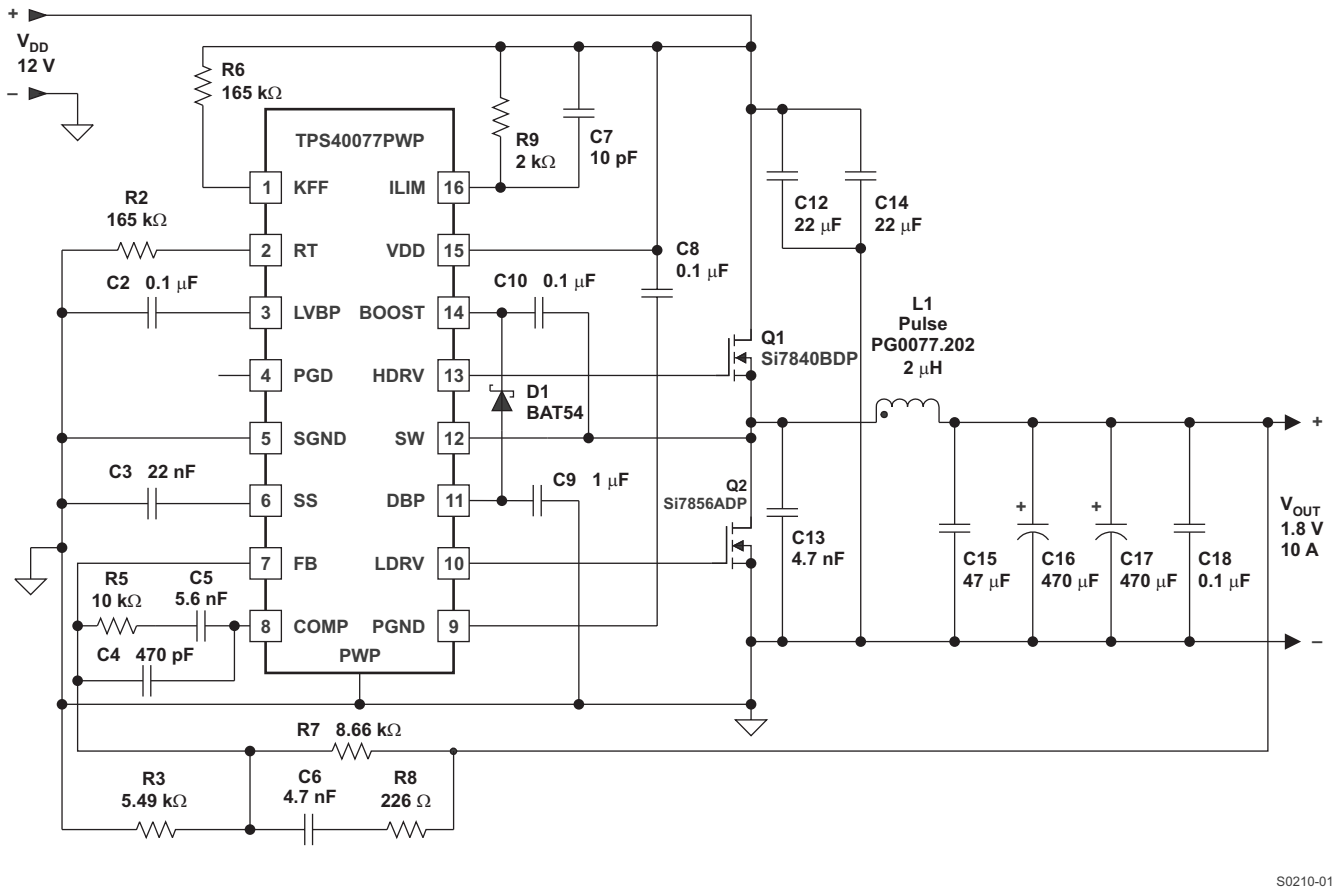


Figure 34. 300 kHz, 12 V to 1.8 v

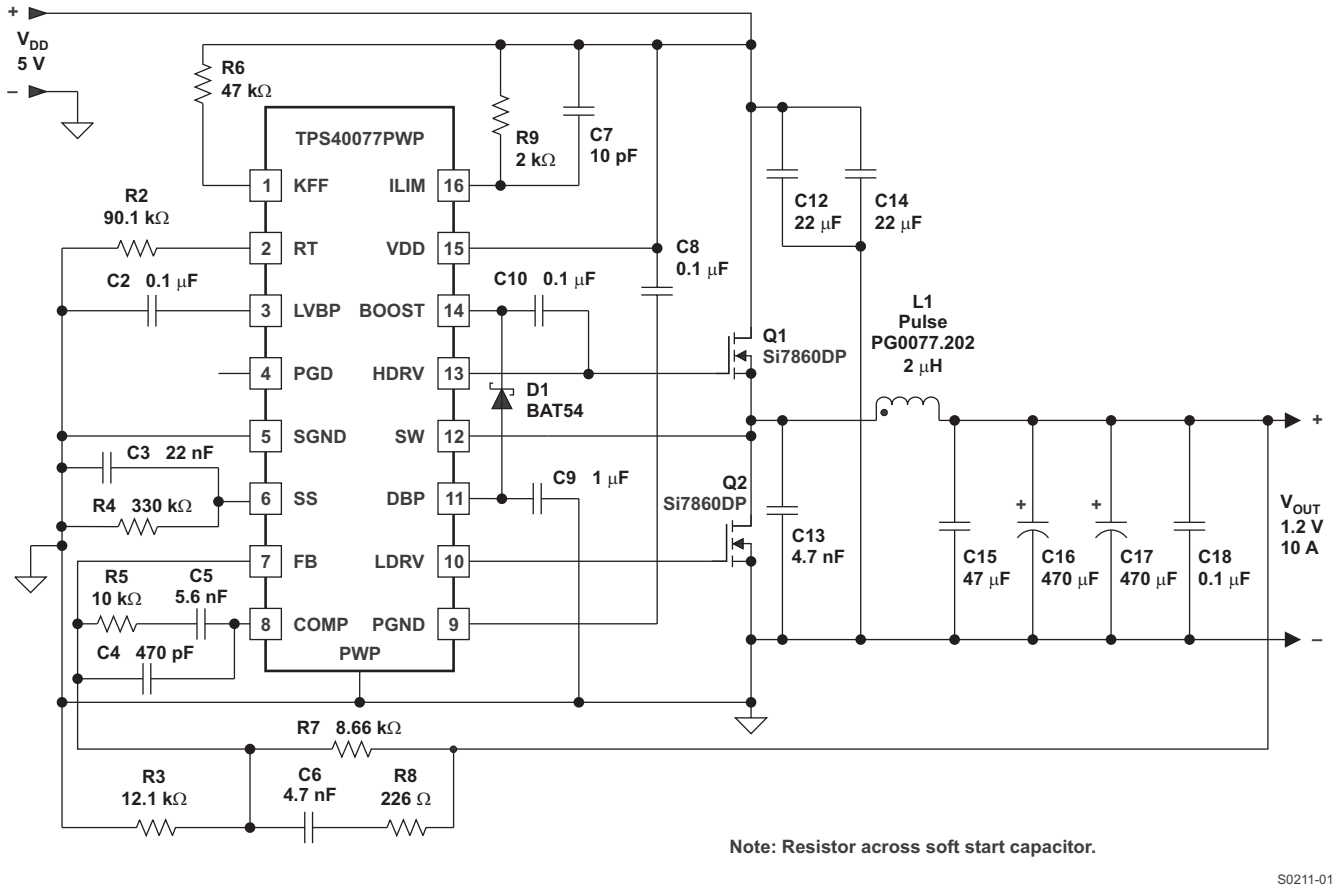
EXAMPLE APPLICATIONS (continued)



See the Boost Diode section.

Figure 35. 300 kHz, 12 V to 1.8 v With Improved High-Side Gate Drive

EXAMPLE APPLICATIONS (continued)

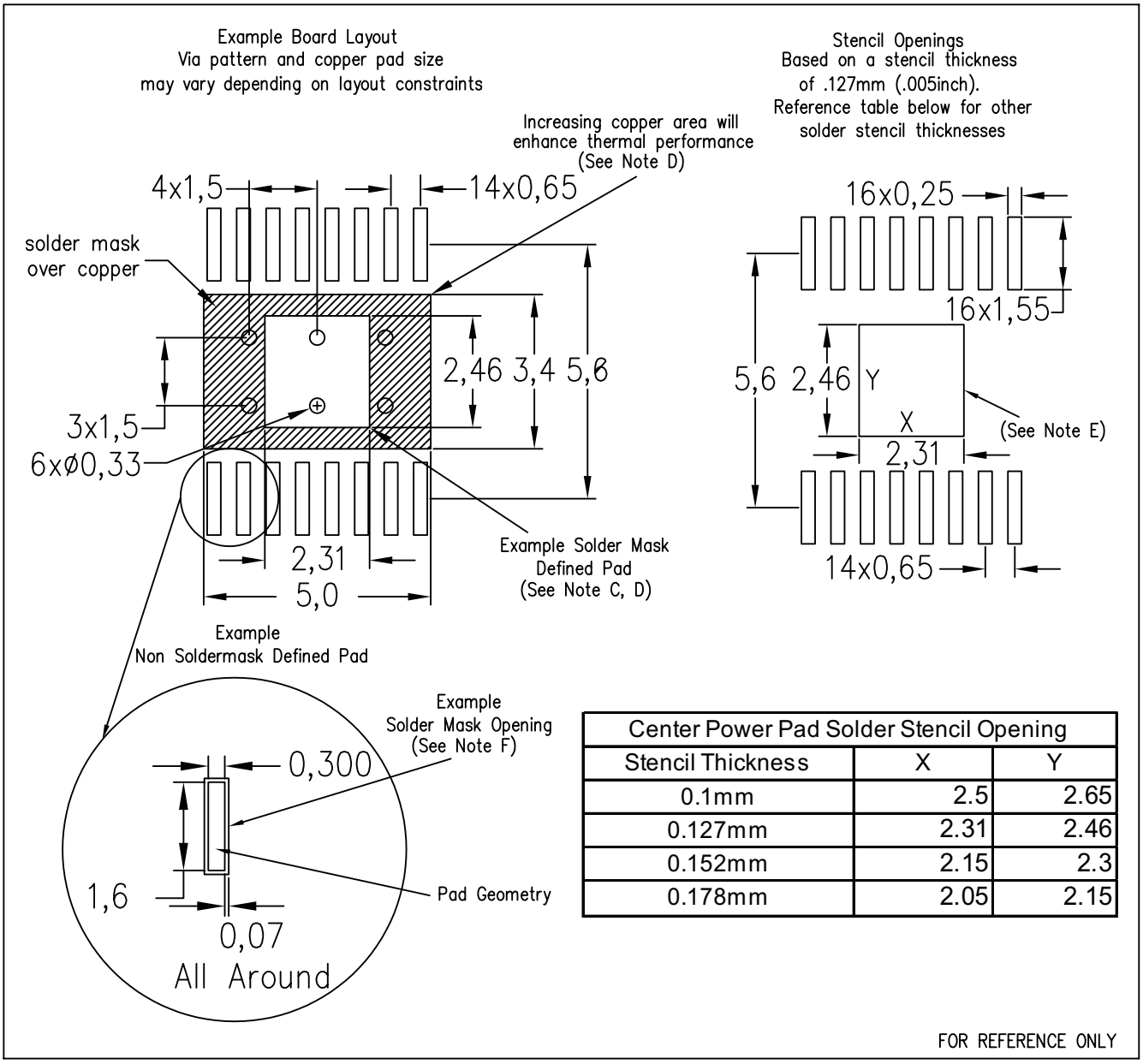


See the Boost Diode section.

Figure 36. 500 kHz, 5V to 1.2 V With Improved High-Side Gate Drive

REFERENCES

Package Footprint



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–SM–782 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

Figure 37. Example Land Pattern for PWP (R-PDSO-G16) PowerPAD™ Package

REFERENCES (continued)

Related Parts

The following parts are similar to the TPS40077 and may be of interest:

- *TPS40190 Low Pin Count Synchronous Buck Controller* (SLUS658)
- *TPS40100 Midrange Input Synchronous Buck Controller With Advanced Sequencing and Output Margining* (SLUS601)
- *TPS40075 Midrange Input Synchronous Buck Controller With Voltage Feed-Forward* (SLUS676)
- *TPS40057 Wide-Input Synchronous Buck Controller* (SLUS593)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS40077PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40077PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

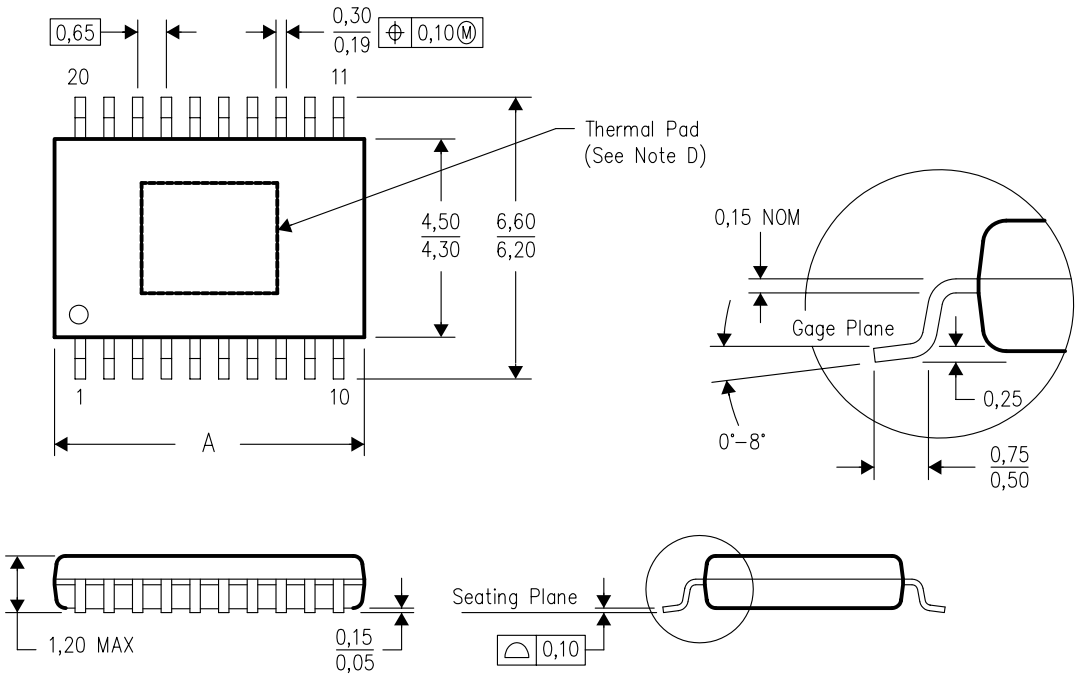
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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