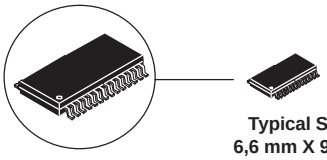


Typical Size
6,6 mm X 9,8 mm

SGLS266D – OCTOBER 2004 – REVISED DECEMBER 2004

3-V TO 6-V INPUT, 6-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **Qualification in Accordance With AEC-Q100**(1)
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **30-mΩ, 12-A Peak MOSFET Switches for High Efficiency at 6-A Continuous Output Source and Sink**
- **0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V Fixed Output Voltage Devices With 1% Initial Accuracy**
- **Internally Compensated for Easy Use and Minimal Component Count**
- **Fast Transient Response**
- **Wide PWM Frequency − Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

(1) Contact Texas Instruments for details. Q100 qualification data available on request.

APPLICATIONS

- **Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**
- **Portable Computing/Notebook PCs**

DESCRIPTION

The SWIFT™ family of dc/dc regulators, the TPS54611, TPS54612, TPS54613, TPS54614, TPS54615, and TPS54616 low-input voltage high-output current synchronous-buck PWM converters integrate all required active components. Included on the substrate are true, high-performance, voltage error amplifiers that provide high performance under transient conditions; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

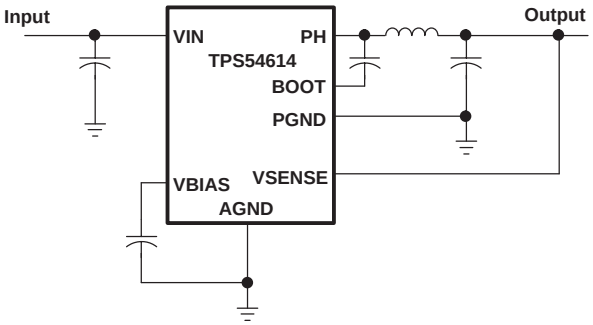
The TPS54611−6 devices are available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. Texas Instruments provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

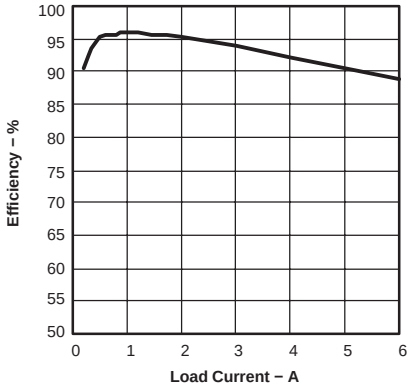
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD and SWIFT are trademarks of Texas Instruments.

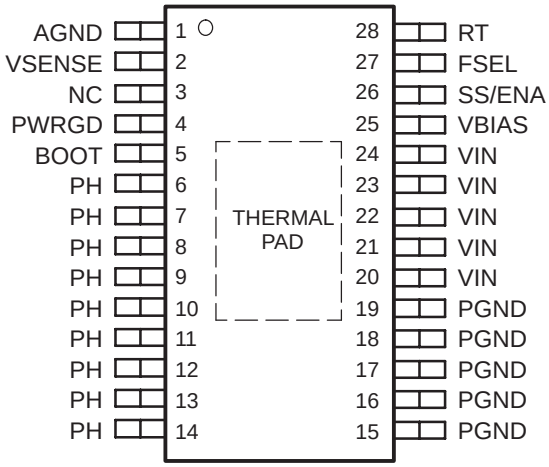
SIMPLIFIED SCHEMATIC



EFFICIENCY AT 350 kHz



PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE	PACKAGED DEVICES	T_J	OUTPUT VOLTAGE	PACKAGED DEVICES
		PLASTIC HTSSOP (PWP)(1)			PLASTIC HTSSOP (PWP)(1)
−40°C to 125°C	0.9 V	TPS54611QPWPRQ1	−40°C to 125°C	1.8 V	TPS54614QPWPRQ1
	1.2 V	TPS54612QPWPRQ1(2)		2.5 V	TPS54615QPWPRQ1
	1.5 V	TPS54613QPWPRQ1		3.3 V	TPS54616QPWPRQ1

(1) The PWP package is taped and reeled as denoted by the R suffix on the device type (i.e., TPS54616QPWPRQ1). See application section of data sheet for PowerPAD drawing and layout information.
(2) Product Preview

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	1	Analog ground. Return for slow-start capacitor, VBIAS capacitor, RT resistor FSEL. Make PowerPAD connection to AGND.
BOOT	5	Bootstrap input. A 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates a floating drive for the high-set FET driver.
NC	3	No connection
PGND	15−19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns and negative terminals of the input and output capacitors.
PH	6−14	Phase input/output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. High-Z when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
FSEL	27	Frequency select input. Provides logic input to select between two internally set switching frequencies.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-µF to 1-µF ceramic capacitor.
VIN	20−24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 1-µF to 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect directly to output voltage sense point.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

V_I	Input voltage range	VIN, SS/ENA, FSEL	−0.3 V to 7 V
		RT	−0.3 V to 6 V
		VSENSE	−0.3 V to 4 V
		BOOT	−0.3 V to 17 V
V_O	Output voltage range	VBIAS, PWRGD	−0.3 V to 7 V
		PH	−0.6 V to 10 V
I_O	Source current	PH	Internally Limited
		VBIAS	6 mA
I_S	Sink current	PH	12 A
		SS/ENA, PWRGD	10 mA
Voltage differential		AGND to PGND	±0.3 V
Continuous power dissipation			See Power Dissipation Rating Table
T_J	Operating virtual junction temperature range		−40°C to 150°C
T_{stg}	Storage temperature		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28 Pin PWP with solder	18.2°C/W	5.49 W(3)	3.02 W	2.2 W
28 Pin PWP without solder	40.5°C/W	2.48 W	1.36 W	0.99 W

(1) For more information on the PWP package, see the Texas Instruments technical brief, literature number SLMA002.
(2) Test board conditions:
1. 3” x 3”, 4 layers, thickness: 0.062”
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 0.5 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias (see “Recommended Land Pattern” in applications section of this data sheet)
(3) Maximum power dissipation may be limited by overcurrent protection.

ADDITIONAL 6A SWIFT™ DEVICES

DEVICE	OUTPUT VOLTAGE
TPS54610	0.9 V to 3.3 V
TPS54672	DDR memory adjustable
TPS54680	Sequencing adjustable
TPS54673	Prebias adjustable

RELATED DC/DC PRODUCTS

- TPS40000—Low-input, voltage-mode synchronous buck controller
- TPS759xx—7.5-A low dropout regulator
- PT6440 series—6 A plugin modules

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
	Input voltage range, VIN			3		6	V
$I_{(Q)}$	Quiescent current		f_S = 350 kHz, FSEL ≤ 0.8 V, RT open, phase pin open		9.8	15	mA
			f_S = 550 kHz, FSEL ≥ 2.5 V, RT open, phase pin open		14	23	
			Shutdown, SS/ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT							
	Start threshold voltage, UVLO				2.95	3	V
	Stop threshold voltage, UVLO			2.7	2.8		V
	Hysteresis voltage, UVLO				0.16		V
	Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE							
	Output voltage, VBIAS		$I_{(VBIAS)}$ = 0	2.7	2.8	2.95	V
	Output current, VBIAS(2)					100	µA
OUTPUT VOLTAGE							
V_O	Output voltage	TPS54611	T_J = 25°C, VIN = 5 V		0.9		V
			3 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−2%		2%	
		TPS54612	T_J = 25°C, VIN = 5 V		1.2		V
			3 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−2%		2%	
		TPS54613	T_J = 25°C, VIN = 5 V		1.5		V
			3 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−2%		2%	
		TPS54614	T_J = 25°C, VIN = 5 V		1.8		V
			3 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−3%		3%	
		TPS54615	T_J = 25°C, VIN = 5 V		2.5		V
			3 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−3%		3%	
		TPS54616	T_J = 25°C, VIN = 5 V		3.3		V
			4 V ≤ VIN ≤ 6 V, 0 ≤ I_L ≤ 6 A, −40° ≤ T_J ≤ 125°C	−3%		3%	
REGULATION							
	Line regulation(1) (3)		I_L = 3 A, 350 ≤ f_S ≤ 550 kHz, T_J = 85°C		0.088		%/V
	Load regulation(1) (3)		I_L = 0 A to 6 A, 350 ≤ f_S ≤ 550 kHz, T_J = 85°C		0.0917		%/A

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR					
Internally set—free running frequency	FSEL ≤ 0.8 V, RT open	265	350	440	kHz
	FSEL ≥ 2.5 V, RT open	415	550	680	
Externally set—free running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
	RT = 160 kΩ (1% resistor to AGND)	290	312	350	
	RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
High level threshold, FSEL		2.5			V
Low level threshold, FSEL				0.8	V
Pulse duration, FSEL(1)		50			ns
Frequency range, FSEL(1) (4)		330		700	kHz
Ramp valley(1)			0.75		V
Ramp amplitude (peak-to-peak)(1)			1		V
Minimum controllable on time(1)				200	ns
Maximum duty cycle(1)		90%			

(1) Specified by design
(2) Static resistive loads only
(3) Tested using circuit in Figure 10.
(4) To ensure proper operation when RC filter is used between external clock and FSEL pin, the recommended values are R ≤ 1kΩ and C ≤ 120 pF.

ELECTRICAL CHARACTERISTICS (CONTINUED)

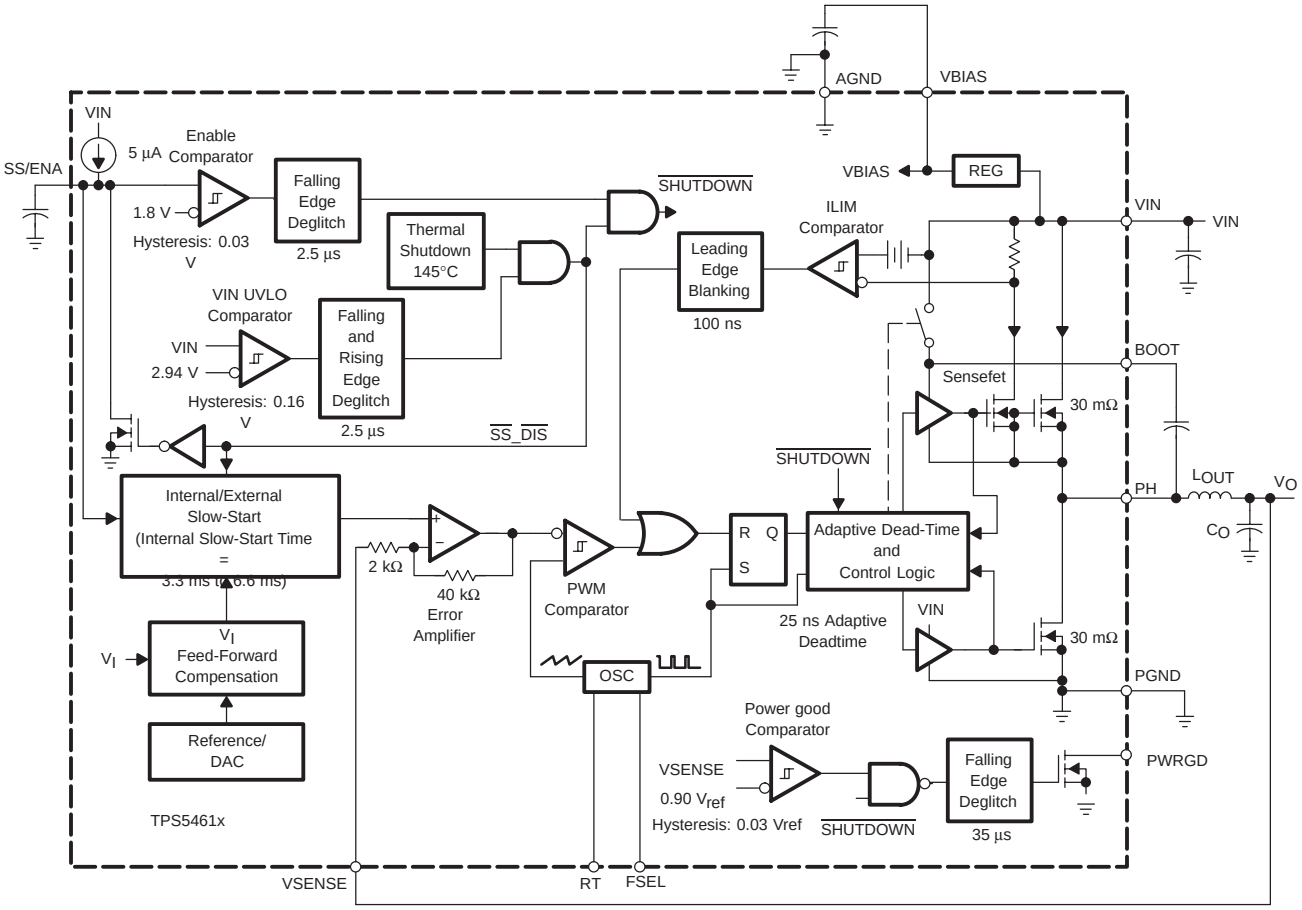
T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Error amplifier open loop voltage gain(1)				26		dB
Error amplifier unity gain bandwidth(1)			3	5		MHz
Error amplifier common mode input voltage range		Powered by internal LDO(1)	0		VBIAS	V
PWM COMPARATOR						
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)		10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
Enable threshold voltage, SS/ENA			0.82	1.20	1.40	V
Enable hysteresis voltage, SS/ENA(1)				0.03		V
Falling edge deglitch, SS/ENA(1)				2.5		µs
Internal slow-start time (1)	TPS54611		2.6	3.3	4.1	ms
	TPS54612		3.5	4.5	5.4	
	TPS54613		4.4	5.6	6.7	
	TPS54614		2.6	3.3	4.1	
	TPS54615		3.6	4.7	5.6	
	TPS54616		4.7	6.1	7.6	
Charge current, SS/ENA		SS/ENA = 0 V	2.5	5	8	µA
Discharge current, SS/ENA		SS/ENA = 0.2 V, V_I = 2.7 V	1.2	2.3	4.0	mA
POWER GOOD						
Power good threshold voltage		VSENSE falling		90		$\%V_O$
Power good hysteresis voltage		See (1)		3		$\%V_O$
Power good falling edge deglitch		See (1)		35		µs
Output saturation voltage, PWRGD		$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD		V_I = 5.5 V			1	µA
CURRENT LIMIT						
Current limit		V_I = 3 V	7.2	10		A
		V_I = 6 V	10	12		
Current limit leading edge blanking time (1)				100		ns
Current limit total response time(1)				200		ns
THERMAL SHUTDOWN						
Thermal shutdown trip point(1)			135	150	165	°C
Thermal shutdown hysteresis(1)				10		
OUTPUT POWER MOSFETS						
$r_{DS(on)}$ Power MOSFET switches		I_O = 3 A, V_I = 6 V(2)		26	47	mΩ
		I_O = 3 A, V_I = 3 V(2)		36	65	

(1) Specified by design

(2) Matched MOSFETs, low side $r_{DS(on)}$ production tested, high side $r_{DS(on)}$ specified by design.

INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

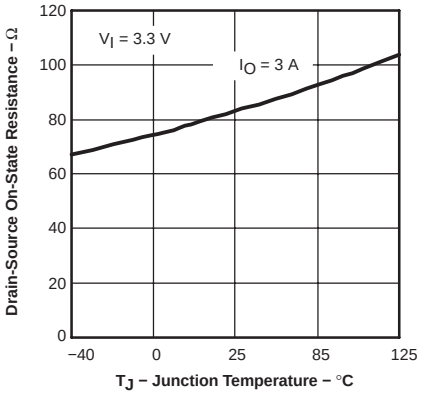


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

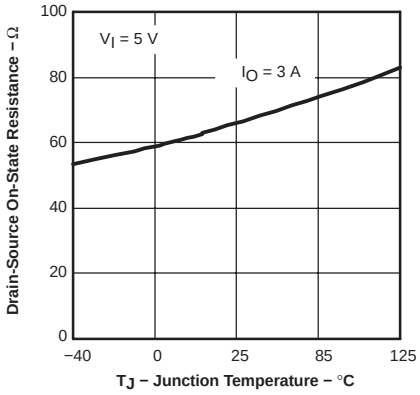


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

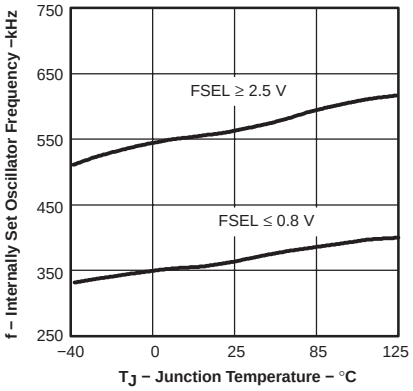


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

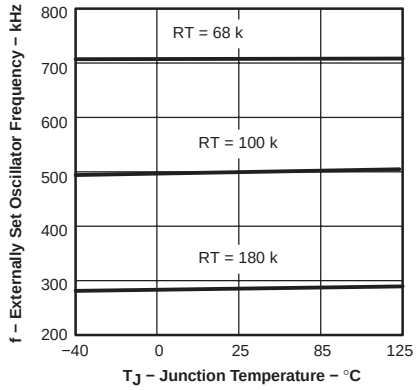


Figure 4

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

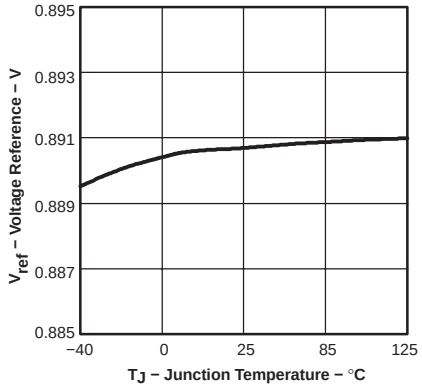


Figure 5

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

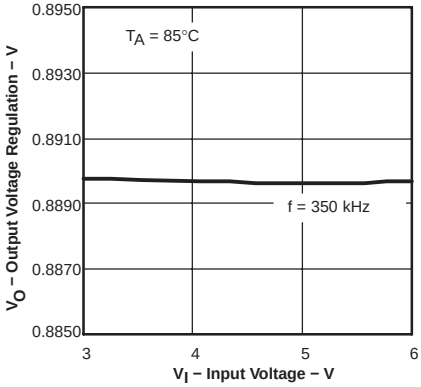


Figure 6

ERROR AMPLIFIER OPEN LOOP RESPONSE

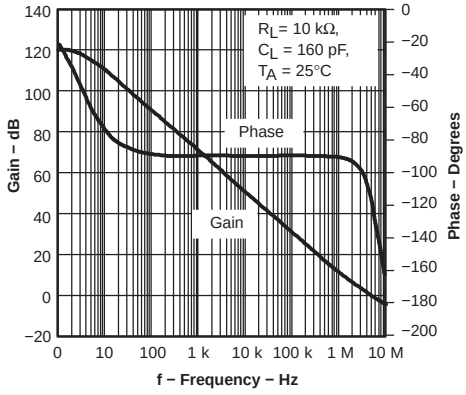


Figure 7

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

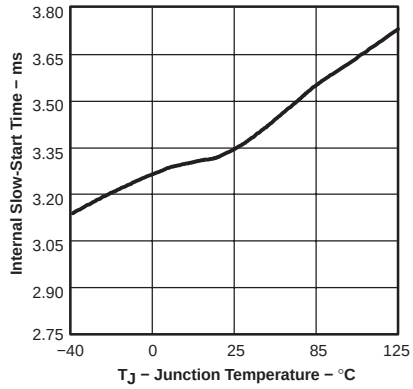


Figure 8

DEVICE POWER LOSSES vs LOAD CURRENT

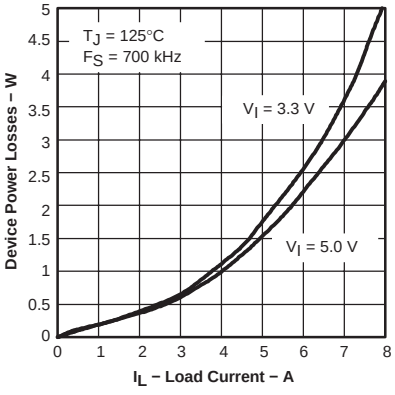


Figure 9

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54614 application. The TPS54614 (U1) can provide greater than 6 A of output current at a nominal output voltage of 1.8 V. For proper operation, the exposed thermal PowerPAD underneath the integrated circuit package needs to be soldered to the printed-circuit board.

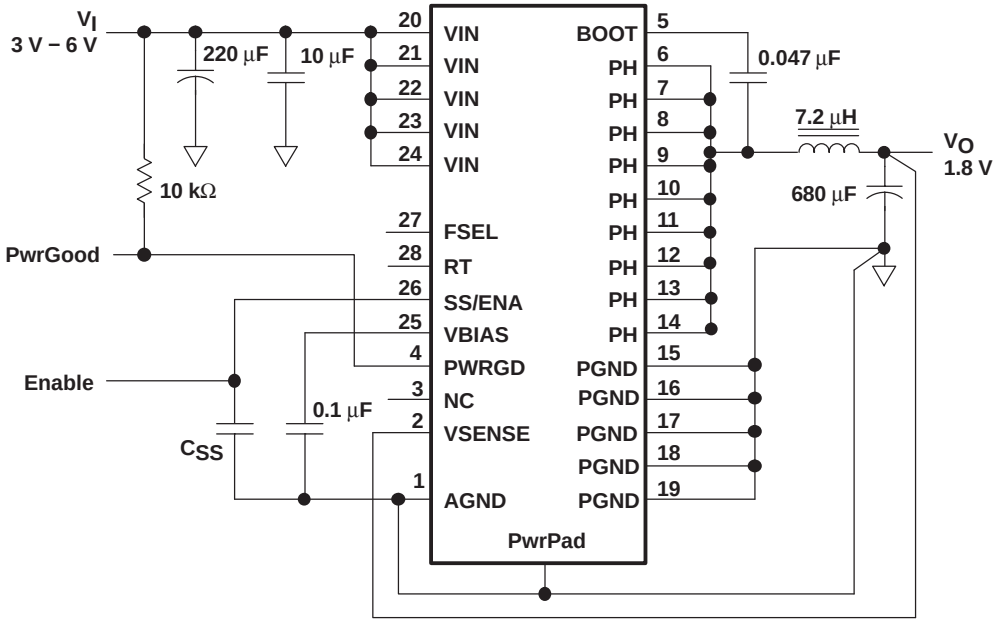


Figure 10. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected using the SWIFT designer software tool. SWIFT designer provides a complete design environment for developing dc-dc converters using the TPS54614, or other devices in the SWIFT product family. Additional design information is available at www.ti.com.

INPUT FILTER

The input to the circuit is a nominal 3.3 VDC or 5 VDC. The input filter is a 220-µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. A 10-µF ceramic capacitor for the TPS54614 is required, and must be located as close as possible to the device.

FEEDBACK CIRCUIT

The output voltage of the converter is fed directly into the VSENSE pin of the TPS54614. The TPS54614 is internally compensated to provide stability of the output under varying line and load conditions.

OPERATING FREQUENCY

In the application circuit, 350 kHz operation is selected by leaving FSEL open. Different operating frequencies can be selected by connecting a resistor between RT pin and AGND. Choose the value of R using Equation 1 for the desired operating frequency:

$$R = \frac{500\ \text{kHz}}{\text{SwitchingFrequency}} \times 100\ \text{k}\Omega \quad (1)$$

Alternately, a preset operating frequency of 550 kHz can be selected by leaving RT open and connecting the FSEL pin to V_I.

OUTPUT FILTER

The output filter is composed of a 5.2-µH inductor and a 470-µF capacitor. The inductor is low dc resistance (16-mΩ) type, Sumida CDRH104R−5R2. The capacitor used is a 4-V POSCAP with a maximum ESR of 40 mΩ. The output filter components work with the internal compensation network to provide a stable closed loop response for the converter.

GROUNDING AND POWERPAD LAYOUT

The TPS54611−16 have two internal grounds (analog and power). Inside the TPS54611−16, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD is tied internally to the analog ground. Noise injected between the two grounds can degrade the performance of the TPS54611−16, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes should tie together directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54611−16. The layout of the TPS54614 evaluation module is representative of a recommended layout for a 4-layer board. Documentation for the TPS54614 evaluation module can be found on the Texas Instruments web site (www.ti.com) under the TPS54614 product folder. See the TPS54614−185 User's Guide, Texas Instruments (SLVU053) and the application note, Texas Instruments (SLVA105).

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposes area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the 10 recommended that enhance thermal performance should be included in areas not under the device package.

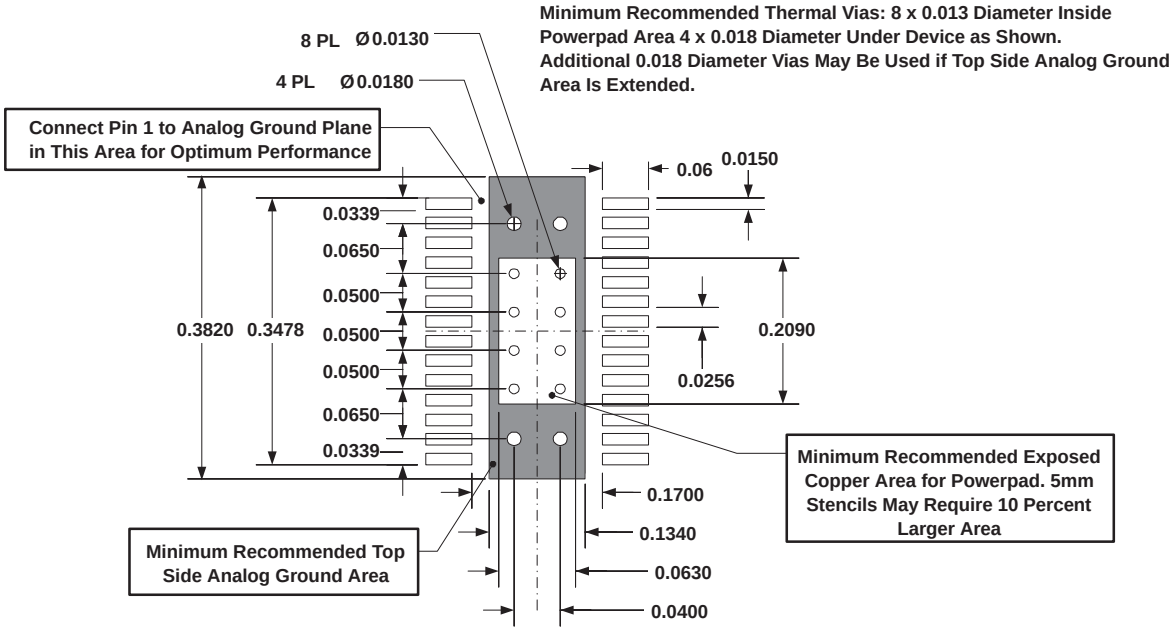


Figure 11. Recommended Land Pattern for 28-Pin PWP PowerPAD

PERFORMANCE GRAPHS

EFFICIENCY vs LOAD CURRENT

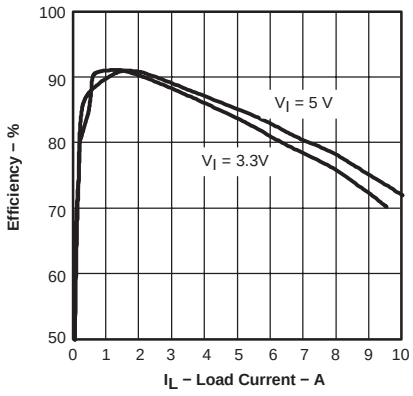


Figure 12

OUTPUT VOLTAGE vs LOAD CURRENT

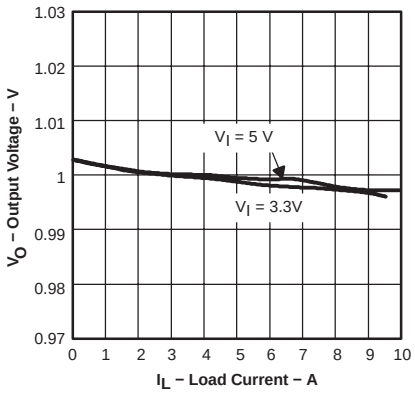


Figure 13

LOOP RESPONSE

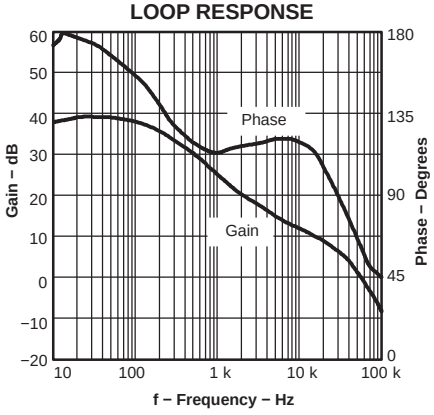


Figure 14

TRANSIENT RESPONSE

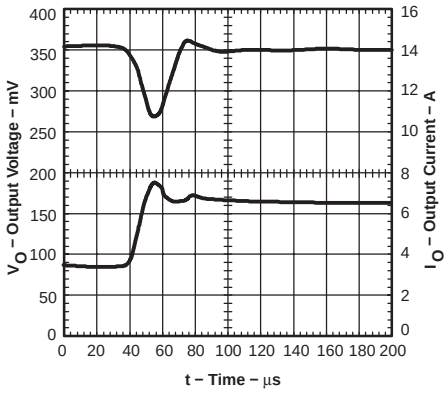


Figure 15

START-UP WAVEFORMS

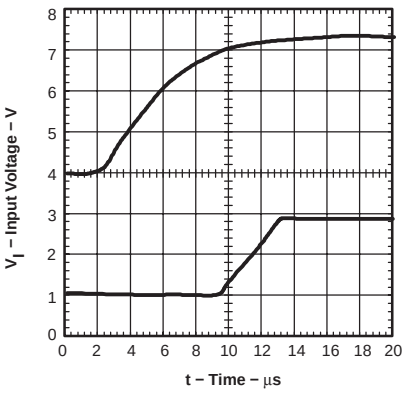


Figure 16

OUTPUT RIPPLE VOLTAGE

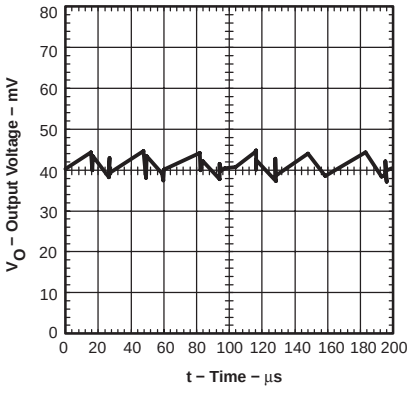


Figure 17

AMBIENT TEMPERATURE vs LOAD CURRENT

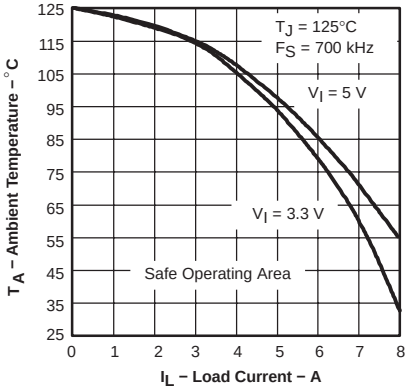


Figure 18

DETAILED DESCRIPTION

Under Voltage Lock Out (UVLO)

The TPS5461x incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator and a 2.5-µs rising and falling edge deglitch circuit reduces the likelihood of shutting the device down due to noise on VIN.

Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise. See the following table for start up times for each device

DEVICE	OUTPUT VOLTAGE	SLOW-START
TPS54611	0.9 V	3.3 ms
TPS54612	1.2 V	4.5 ms
TPS54613	1.5 V	5.6 ms
TPS54614	1.8 V	3.3 ms
TPS54615	2.5 V	4.7 ms
TPS54616	3.3 V	6.1 ms

The second function of the SS/ENA pin provides an external means for extending the slow-start time with a ceramic capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (2)$$

Second, as the output becomes active, a brief ramp up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (3)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp up at the internal rate.

VBIAS Regulator

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

Voltage Reference

The voltage reference system produces a precise, temperature-stable voltage from a bandgap circuit. A scaling amplifier and DAC are then used to produce the reference voltages for each of the fixed output devices.

Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the FSEL pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor from the RT pin to AGND and floating the FSEL pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ k\Omega}{R} \times 500\ [kHz] \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into FSEL and connecting a resistor from RT to AGND. Choose an RT resistor that sets the free-running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations.

Table 1. Summary of the Frequency Selection Configurations

SWITCHING FREQUENCY	FSEL PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 68 k to 180 k
Externally synchronized frequency(1)	Synchronization signal	R = RT value for 80% of external synchronization frequency

(1) To ensure proper operation when RC filter is used between external clock and FSEL pin, the recommended values are R ≤ 1kΩ and C ≤ 120 pF.

Error Amplifier

The high performance, wide bandwidth, voltage error amplifier is gain-limited to provide internal compensation of the control loop. The user is given limited flexibility in choosing output L and C filter components. Inductance values of 4.7 µH to 10 µH are typical and available from several vendors. The resulting designs exhibit good noise and ripple characteristics, but with exceptional transient response. Transient recovery times are typically in the range of 10 µs to 20 µs.

PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately set and reset the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as V_{ref}. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54611−TPS54616 devices are capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and the low-side FET turns on to decrease the energy in the output inductor and consequently decrease the output current. This process is repeated each cycle in which the current limit comparator is tripped.

Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. The high-side and low-side drivers are designed with 300 mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

Overcurrent Protection

Cycle-by-cycle current limiting is achieved by sensing the current flow through the high-side MOSFET and a differential amplifier with preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously: starting up by

control of the slow-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown trip point.

Power Good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE falls 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling edge deglitch circuit prevent tripping of the power good comparator due to high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS54613QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
TPS54614QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
TPS54615QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR

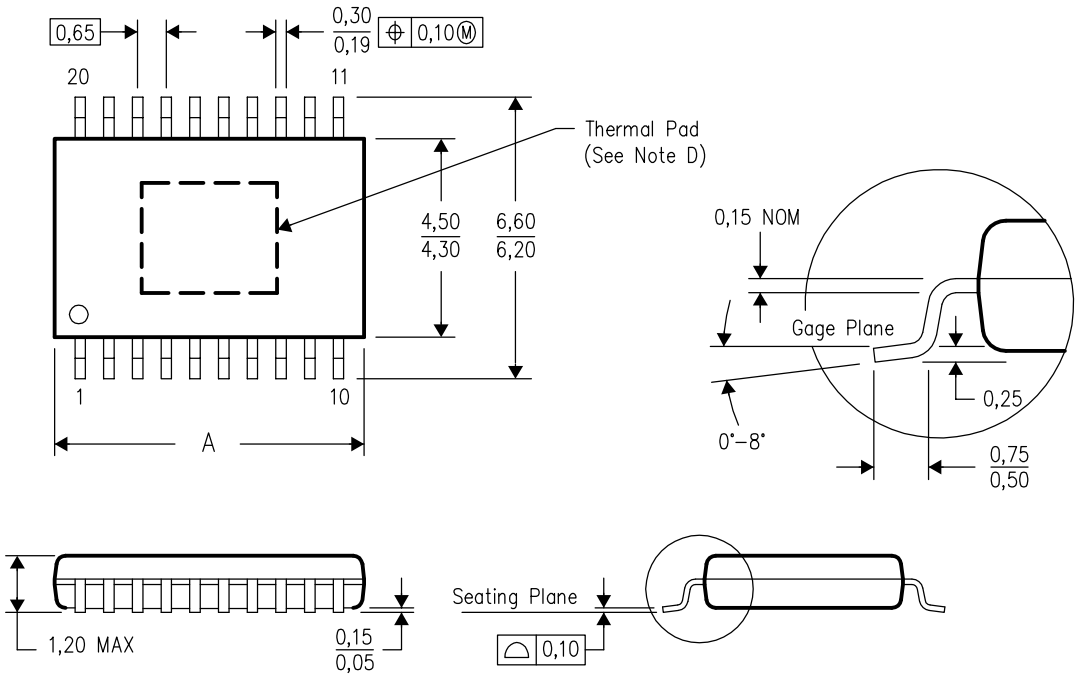
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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