

**Product Description**

The TQ3M31 is a 2.8V, RF dual band LNA IC designed specifically for Cellular & PCS band CDMA/AMPS applications. It's RF performance meets the requirements of products designed to the IS-95 and AMPS standards. The TQ3M31 is designed to be used with the TQ5131 (Cellular CDMA/AMPS mixer) and the TQ5631 (PCS CDMA mixer) which provides a complete Tri-Mode CDMA receiver for 800MHz dual-mode and 1900MHz phones.

The LNA incorporates on-chip switches which determine CDMA, AMPS, and bypass mode select. When used with the TQ5131 and TQ5631, four gain states are available in each band. The RF output port is internally matched to 50 Ω, greatly simplifying the design and keeping the number of external components to a minimum. The TQ3M31 achieves good RF performance with low current consumption, supporting long standby times in portable applications. Coupled with the very small MLF 3x3 package, the part is ideally suited for Cellular & PCS band mobile phones.

**Electrical Specifications<sup>1</sup>**

Parameter	Min	Typ	Max	Units
Gain	881MHz	13.0		dB
	1960MHz	13.5		dB
Noise Figure	881MHz	1.4		dB
	1960MHz	1.5		dB
Input 3 <sup>rd</sup> Order Intercept	881MHz	12.5		dBm
	1960MHz	9.0		dBm
DC supply Current	881MHz	10.0		mA
	1960MHz	11.0		mA

Note 1: Test Conditions: Vdd=2.8V, Tc=25C, CDMA High Gain state.

**TQ3M31**

**DATA SHEET**

**Dual Band LNA: 2.8V Cellular and PCS Band CDMA/AMPS LNA IC**

**Features**

- Small size: Leadless 3x3mm
- Single 2.8V operation
- Low-current operation
- Gain Select
- Mode Select
- High IP3 performance
- Few external components

**Applications**

- IS-95 CDMA Mobile Phones
- AMPS Mobile Phones
- Dual Mode CDMA Cellular applications
- Dual Band CDMA Cellular & PCS
- 832-870MHz CDMA applications
- 1930-1990MHz CDMA applications

# TQ3M31

## Data Sheet

### Electrical Characteristics

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
<b>Cellular LNA:</b> RF Frequency		832	881	894	MHz
<b>PCS LNA:</b> RF Frequency		1930	1960	1990	MHz
<b>CDMA Mode-High Gain</b>					
Gain	881MHz	12.0	13.0		dB
	1960MHz	12.0	13.5		dB
Noise Figure	881MHz		1.4	1.8	dB
	1960MHz		1.5	2.0	dB
Input IP3	881MHz	10.0	12.5		dBm
	1960MHz	8.0	9.0		dBm
LNA IN Return Loss (with external matching)	All modes, both bands	10			dB
LNA OUT Return Loss	All modes, both bands	10			dB
Supply Current	881MHz		10.0	13.0	mA
	1960MHz		11.0	13.0	mA
<b>Bypass Mode</b>					
Gain	881MHz	-6.0	-5.0		dB
	1960MHz	-3.5	-2.0		dB
Noise Figure	881MHz		5.0	6.0	dB
	1960MHz		2.0	3.2	dB
Input IP3	881MHz	18.0			dBm
	1960MHz	18.0			dBm
Supply Current	881MHz		1.0	2.0	mA
	1960MHz		1.0	2.0	mA
<b>High Gain Low Linearity Mode</b>					
Gain	881MHz		11.0		dB
	1960MHz		11.5		dB
Noise Figure	881MHz		1.6		dB
	1960MHz		1.7		dB
Input IP3	881MHz		7.5		dBm
	1960MHz		6.0		dBm
Supply Current	881MHz		4.5		mA
	1960MHz		4.5		mA
Supply Voltage		2.7	2.8	3.3	V
Logic low input		0		0.25	V
Logic high input		V <sub>cc</sub> -0.25		V <sub>cc</sub>	V

Note 1: Test Conditions: V<sub>dd</sub>=2.8V, T<sub>c</sub> = 25° C, unless otherwise specified.

Note 2: Min/Max limits are at +25°C case temperature, unless otherwise specified.

*Absolute Maximum Ratings*

Parameter	Value	Units
DC Power Supply	5.0	V
Power Dissipation	250	mW
Operating Temperature	-30 to 85	C
Storage Temperature	-60 to 150	C
Signal level on inputs/outputs	+20	dBm
Voltage to any non supply pin	+0.3	V

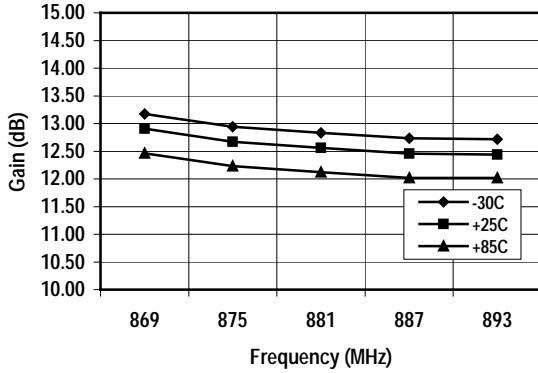
# TQ3M31

## Data Sheet

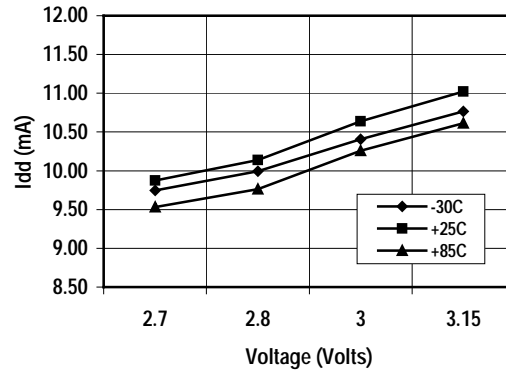
### Typical Performance

Cellular Band Test Conditions, unless Otherwise Specified: Vdd=2.8V, Tc=+25C, RF=881MHz

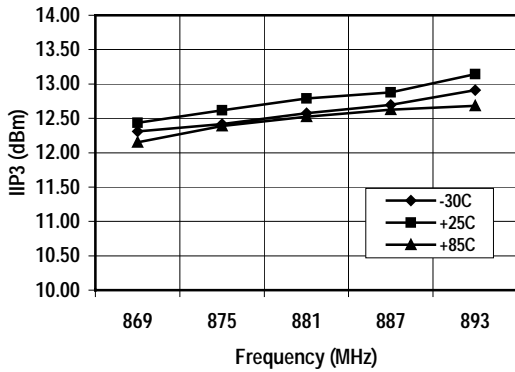
CDMA High Gain Mode  
Gain v Freq v Temp



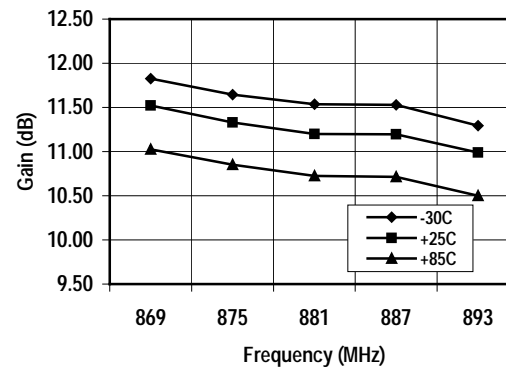
CDMA High Gain Mode  
Idd v Vdd v Temp



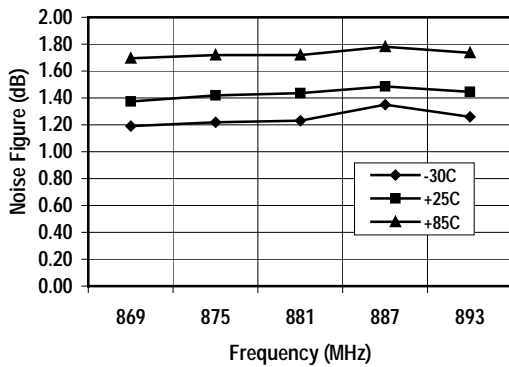
CDMA High Gain Mode  
IIP3 v Freq v Temp



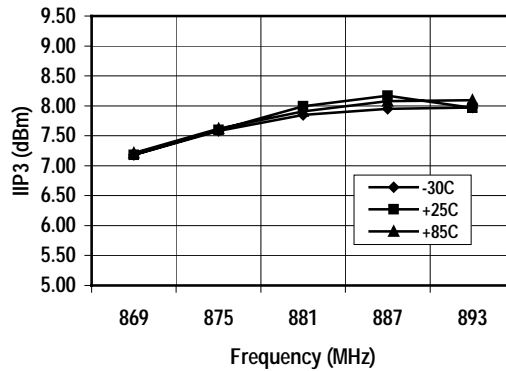
High Gain Low Linearity Mode  
Gain v Freq v Temp



CDMA High Gain Mode  
Noise Figure v Freq v Temp

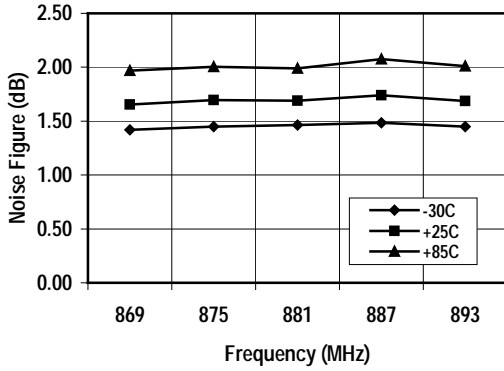


High Gain Low Linearity Mode  
IIP3 v Freq v Temp

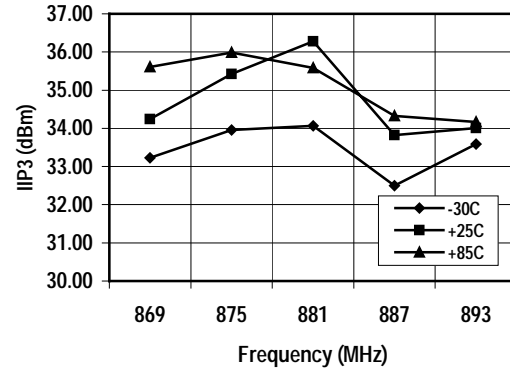


# TQ3M31 Data Sheet

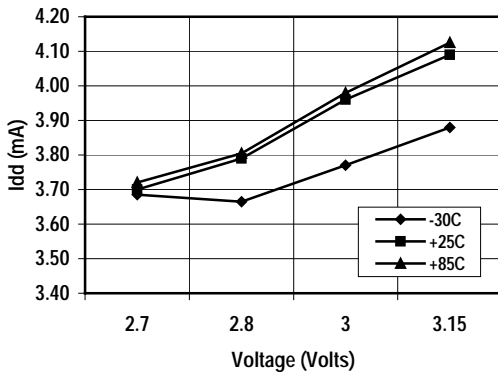
High Gain Low Linearity Mode  
Noise Figure v Freq v Temp



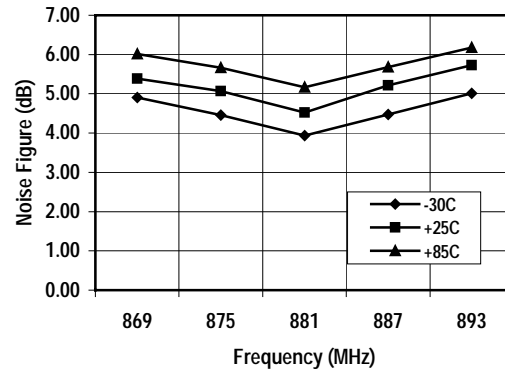
Bypass Mode  
IIP3 v Freq v Temp



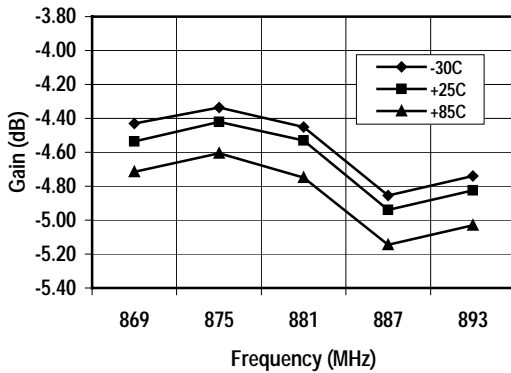
High Gain Low Linearity Mode  
Idd v Vdd v Temp



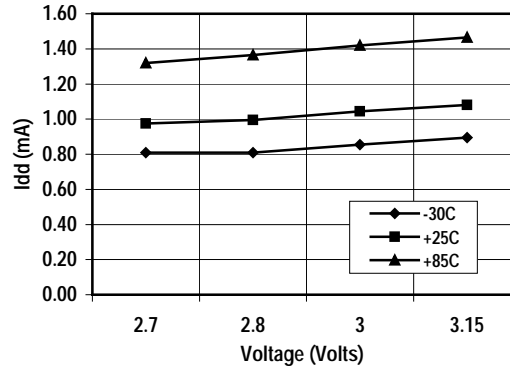
Bypass Mode  
Noise Figure v Freq v Temp



Bypass Mode  
Gain v Freq v Temp



Bypass Mode  
Idd v Vdd v Temp



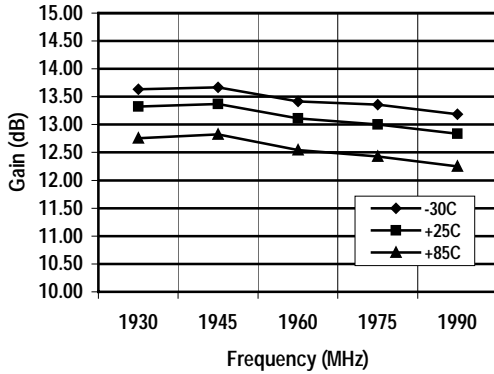
# TQ3M31

## Data Sheet

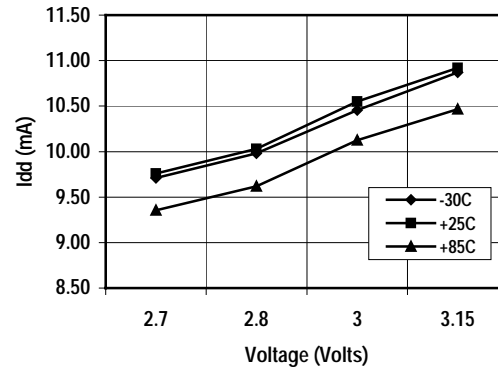
### Typical Performance

PCS Band Test Conditions, unless Otherwise Specified: Vdd=2.8V, Tc=+25C, RF=1960MHz

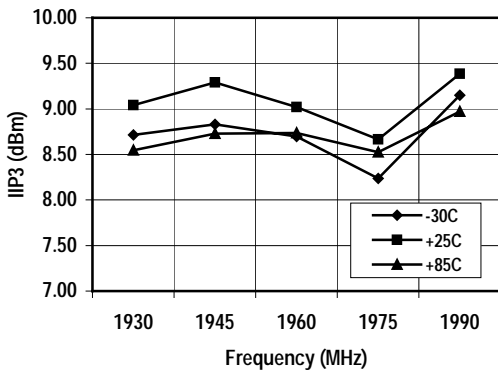
CDMA High Gain Mode  
Gain v Freq v Temp



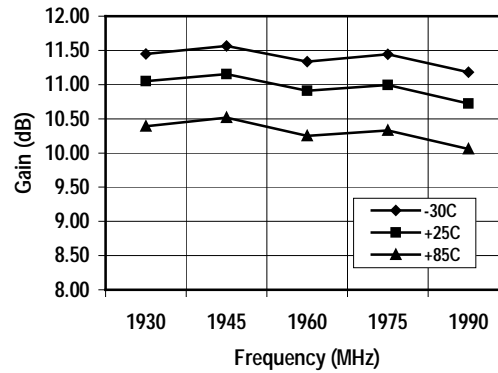
CDMA High Gain Mode  
Idd v Vdd v Temp



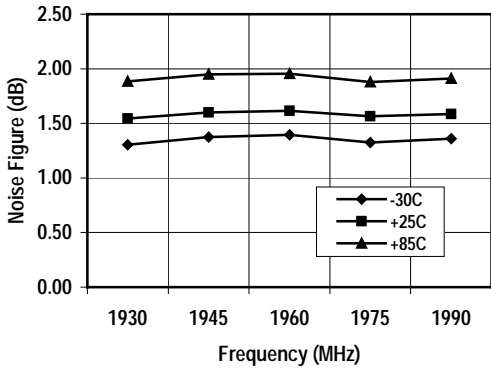
CDMA High Gain Mode  
IIP3 v Freq v Temp



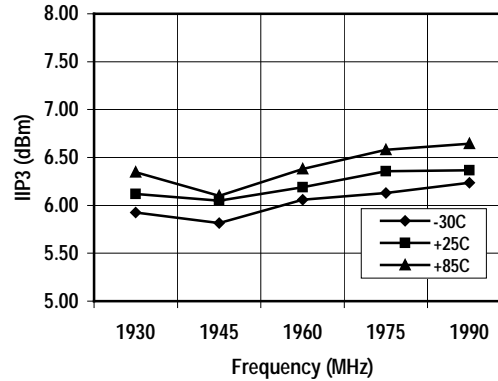
High Gain Low Linearity Mode  
Gain v Freq v Temp



CDMA High Gain Mode  
Noise Figure v Freq v Temp

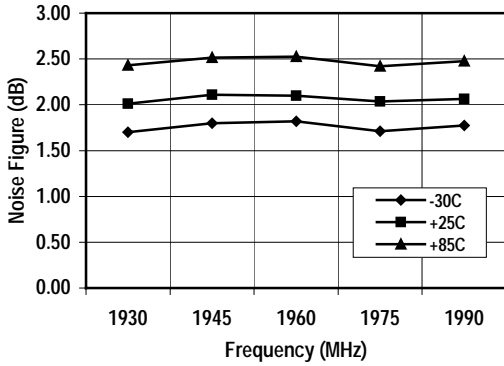


High Gain Low Linearity Mode  
IIP3 v Freq v Temp

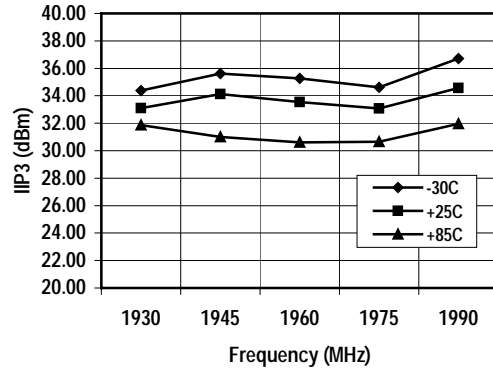


# TQ3M31 Data Sheet

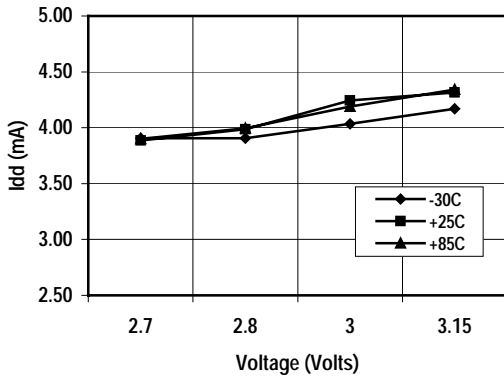
High Gain Low Linearity Mode  
Noise Figure v Freq v Temp



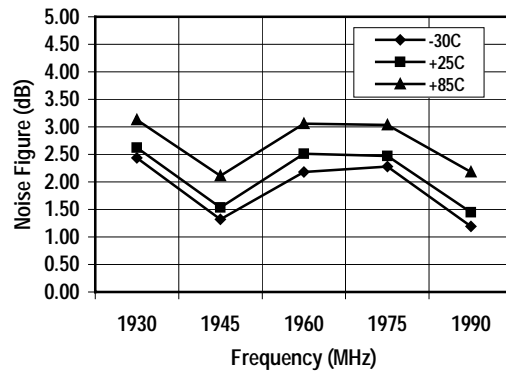
Bypass Mode  
IIP3 v Freq v Temp



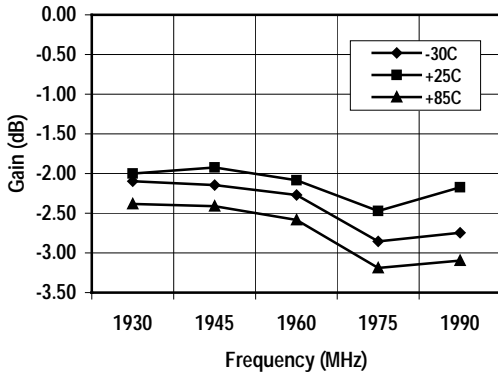
High Gain Low Linearity Mode  
Idd v Vdd v Temp



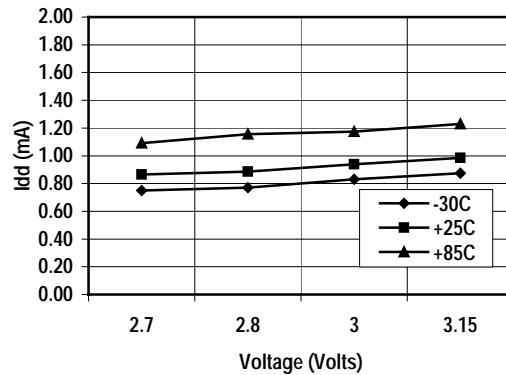
Bypass Mode  
Noise Figure v Freq v Temp



Bypass Mode  
Gain v Freq v Temp

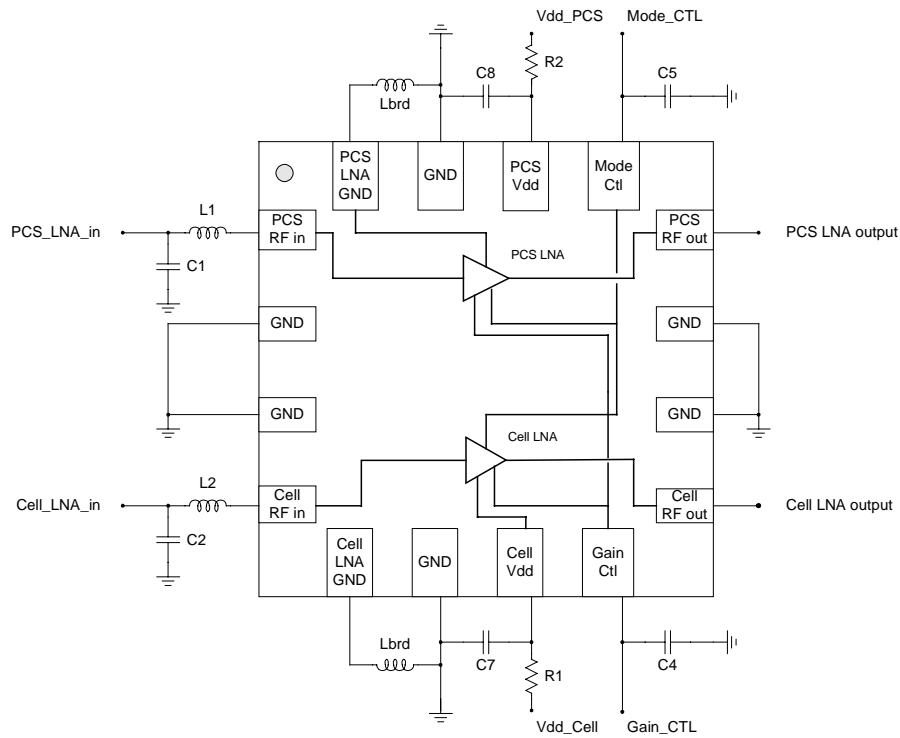


Bypass Mode  
Idd v Vdd v Temp



# TQ3M31 Data Sheet

## Application/Test Circuit



### Bill of Material for TQ3M31 LNA Application/Test Circuit

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC	U1	TQ3M31		Leadless 3x3mm	TriQuint Semiconductor
Capacitor	C1		1.2pF	0402	
Capacitor	C2		2.2pF	0402	
Capacitor	C3, C4, C5, C6		1000pF	0402	
Capacitor	C7		39pF	0402	
Capacitor	C8		10pF	0402	
Resistor	R1, R2		3.3Ω	0402	
Inductor	L1		4.7nH	0603	
Inductor	L2		18nH	0603	
Inductor	Lbrd		See application note		



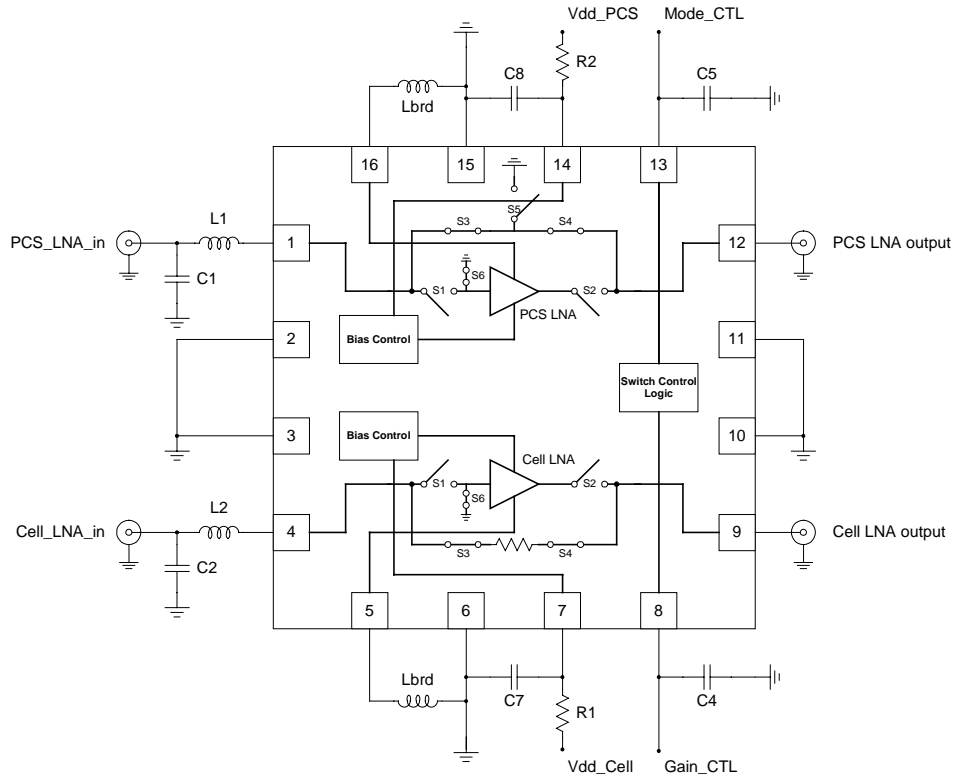
**TQ3M31 Product Description**

The TQ3M31 LNA uses two cascode low noise amplifiers along with signal path switching. Two bias control circuits set each LNA's quiescent current for each mode and ensure peak performance over process and temperature, see Figure 1. In the application, a switch control logic linked to the mode control and gain control pins sets the device to the desired mode. See Table 1 for truth table. Each LNA is selected by applying the supply voltage to the Vdd PCS or Cell pin as desired.

In the high-gain and high-gain-low-linearity modes, switches S1, S2, S5 (only on high band) and S6 are closed, with switches S3 and S4 opened. In the bypass mode, switches S1, S2, and S5 are opened, with switches S3, S4 and S6 closed. Internal switches ensure there are no parasitic feedback paths for the RF signal. In the AMPS mode, control logic switches the LNA into a low current bias condition.

Only four external components are needed for the input and output match of the LNA. The chip uses an external cap and inductor for each LNA input match to pin 1 and 4. The outputs are internally matched to 50 ohms at pin 12 and 9. A Vdd bypass cap is required close to each of the pins 7 and 14.

External degeneration of the cascode is required between pin 5&16 and ground. However, a small amount of PC board trace can be used as the inductor. Alternatively, if an extra component can be tolerated, a small value chip inductor could be used. See Figure 2



**Figure 1 TQ3M31 Simplified Schematic**

# TQ3M31

## Data Sheet

### Operation

MODE	Gain_Ctl	Mode Ctl	Cell Vdd	PCS Vdd	Typical gain
PCS HG	0	0	0	Vdd	13.5 (dB)
PCS HGLL	0	1	0	Vdd	11.5 (dB)
PCS Bypass	1	1	0	Vdd	-2 (dB)
Cell HG	0	0	Vdd	0	13 (dB)
Cell HGLL	0	1	Vdd	0	11 (dB)
Cell Bypass	1	1	Vdd	0	-5 (dB)

Table 1 LNA States and Control Bits

### LNA Input Network Design

Input network design for most LNA's is a straightforward compromise between noise figure and gain. The TQ3M31 is no exception, even though it has 3 different modes. The device was designed so that one only needs to optimize the input match in the high gain mode. As long as the proper grounding and source inductance are used, the other two modes will perform well with the same match.

It is probably wise to synthesize the matching network component values for some intermediate range of Gamma values, and then by experimentation, find the one which provides the best compromise between noise figure and gain. The quality of the chip ground will have some effect on the match, which is why some experimentation will likely be needed. The input match will affect the output match to some degree, so S22 should be monitored.

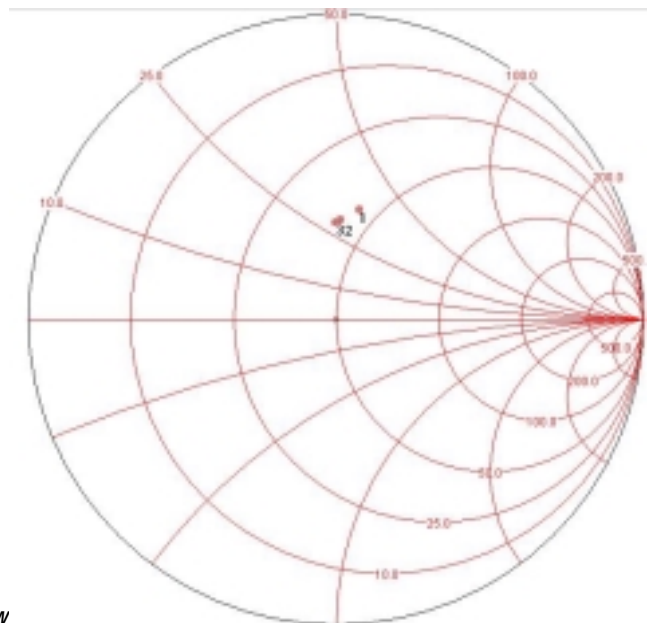
The values used on our evaluation board may be taken as a starting point. It has to be noted that another input match network was tested (PCS: 7pF series cap & 2.2nH shunt ind; Cell: 5.6nH series ind & 5.6nH shunt ind) but it proved to degrade the NF and IIP3.

### Noise Parameter Analysis

A noise parameter analysis is shown below for the high gain and HGLL modes. A "nominal" device was mounted directly on a standard evaluation board without matching network (through connected). The input reference plane was set at pin 1 & 4 and board loss was included in the calculations. C7 was set to 39pF and C8 to 18pF.

#### Gamma Opt analysis for TQ3M31 High Gain Mode – PCS band

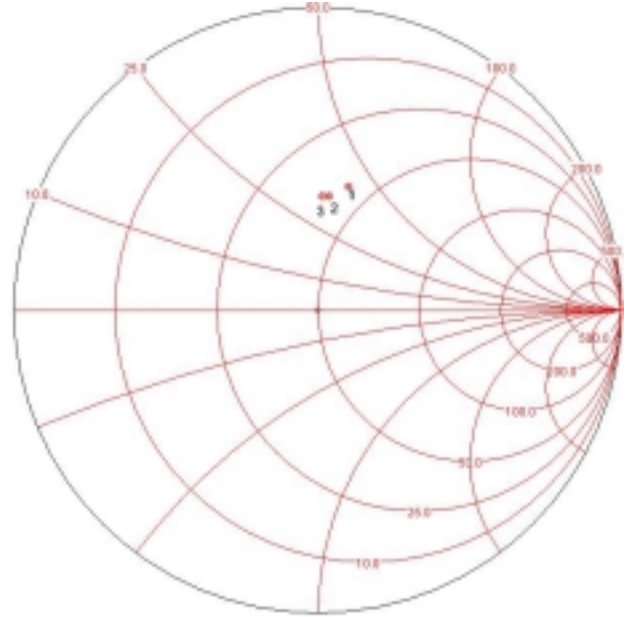
Freq. (MHz)	$\Gamma_{opt}$	$\Gamma_{angle}$	F min	R noise	Point#
1800	0.38	81.2	1.19	17.4	1
1960	0.33	86.6	1.23	17.0	2
2040	0.33	91.4	1.28	15.9	3



# TQ3M31 Data Sheet

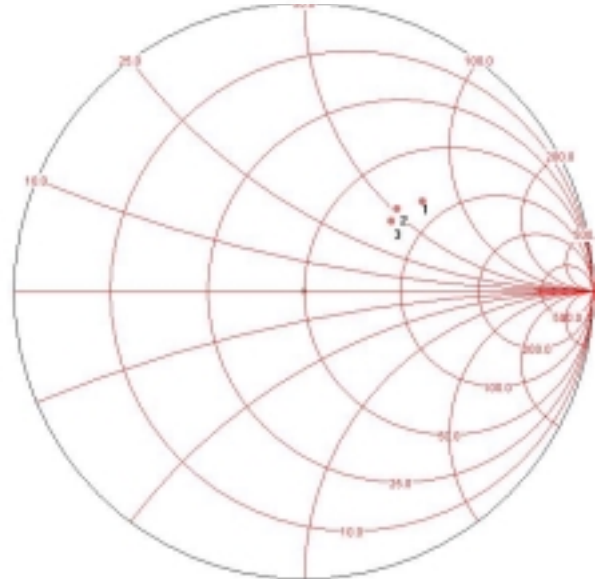
Gamma Opt analysis for TQ3M31 HGLL Mode – PCS band

Freq. (MHz)	$\Gamma_{opt}$	$\Gamma_{angle}$	F min	R noise	Point#
1800	0.46	77.0	1.61	27.2	1
1960	0.41	83.1	1.69	26.4	2
2040	0.40	86.7	1.75	24.1	3



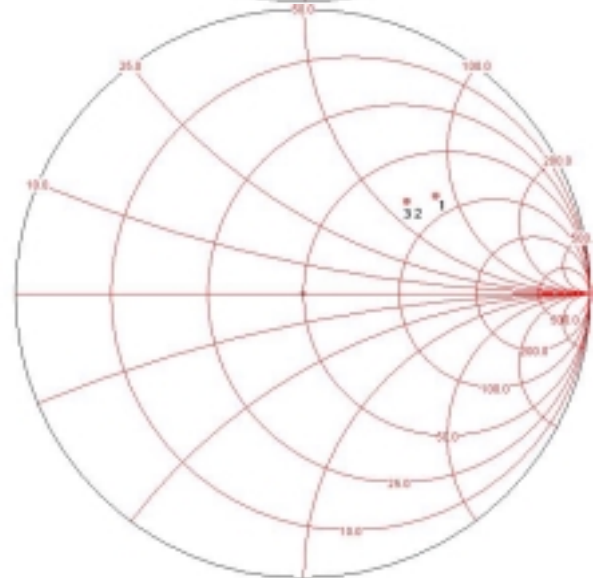
Gamma Opt analysis for TQ3M31 High Gain Mode – Cell band

Freq. (MHz)	$\Gamma_{opt}$	$\Gamma_{angle}$	F min	R noise	Point#
700	0.51	37.4	1.11	26.6	1
880	0.45	40.5	1.04	19.4	2
1000	0.41	41.0	1.15	19.3	3



Gamma Opt analysis for TQ3M31 HGLL Mode – Cell band

Freq. (MHz)	$\Gamma_{opt}$	$\Gamma_{angle}$	F min	R noise	Point#
700	0.57	36.9	1.52	43.8	1
880	0.50	40.2	1.40	31.4	2
1000	0.50	43.8	1.47	31.1	3



### ***Gain Control via Pin 5 & 16 Inductance***

The source connection of the LNA cascode is brought out separately through pin 5&16. That allows the designer to make some range of gain adjustment. The total amount of inductance present at the source of the cascode is equal to the bond wire plus package plus external inductance. One should generally use an external inductance such that gain in the high gain PCS mode = 13.5dB. Although it is possible to increase the gain of the TQ3M31, 3 effects are to be expected: the NF and IIP3 will be degraded, and the input match may not work for all modes at the same time anymore. The cell band LNA is especially sensitive to this effect.

Figure 2 shows how a rectangular PC board trace can be used as the external inductance. It is suggested that such a circuit be used for the initial design prototype. Then the optimum inductance can be found by simply solder bridging across the inductor. The final PC board design can then include the proper-shortened version of the inductor.

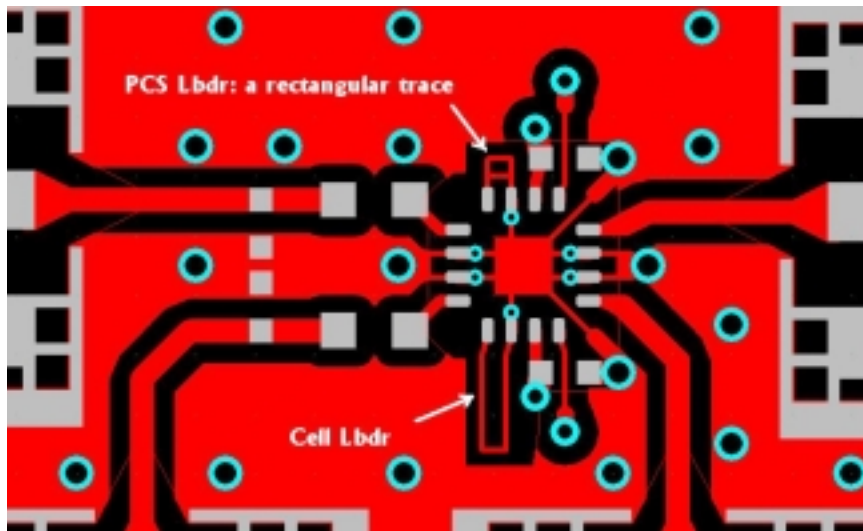


Figure 2 Showing Lbdr and Grounding on Evaluation Board

### ***Selection of the Vdd Bypass Cap for Optimum Performance***

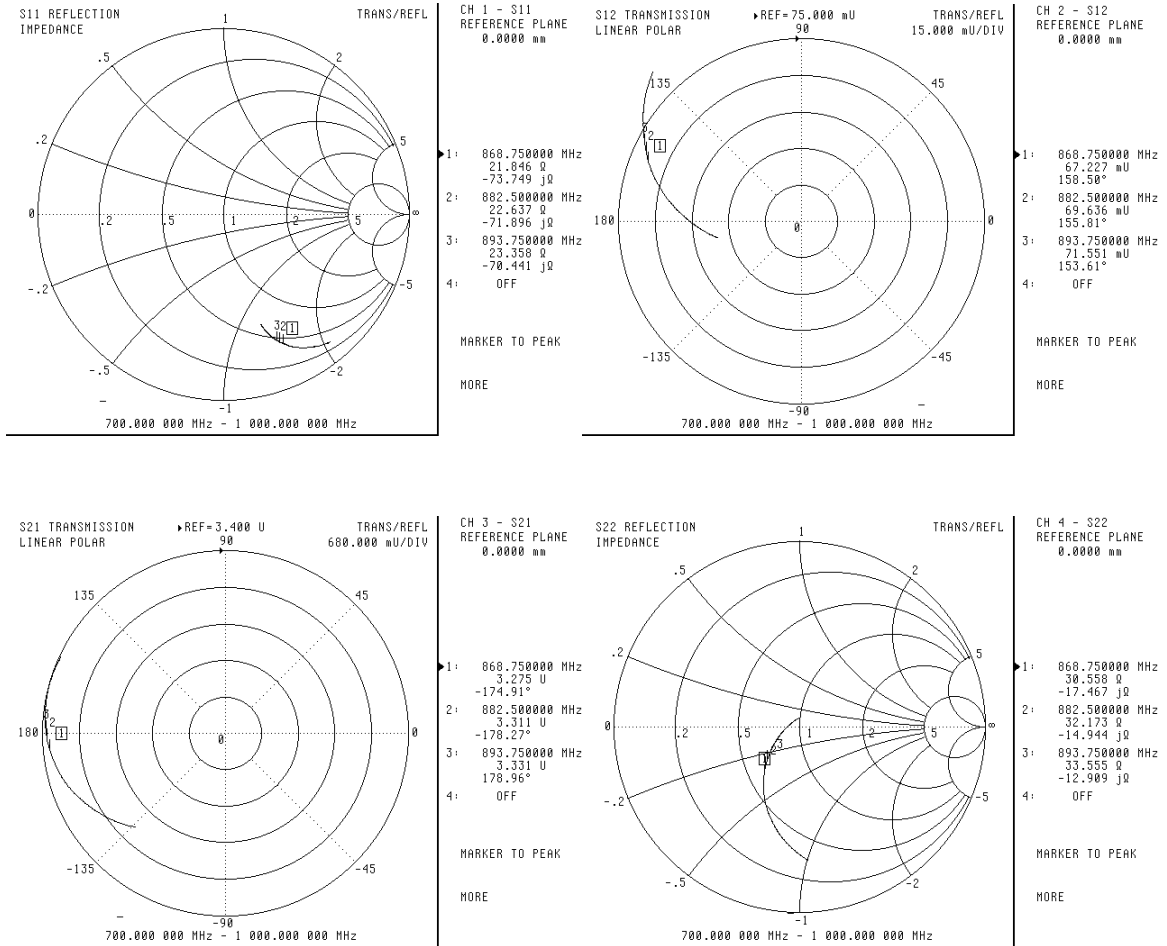
The Vdd bypass capacitor has the largest effect on the LNA output match, and is required for proper operation. Because the input match affects the output match to some degree as well, the process of picking the bypass cap value involves some iteration. First, an input match is selected which gives adequate gain and noise figure. Then the bypass capacitor is varied to give the best output match. The demo board achieves at least 12dB of return loss for the PCS band, and at least 11.5dB for the Cell band, which is adequate for connection directly to the input of a SAW filter.

### ***Grounding***

An optimal ground for the device is important in order to achieve datasheet specified performance. Symptoms of a poor ground include reduced gain and the inability to achieve <2:1 VSWR at the output when the input is matched. It is recommended to use multiple vias to a mid ground plane layer. The vias at pins 2, 3, 10 and 11 to this layer should be as close to the lead pads as possible. Additionally, the ground return on the Vdd bypass cap should provide minimal inductance back to chip pins 2, 3, 10 and 11.

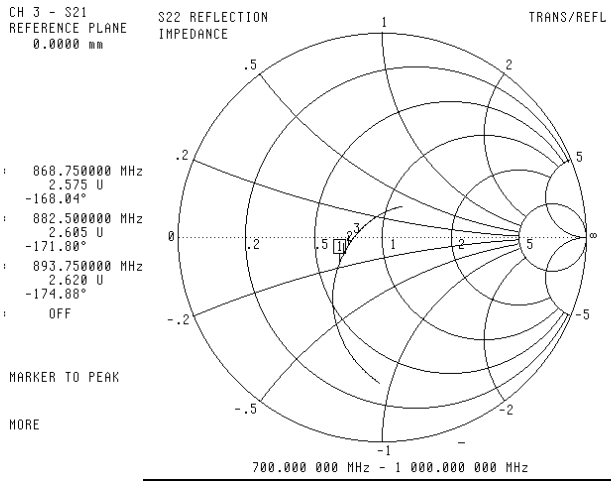
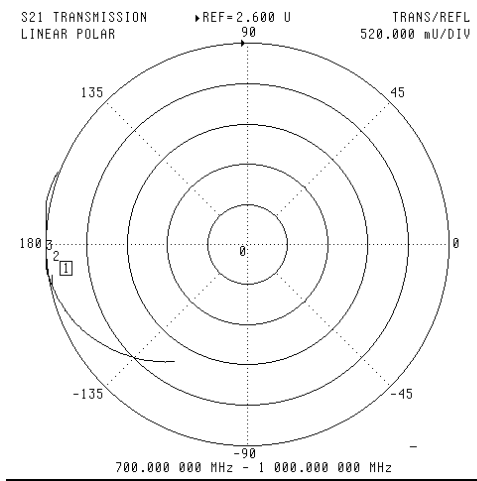
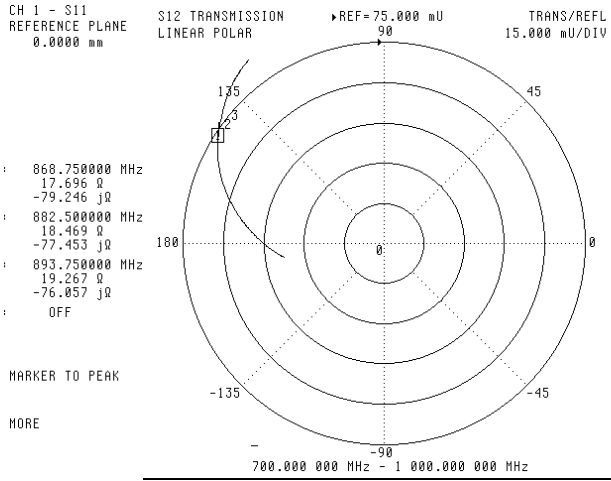
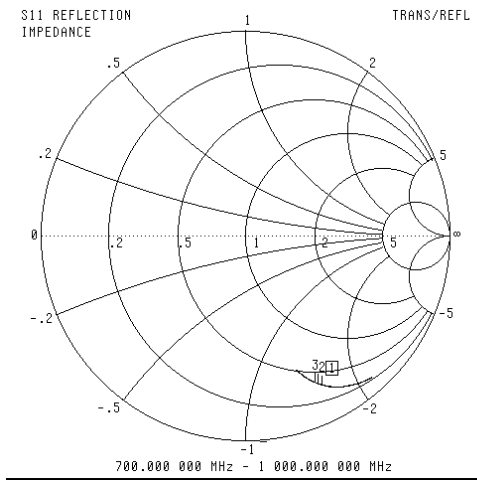
**TQ3M31 S-Parameters**

Following are S-Parameter graphs for the HG and HGLL modes in both bands. Data was taken on a single “nominal” device at 2.8V Vdd. The reference planes were set at the end of the package pins.

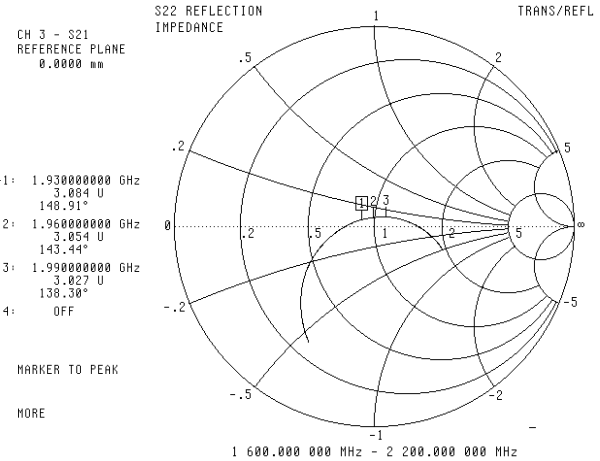
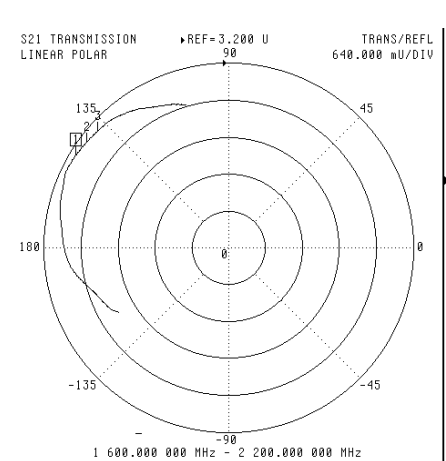
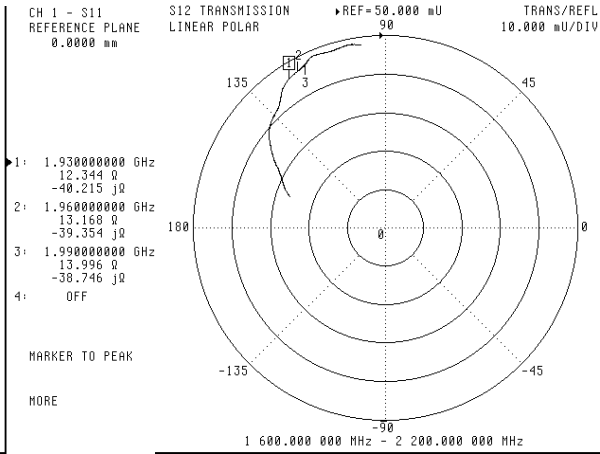
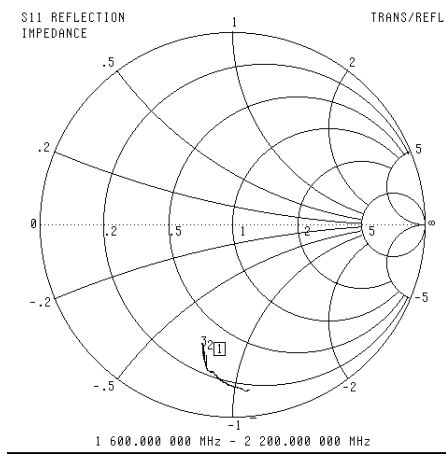


**Cell band - High Gain Mode S-parameters**

# TQ3M31 Data Sheet

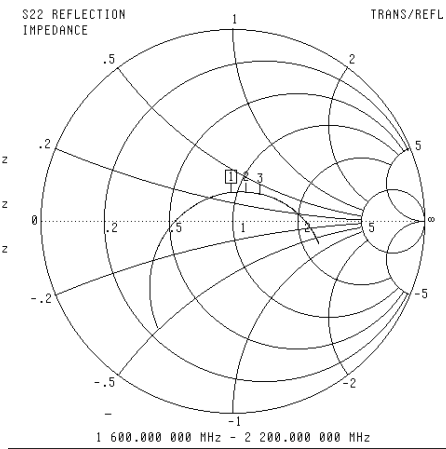
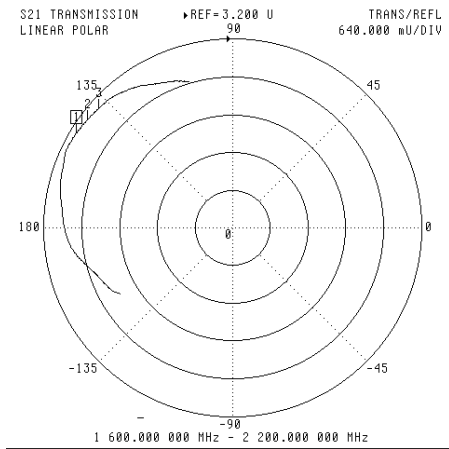
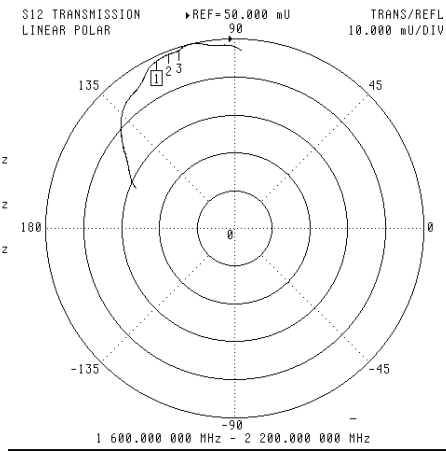
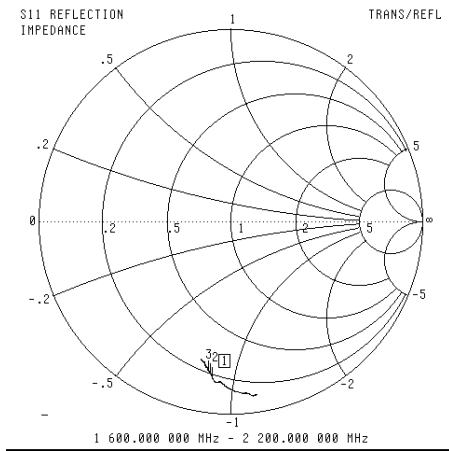


## Cell band - HGLL Mode S-Parameters



### PCS band - High Gain Mode S-parameters

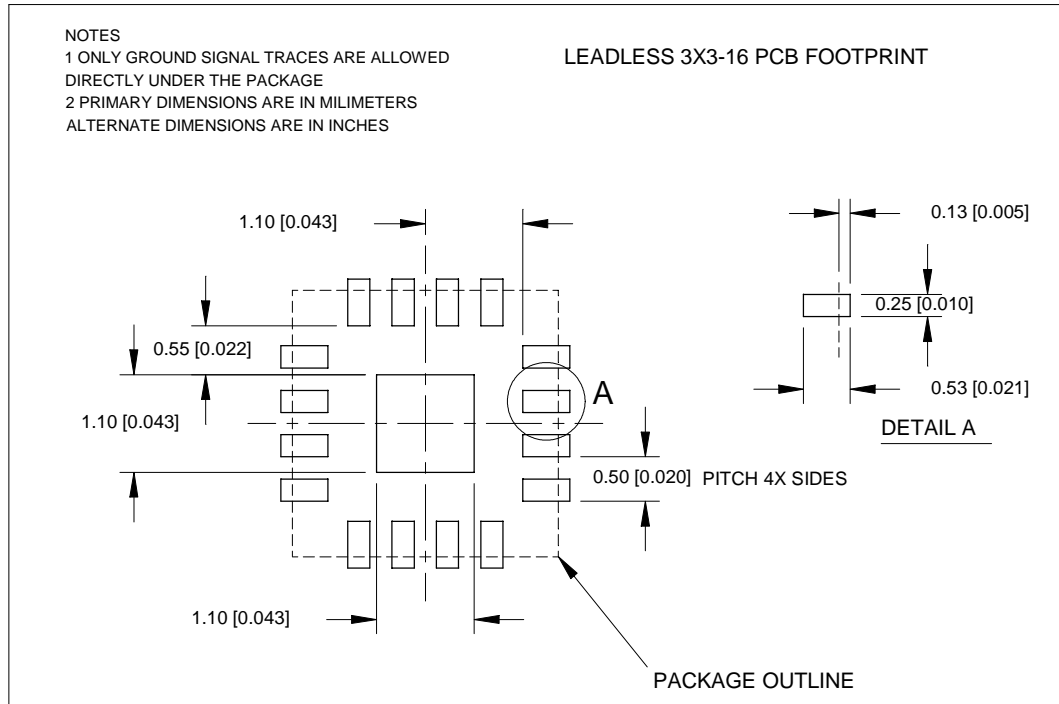
# TQ3M31 Data Sheet



## PCS band - HGLL Mode S-Parameters



*Leadless 3x3 mm Package*



---

**TQ3M31**  
**Data Sheet**

***Additional Information***

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

**Web:** [www.triquint.com](http://www.triquint.com)      **Tel:** (503) 615-9000  
**Email:** [info\\_wireless@tqs.com](mailto:info_wireless@tqs.com)      **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

**Email:** [info\\_wireless@tqs.com](mailto:info_wireless@tqs.com)

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party.

TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1998 TriQuint Semiconductor, Inc. All rights reserved.

Revision A, June, 2001