FEATURES

- **2-V to 12-V Single-Supply Operation**
- **Specified ON-State Resistance:**
  - **15 Ω Max With 12-V Supply**
  - **20 Ω Max With 5-V Supply**
  - **50 Ω Max With 3.3-V Supply**
- **Specified Low OFF-Leakage Currents:**
  - **1 nA at 25°C**
  - **10 nA at 85°C**
- **Specified Low ON-Leakage Currents:**
  - **1 nA at 25°C**
  - **10 nA at 85°C**
- **Low Charge Injection: 11.5 pC (12-V Supply)**
- **Fast Switching Speed:** **t_{ON} = 80 ns, t_{OFF} = 50 ns (12-V Supply)**
- **Break-Before-Make Operation (t_{ON} > t_{OFF})**
- **TTL/CMOS-Logic Compatible With 5-V Supply**

DESCRIPTION/ORDERING INFORMATION

The TS12A4514/TS12A4515 are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A4514 is normally open (NO). The TS12A4515 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2 V and 12 V. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

All digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5-V supply.

For pin-compatible parts for use with dual supplies, see the TS12A4516/TS12A4517.

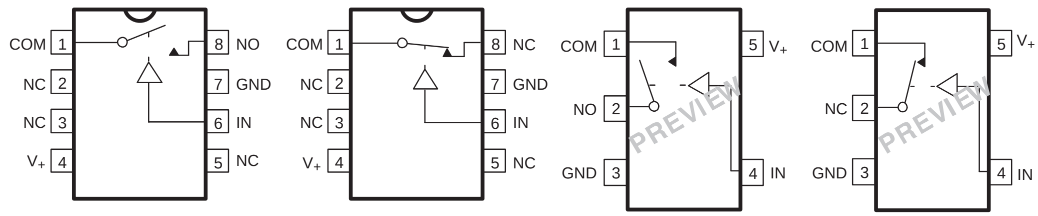
ORDERING INFORMATION

T_A	PACKAGE[(1)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Reel of 1000	TS12A4514P	TS12A4514P
	SOIC – D	Reel of 1500	TS12A4514D	YD514
		Reel of 2500	TS12A4514DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4514DBVR	PREVIEW
	PDIP – P	Reel of 1000	TS12A4515P	TS12A4515P
	SOIC – D	Reel of 1500	TS12A4515D	YD515
		Reel of 2500	TS12A4515DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4515DBVR	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

TS12A4514 D OR P PACKAGE (TOP VIEW) | **TS12A4515 D OR P PACKAGE (TOP VIEW)** | **TS12A4514 SOT-23 PACKAGE (TOP VIEW)** | **TS12A4515 SOT-23 PACKAGE (TOP VIEW)**



INPUT	SWITCH STATE	
	TS12A4514	TS12A4515
LOW	OFF	ON
HIGH	ON	OFF

MARKNG INFORMATION (SOTs only)
XXLXX → LOT SPECIFIC CODE
→ AE = TS12A4514
AF = TS12A4515

N.C. = Not internally connected
NO = Normally open

Absolute Minimum and Maximum Ratings[(1)(2)]

voltages referenced to GND

			MIN	MAX	UNIT
V_+	Supply voltage range[(3)]		–0.3	13	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[(4)]		–0.3	V_+ + 0.3 or ±20 mA	V
	Continuous current into any terminal			±20	mA
	Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle)			±30	mA
	ESD per method 3015.7			>2000	V
	Continuous power dissipation (T_A = 70°C)	8-pin plastic DIP (derate 9.09 mW/°C above 70°C)		727	mW
		8-pin SOIC (derate 5.88 mW/°C above 70°C)		471	
		5-pin SOT-23 (derate 7.1 mW/°C above 70°C)		571	
T_A	Operating temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Voltages exceeding V_+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 4.5 V, V_{COM} = 3.5 V, I_{COM} = 1 mA	25°C		9.5	15	Ω
			Full			20	
ON-state resistance flatness	$r_{on(flat)}$	V_{COM} = 1 V, 2 V, 3 V, I_{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
NO, NC OFF leakage current(3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
COM OFF leakage current(3)	$I_{COM(OFF)}$	V_+ = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
COM ON leakage current(3)	$I_{COM(ON)}$	V_+ = 5.5 V, V_{COM} = 4.5 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	2.4		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time	t_{ON}	see Figure 2	25°C		32	100	ns
			Full			125	
Turn-off time	t_{OFF}	see Figure 2	25°C		25	50	ns
			Full			60	
Charge injection(4)	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–3		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		19		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		475		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–94		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.08		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.05	µA
			Full			0.1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Electrical Characteristics for 12-V Supply[1]

V_+ = 11.4 V to 12.6 V, V_{INH} = 5 V, V_{INL} = 0.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP[2]	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 11.4 V, V_{COM} = 10 V, I_{COM} = 1 mA	25°C		6.5	10	Ω
			Full			15	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 11.4 V, V_{COM} = 2 V, 5 V, 10 V, I_{COM} = 1 mA	25°C		1.5	3	Ω
			Full			4	
NO, NC OFF leakage current[3]	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
COM OFF leakage current[3]	$I_{COM(OFF)}$	V_+ = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
COM ON leakage current[3]	$I_{COM(ON)}$	V_+ = 12.6 V, V_{COM} = 10 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	5		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.001	µA
Dynamic							
Turn-on time	t_{ON}	See Figure 2	25°C		22	75	ns
			Full			80	
Turn-off time	t_{OFF}	See Figure 2	25°C		20	45	ns
			Full			50	
Charge injection[4]	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–11.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		21.5		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		520		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–95		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.07		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.05	µA
			Full			0.2	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Electrical Characteristics for 3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 3 V, V_{COM} = 1.5 V, I_{NO} = 1 mA,	25°C		18.5	40	Ω
			Full			50	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 3 V, V_{COM} = 1 V, 1.5 V, 2 V, I_{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
NO, NC OFF leakage current(3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
COM OFF leakage current(3)	$I_{COM(OFF)}$	V_+ = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
COM ON leakage current(3)	$I_{COM(ON)}$	V_+ = 3.6 V, V_{COM} = 3 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	2.4		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time(4)	t_{ON}	See Figure 2	25°C		63	120	ns
			Full			175	
Turn-off time(4)	t_{OFF}	See Figure 2	25°C		33	80	ns
			Full			120	
Charge injection(4)	Q_C	C_L = 1 nF, See Figure 1	25°C		–1.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		17		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		460		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–94		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.15		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.03	µA
			Full			0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

PIN DESCRIPTION(1)

PIN NO.				NAME	DESCRIPTION
TS12A4514		TS12A4515			
D, P	SOT-23	D, P	SOT-23		
1	1	1	1	COM	Common
2, 3, 5	–	2, 3, 5	–	NC	No connect (not internally connected)
4	5	4	5	V_+	Power supply
6	4	6	4	IN	Digital control to connect COM to NO or NC
7	3	7	3	GND	Digital ground
8	2	–	–	NO	Normally open
–	–	8	2	NC	Normally closed

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

APPLICATION INFORMATION

Power-Supply Considerations

The TS12A4514/TS12A4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V_+ and GND. V_+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V_+ and GND. One of these diodes conducts if any analog signal exceeds V_+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V_+ or GND. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either V_+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V_+ or GND.

V_+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V_+ and GND signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V_+ is 5 V. As V_+ is raised, the level threshold increases slightly. When V_+ reaches 12 V, the level threshold is about 3 V – above the TTL-specified high-level minimum of 2.8 V, but still compatible with CMOS outputs.

CAUTION:

Do not connect the TS12A4514/MAS4515 V_+ to 3 V and then connect the logic-level pins to logic-level signals that operate from 5-V supply. Output levels can exceed 3 V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50-Ω systems, signal response is reasonably flat up to 250 MHz (see *Typical Operating Characteristics*). Above 20 MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it is turning it off. The OFF-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10 MHz, OFF isolation is about –45 dB in 50-Ω systems, decreasing (approximately 20 dB per decade) as frequency increases. Higher circuit impedances also make OFF isolation decrease. OFF isolation is about 3 dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

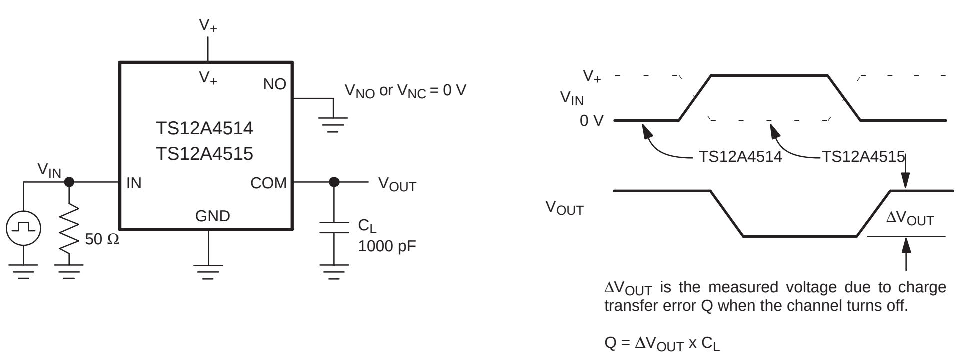


Figure 1. Charge Injection

APPLICATION INFORMATION (continued)

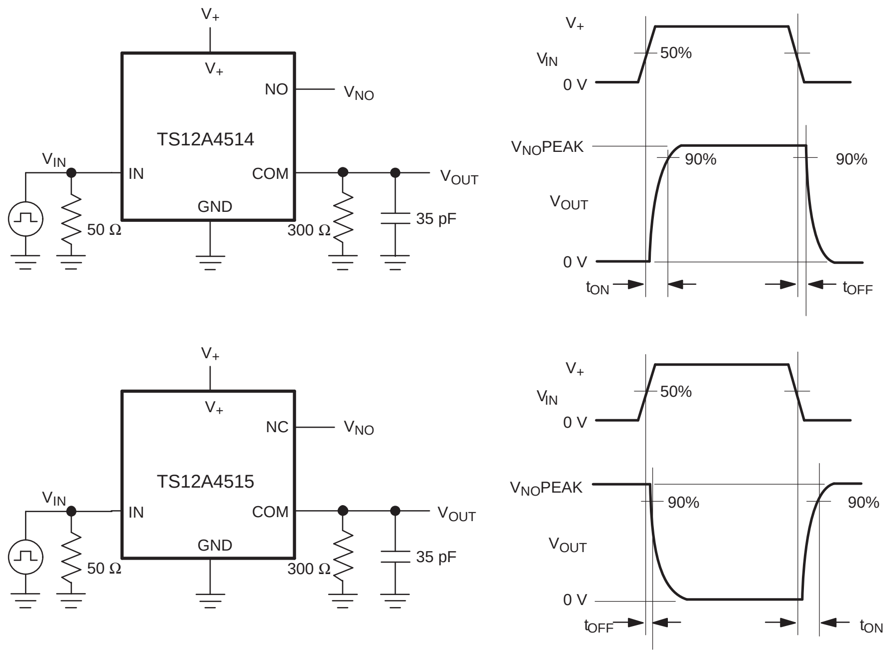
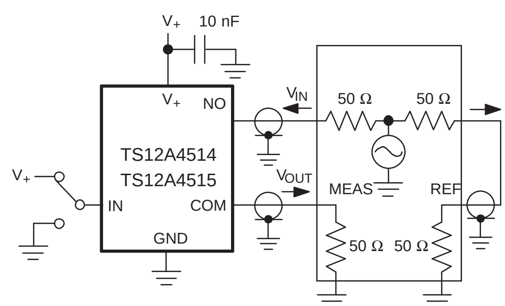


Figure 2. Switching Times



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20\log\frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20\log\frac{V_{OUT}}{V_{IN}}$$

Figure 3. OFF Isolation and ON Loss

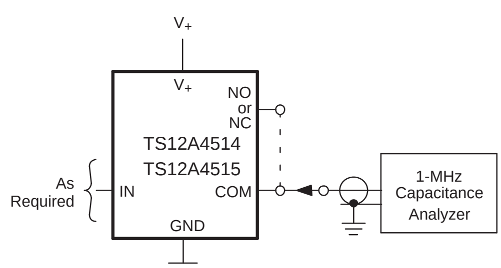


Figure 4. NO, NC, and COM Capacitance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS12A4514D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4514DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4514DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4514DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4514P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TS12A4514PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TS12A4515D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4515DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4515DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4515DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS12A4515P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TS12A4515PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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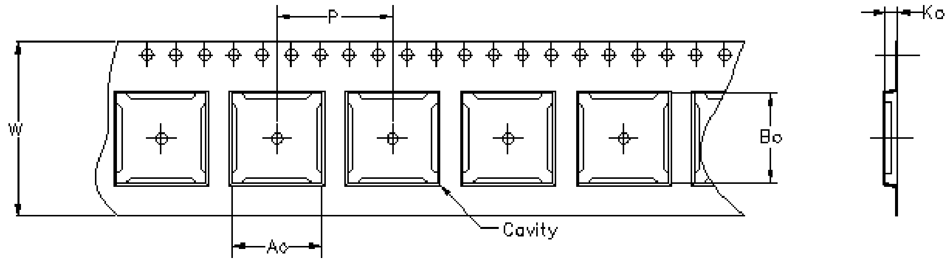
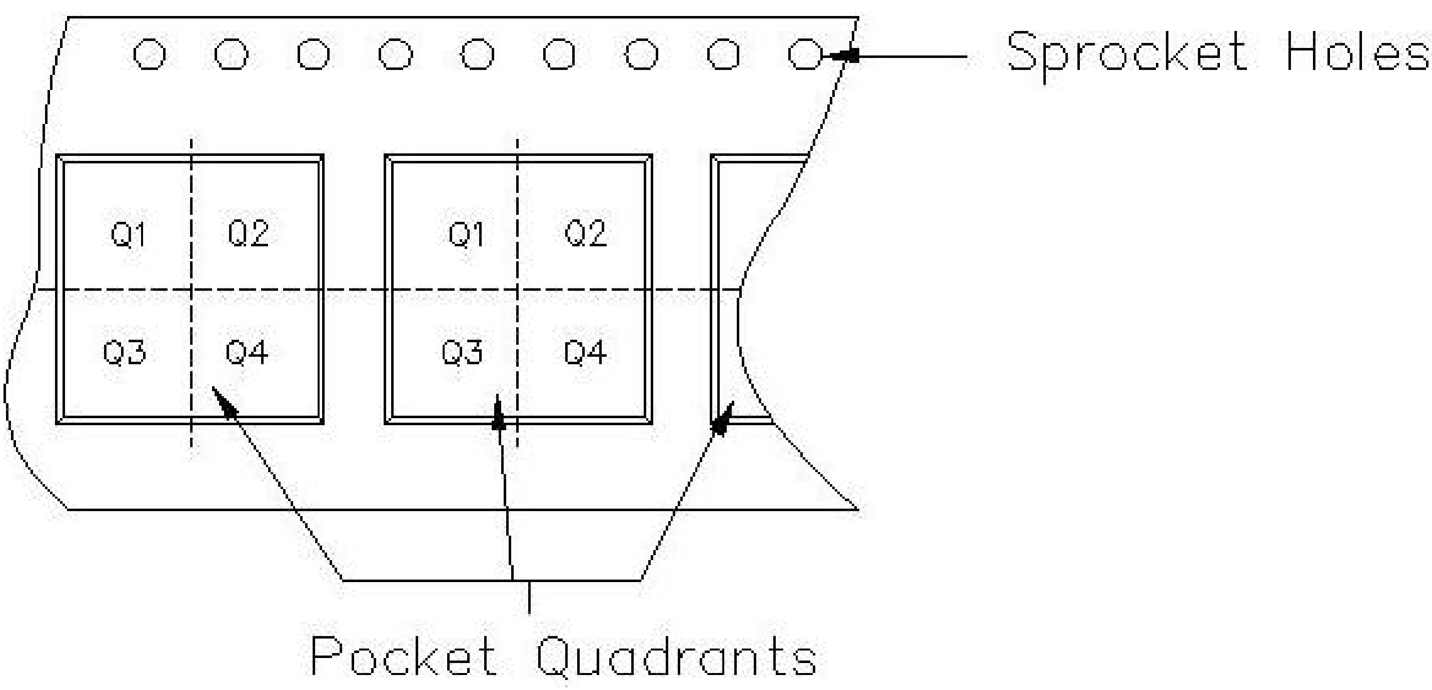


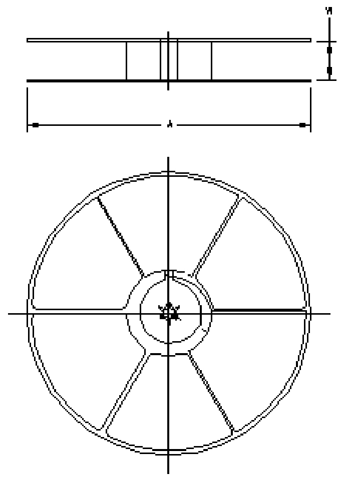
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



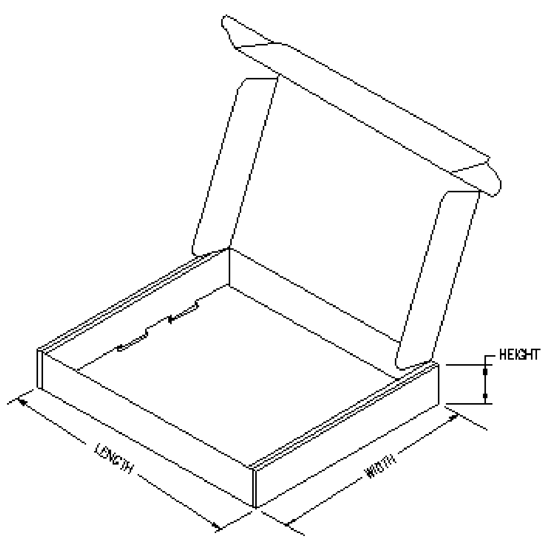
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A4514DR	D	8	MLA	330	12	6.4	5.2	2.1	8	12	Q1
TS12A4515DR	D	8	MLA	330	12	6.4	5.2	2.1	8	12	Q1

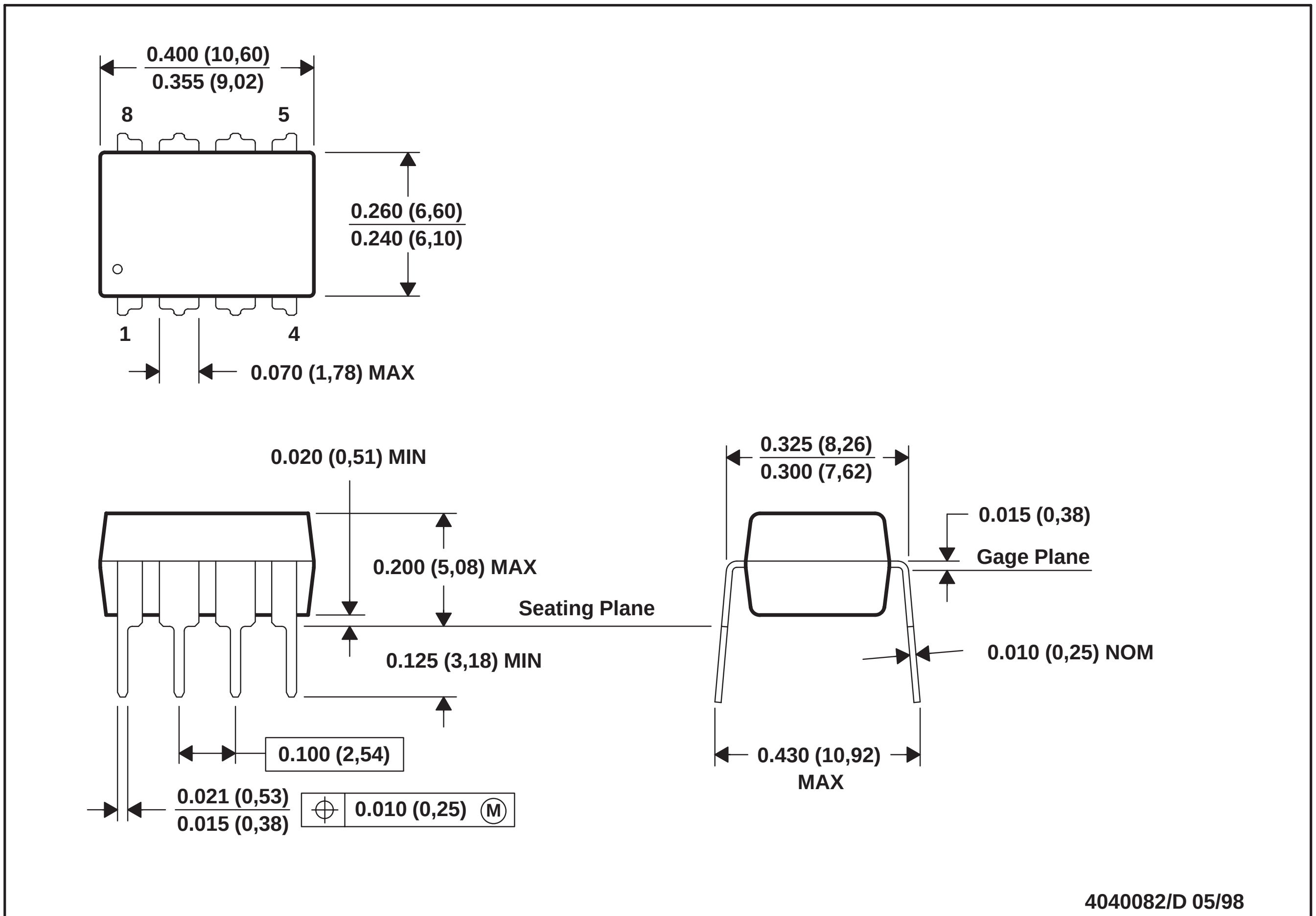


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TS12A4514DR	D	8	MLA	338.1	340.5	20.64
TS12A4515DR	D	8	MLA	338.1	340.5	20.64

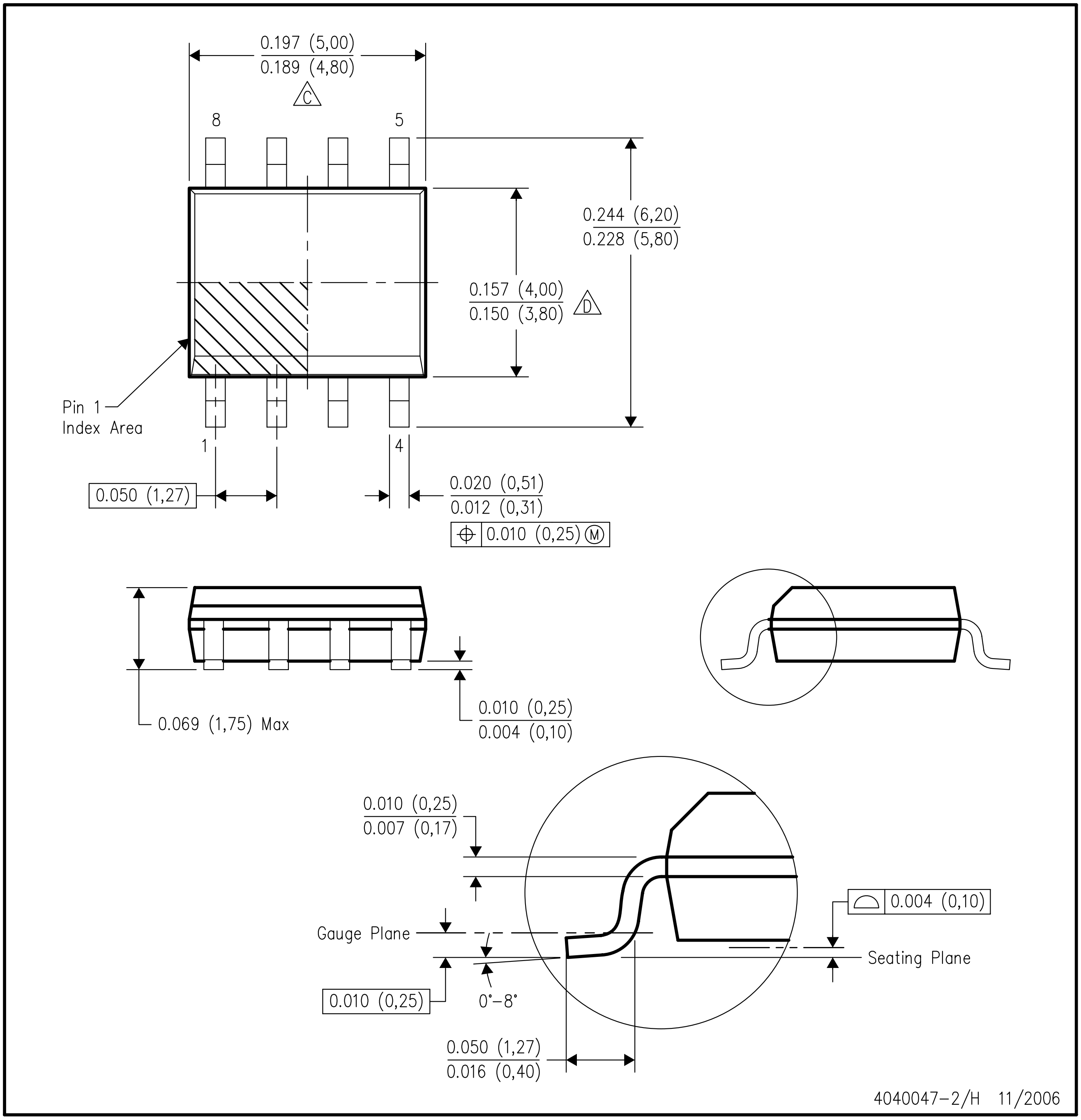


P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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