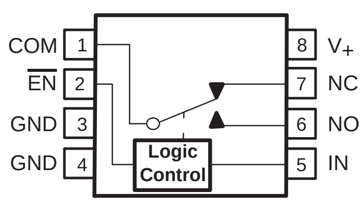
Description

The TS5A3153 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent on-resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

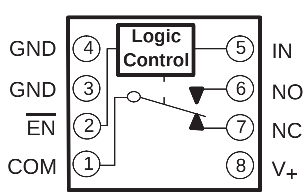
Applications

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio and Video Signal Routing**
- **Low-Voltage Data Acquisition System**
- **Communication Circuits**
- **Modems**
- **Hard Drives**
- **Computer Peripherals**
- **Wireless Terminals and Peripherals**

SSOP OR VSSOP PACKAGE (TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE (BOTTOM VIEW)



Features

- **Isolation in the Powered-Off Mode, V_+ = 0**
- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (1 Ω)**
- **Control Inputs Are 5.5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

Summary of Characteristics

V_+ = 5 V, T_A = 25°C

Configuration	2:1 Multiplexer/ Demultiplexer (SPDT)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	20 ns/15 ns
Break-before-make time (t_{BBM})	12 ns
Charge injection (Q_C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	−65 dB at 1 MHz
Crosstalk (X_{TALK})	−66 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/I_{NO(OFF)}$)	±20 nA
Power-supply current (I_+)	0.1 µA
Package option	8-pin SSOP, VSSOP, or DSBGA

FUNCTION TABLE

$\overline{EN}$	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[2]
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17−mm Small Bump − YEA	Tape and reel	TS5A3153YEAR	PREVIEW
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		TS5A3153YZAR	PREVIEW
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		TS5A3153YEPR	PREVIEW
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		TS5A3153YZPR	PREVIEW
	SSOP − DCT	Tape	TS5A3153DCT	PREVIEW
	VSSOP − DCU	Tape and reel	TS5A3153DCUR	JCD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Absolute Minimum and Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[3]		−0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[3][4][5]		−0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	−50		mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	−200	200	mA
	On-state peak switch current[6]		−400	400	
V_I	Digital input voltage range[3][4]		−0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100	100	mA
θ_{JA}	Package thermal impedance[7]	DCT package		220	°C/W
		DCU package		227	
		YEA/YZA package		140	
		YEP/YZP package		102	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1 ms duration < 10% duty cycle
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −100 mA,	Switch ON, See Figure 13	25 °C	4.5 V		0.9	1.1	Ω
				Full				1.3	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.8	0.9	Ω
				Full				1.1	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.05	0.10	Ω
				Full				0.10	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.15		Ω
				Full					
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C			0.09	0.15	
				Full				0.15	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	−20	2	20	nA
				Full		−150		150	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−5	0.7	5	µA
				Full		−25		25	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	−20	2	20	nA
				Full		−150		150	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V, or V_{NC} or V_{NO} = 1 V, V_{COM} = 4.5 V,	Switch ON, See Figure 14	25°C	5.5 V	−20	2	20	nA
				Full		−150		150	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−5	0.7	5	µA
				Full		−25		25	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 4.5 V,	Switch ON, See Figure 15	25°C	5.5 V	−20	2	20	nA
				Full		−150		150	
Digital Control Inputs (IN, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	−100	25	100	nA
				Full		−100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	5 V	1	12.5	16	ns
				Full	4.5 V to 5.5 V	1		17.5	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	5 V	2.5	8.5	15	ns
				Full	4.5 V to 5.5 V	2		18	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 18	25°C	5 V	1	7	12	ns
				Full	4.5 V to 5.5 V	0.5		15	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, C_L = 1 nF,	See Figure 22	25°C	5 V		12		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		19		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		57		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		57		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 19	25°C	5 V		97		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 20	25°C	5 V		−64		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch ON, See Figure 21	25°C	5 V		−64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	5 V		0.004		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		0.02	0.10	µA
				Full				0.50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −100 mA,	Switch ON, See Figure 13	25 °C	3 V		1.3	1.6	Ω
				Full				1.8	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	3 V		1.2	1.5	Ω
				Full				1.7	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	3 V		0.08	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C	3 V		0.2		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = 100 mA,	Switch ON, See Figure 13	25°C			0.09	0.15	
				Full				0.15	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−20	2	20	nA
				Full		−50		50	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.2	1	µA
				Full		−15		15	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	−20	2	20	nA
				Full		−50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V, or V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V,	Switch ON, See Figure 14	25°C	3.6 V	−20	2	20	nA
				Full		−50		50	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 3.6 to 0 V, V_{COM} = 0 to 3.6 V,	Switch OFF, See Figure 14	25°C	0 V	−1	0.2	1	µA
				Full		−15		15	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 15	25°C	3.6 V	−20	2	20	nA
				Full		−50		50	
Digital Control Inputs (IN, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	−100	25	100	nA
				Full		−100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply(1) (continued)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1	17	22	ns
				Full	3 V to 3.6 V	1		24	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.3	9.5	16	ns
				Full	3 V to 3.6 V	4		19	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	2	12	22	ns
				Full	3 V to 3.6 V	1		25	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF,	See Figure 22	25°C	3.3 V		8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		57		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		57		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	3.3 V		97		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 20	25°C	3.3 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 21	25°C	3.3 V		−64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	3.3 V		0.010		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.10	μA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = −8 mA,	Switch ON, See Figure 13	25 °C	2.3 V		1.9	2.5	Ω
				Full				2.7	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = 8 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.6	2.1	Ω
				Full				2.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.8 V, I_{COM} = 8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.12	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = 8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.65		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = 8 mA,	Switch ON, See Figure 13	25°C			0.5	1	
				Full				1	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	−20	2	20	nA
				Full		−50		50	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.1	1	μA
				Full		−10		10	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	−20	2	20	nA
				Full		−50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V, or V_{NO} = 0.5 V, V_{COM} = 2.2 V,	Switch ON, See Figure 14	25°C	2.7 V	−20	2	20	nA
				Full		−50		50	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,	Switch OFF, See Figure 14	25°C	0 V	−1	0.1	1	μA
				Full		−10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See Figure 15	25°C	2.7 V	−20	2	20	nA
				Full		−50		50	
Digital Control Inputs (IN, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	−100	25	100	nA
				Full		−100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	1.7	24	31	ns
				Full	2.3 V to 2.7 V	1.5		33.5	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	5.2	10.5	17	ns
				Full	2.3 V to 2.7 V	5		20	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	3	10	30	ns
				Full	2.3 V to 2.7 V	2		40	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF,	See Figure 22	25°C	2.5 V		6		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		57		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		57		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	2.5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 20	25°C	2.5 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 21	25°C	2.5 V		−64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	2.5 V		0.020		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.05	μA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = −2 mA,	Switch ON, See Figure 13	25°C	1.65 V		5.2	15	Ω
				Full				20	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = 2 mA,	Switch ON, See Figure 13	25°C	1.65 V		2	2.7	Ω
				Full				3.1	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = 2 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.16	0.3	Ω
				Full				0.3	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = 2 mA,	Switch ON, See Figure 13	25°C	1.65 V		3		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = 2 mA,	Switch ON, See Figure 13	25°C			3	6	
				Full				8	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 14	25°C	1.95 V	−20	1.5	20	nA
				Full		−50		50	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.1	1	μA
				Full		−10		10	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	−20	1.5	20	nA
				Full		−50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V,	Switch ON, See Figure 14	25°C	1.95 V	−20	1.5	20	nA
				Full		−50		50	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V,	Switch OFF, See Figure 14	25°C	0 V	−1	0.06	1	μA
				Full		−10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 15	25°C	1.95 V	−20	1.5	20	nA
				Full		−50		50	
Digital Control Inputs (IN, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	−100	25	100	nA
				Full		−100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	4.5	45	61	ns
				Full	1.65 V to 1.95 V	4		63	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5.4	12	19	ns
				Full	1.65 V to 1.95 V	5		21	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	4	31	60	ns
				Full	1.65 V to 1.95 V	3		65	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF,	See Figure 22	25°C	1.8 V		4		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		57		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		57		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 19	25°C	1.8 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 20	25°C	1.8 V		−64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 21	25°C	1.8 V		−64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	1.8 V		0.060		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.05	μA
				Full				0.1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

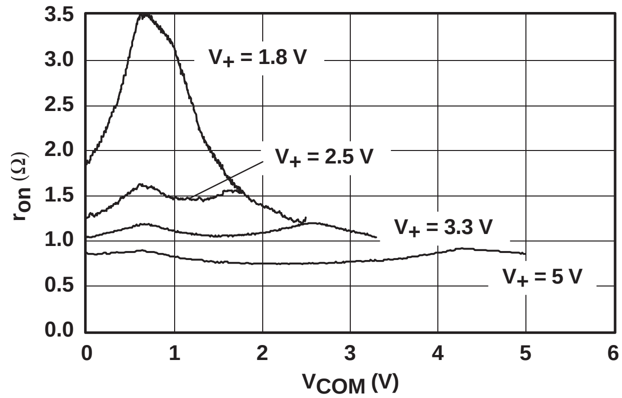


Figure 1. r_{on} vs V_{COM}

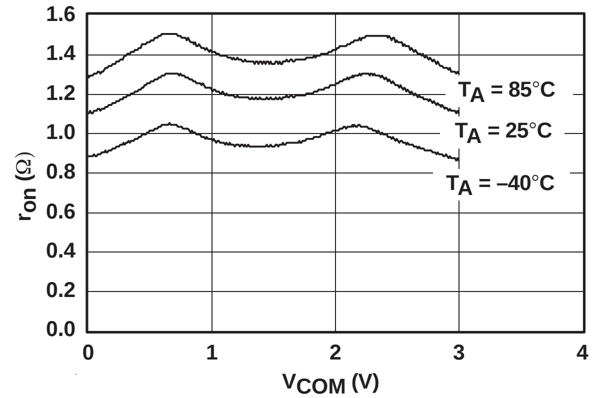


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

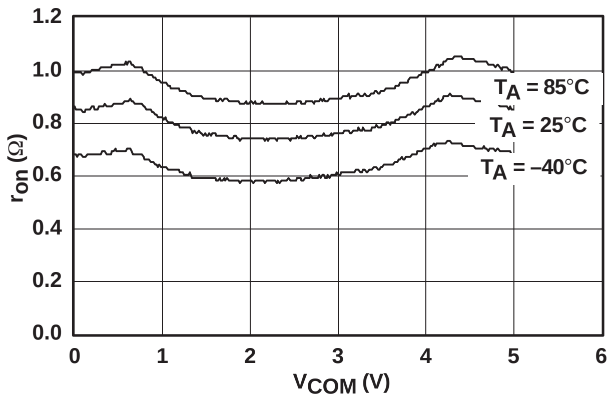


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

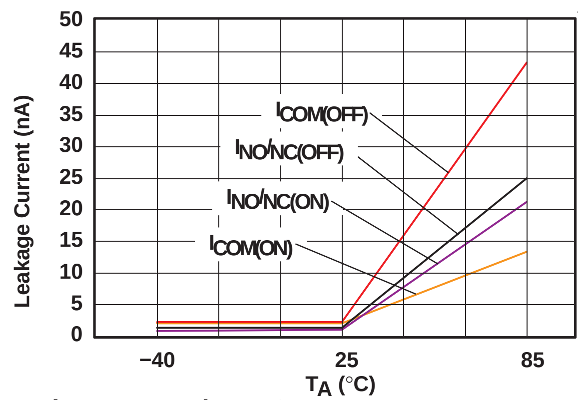


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

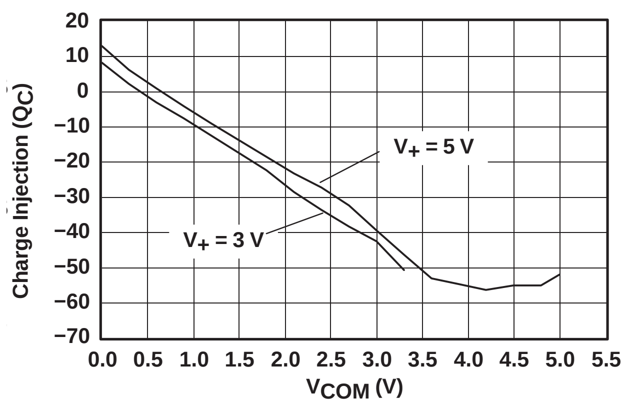


Figure 5. Charge Injection (Q_C) vs V_{COM}

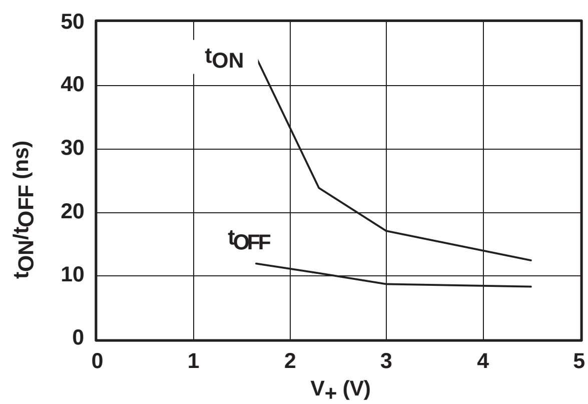


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE

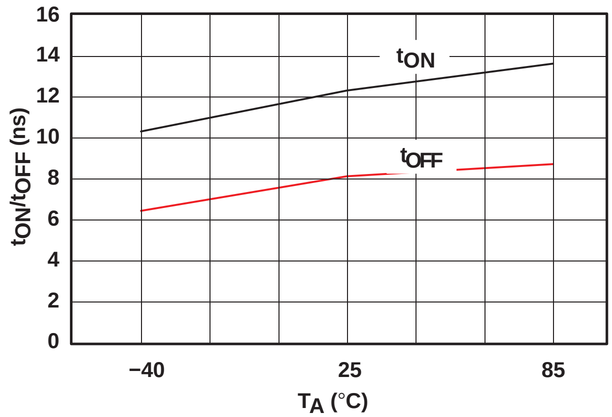


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 4.5 V)

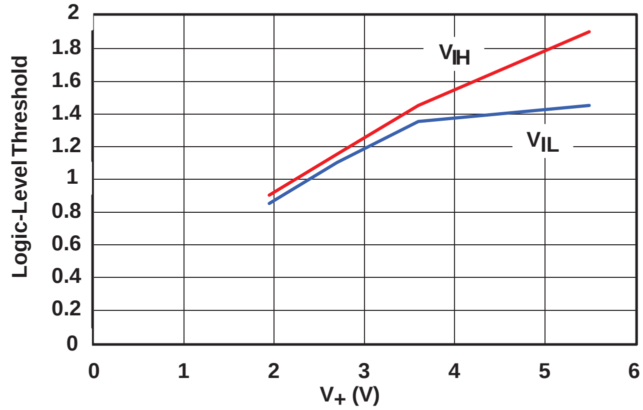


Figure 8. Logic-Level Threshold vs V_+

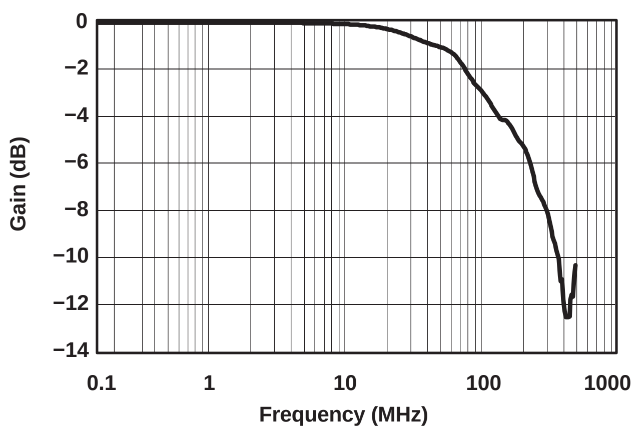


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

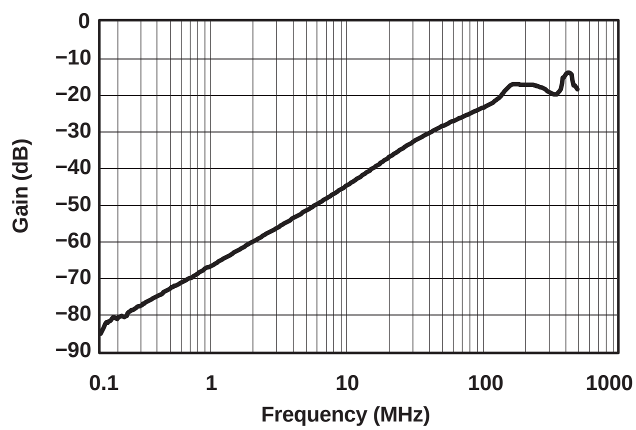


Figure 10. OFF Isolation vs Crosstalk (V_+ = 5 V)

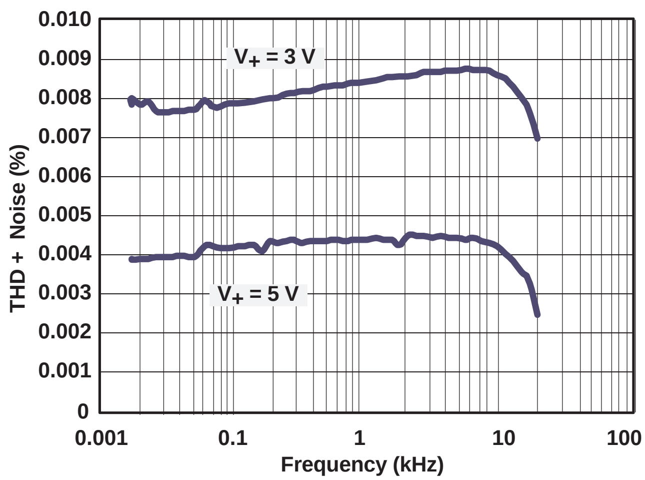


Figure 11. Total Harmonic Distortion vs Frequency

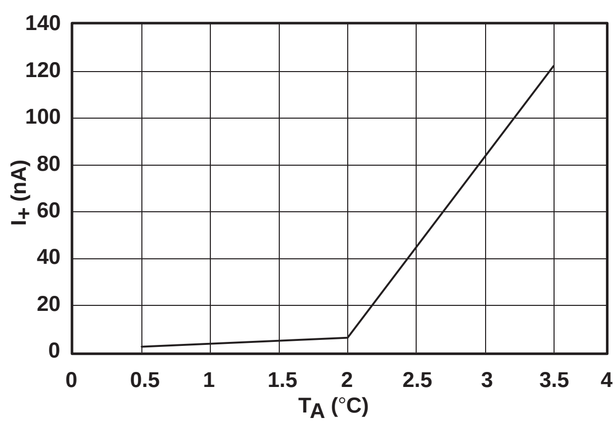


Figure 12. Power-Supply Current vs Temperature (V = 5 V)

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	COM	Common
2	$\overline{EN}$	Enable control input
3	GND	Digital ground
4	GND	Digital ground
5	IN	Digital control to connect COM to NO or NC
6	NO	Normally open
7	NC	Normally closed
8	V_+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-off condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-off condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the OFF state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-off condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is OFF
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN, $\overline{EN}$) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

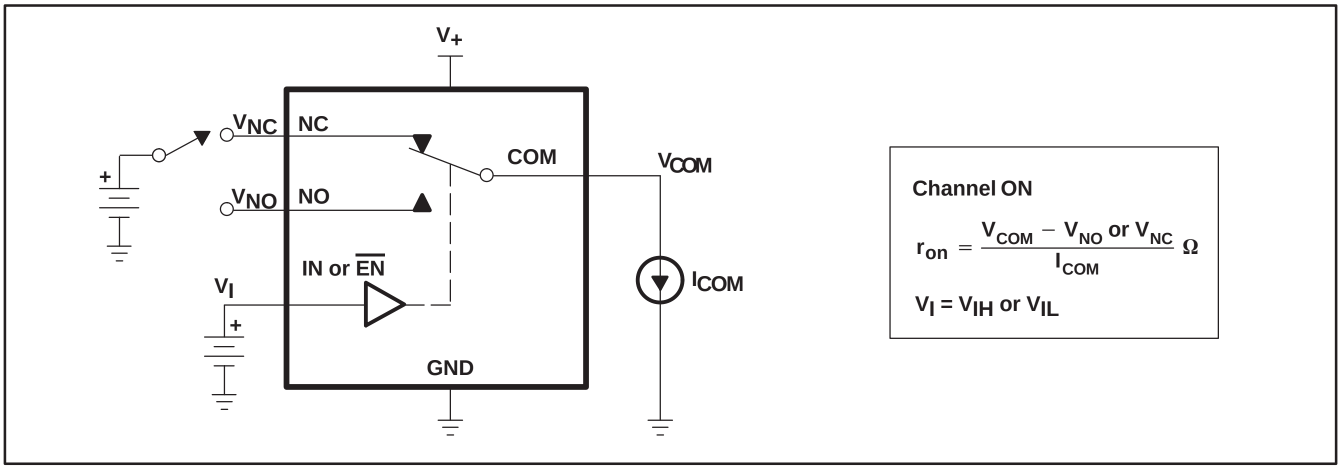


Figure 13. ON-State Resistance (r_{on})

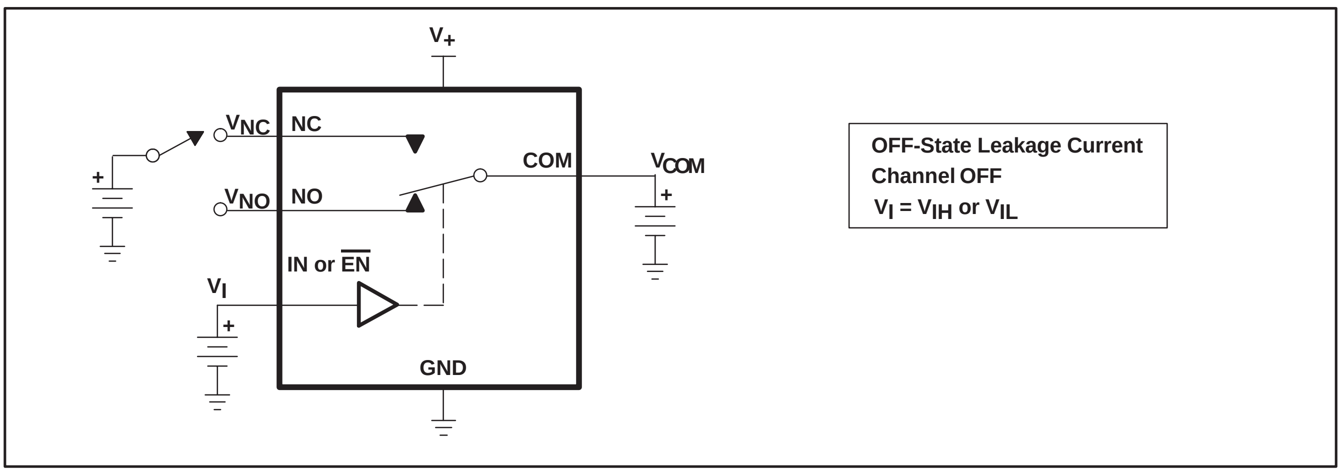


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(PWROFF)}$)

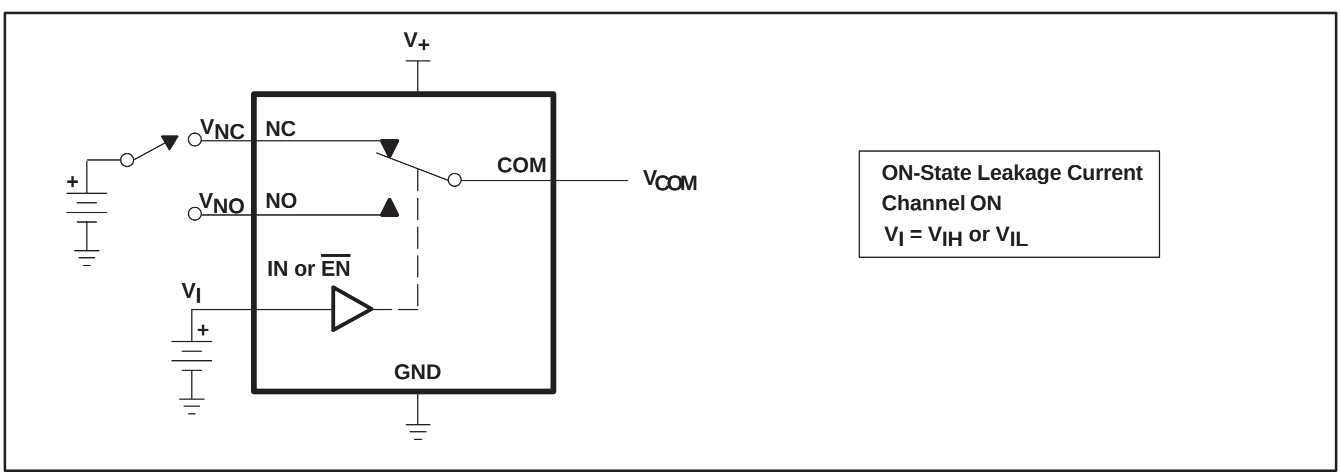


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

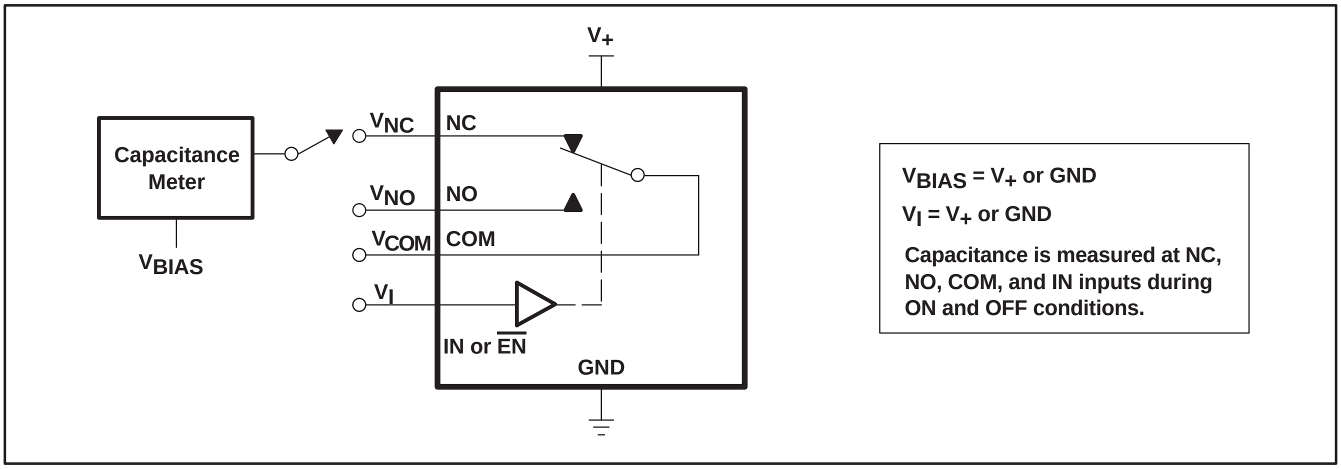
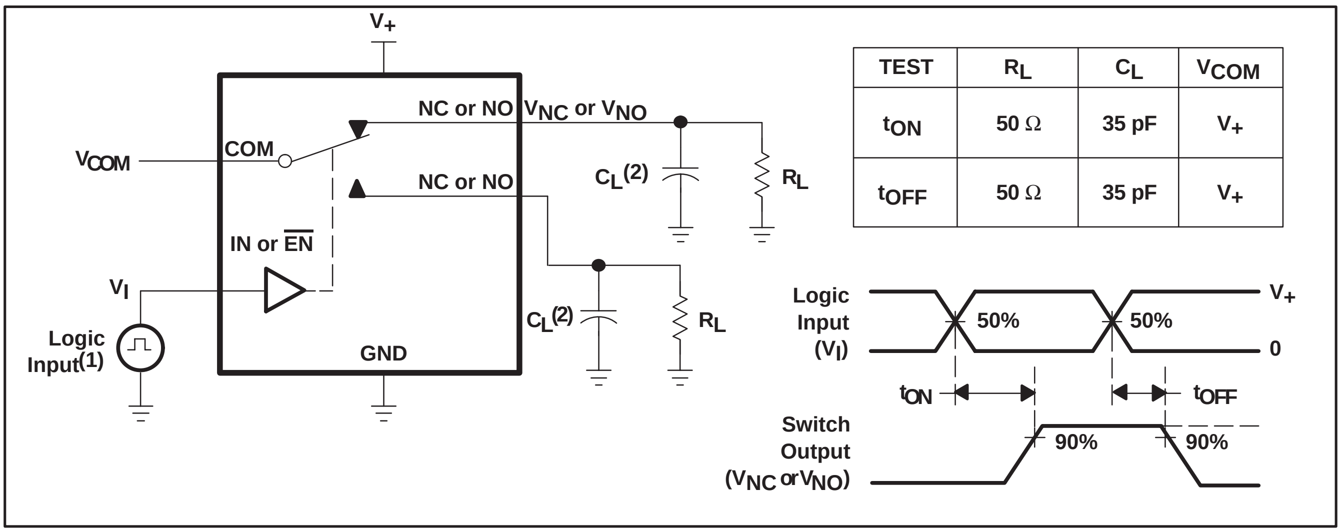


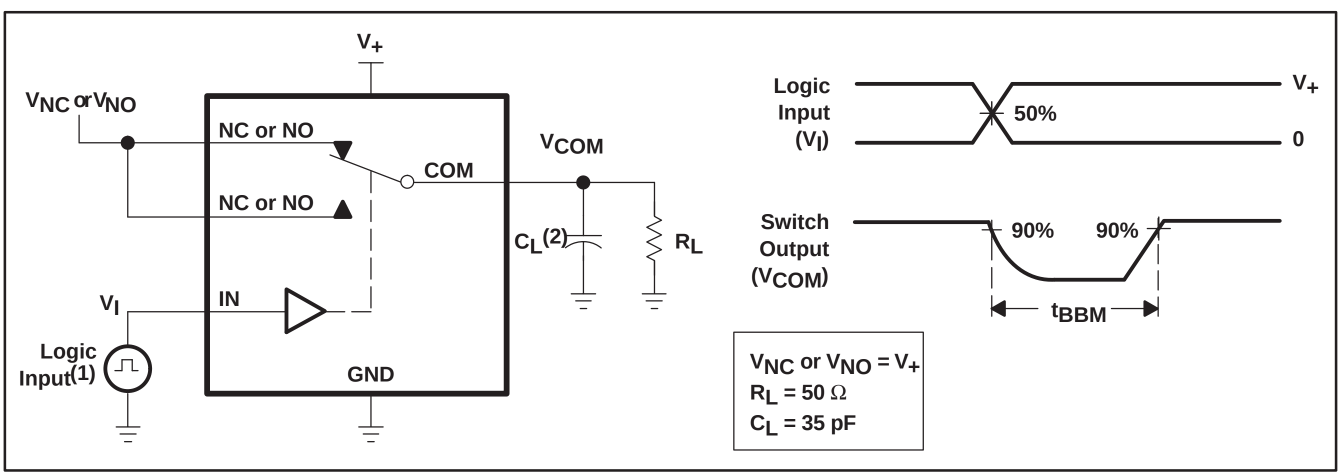
Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V+
t_{OFF}	50 Ω	35 pF	V+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 18. Break-Before-Make Time (t_{BBM})

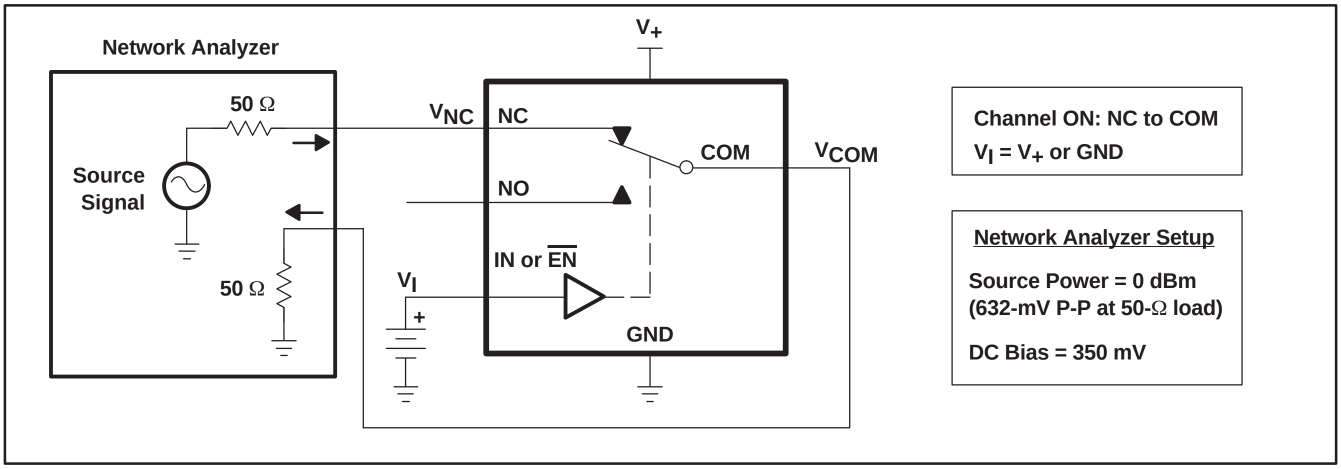


Figure 19. Bandwidth (BW)

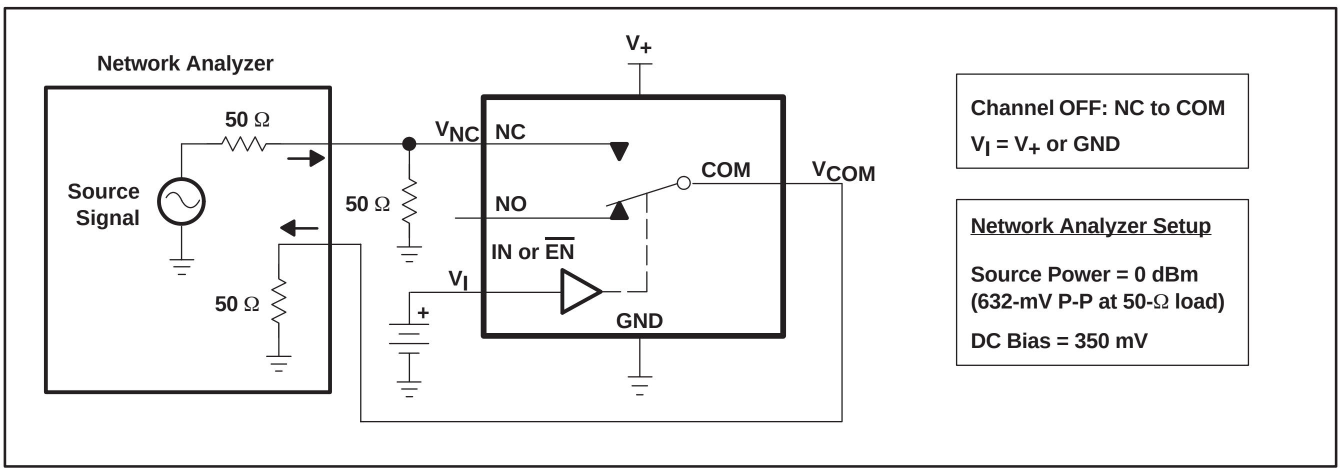


Figure 20. OFF Isolation (O_{ISO})

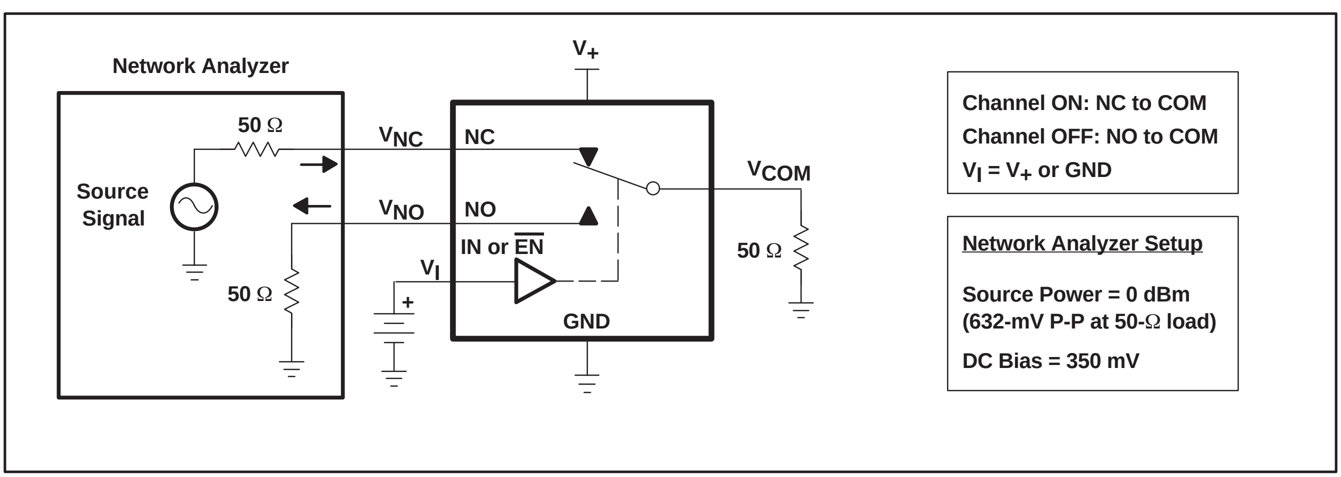
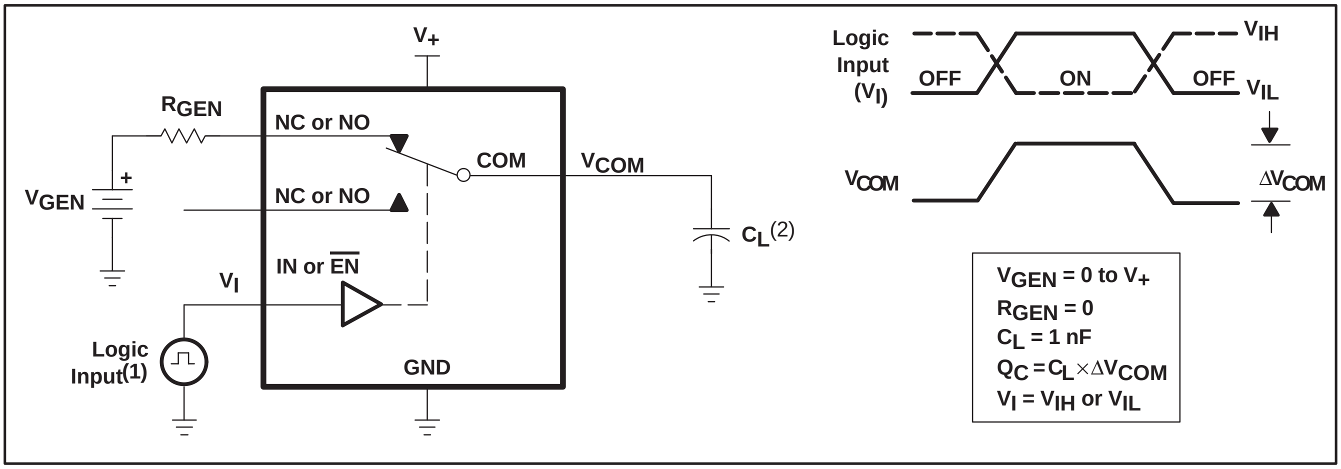
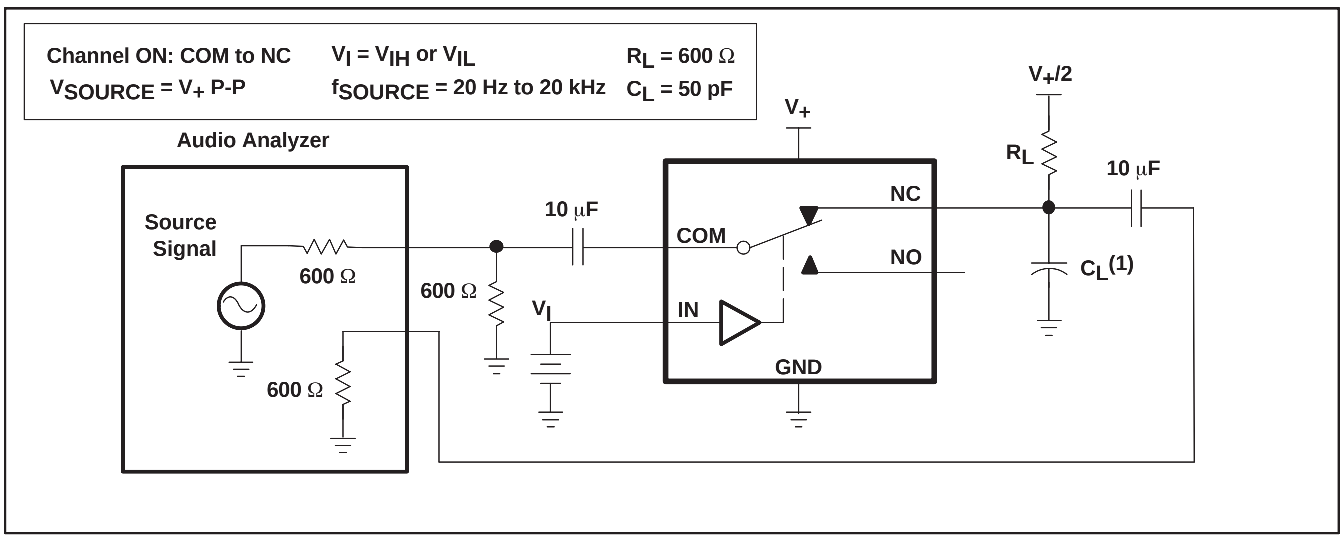


Figure 21. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 22. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS5A3153DCUR	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
TS5A3153DCURE4	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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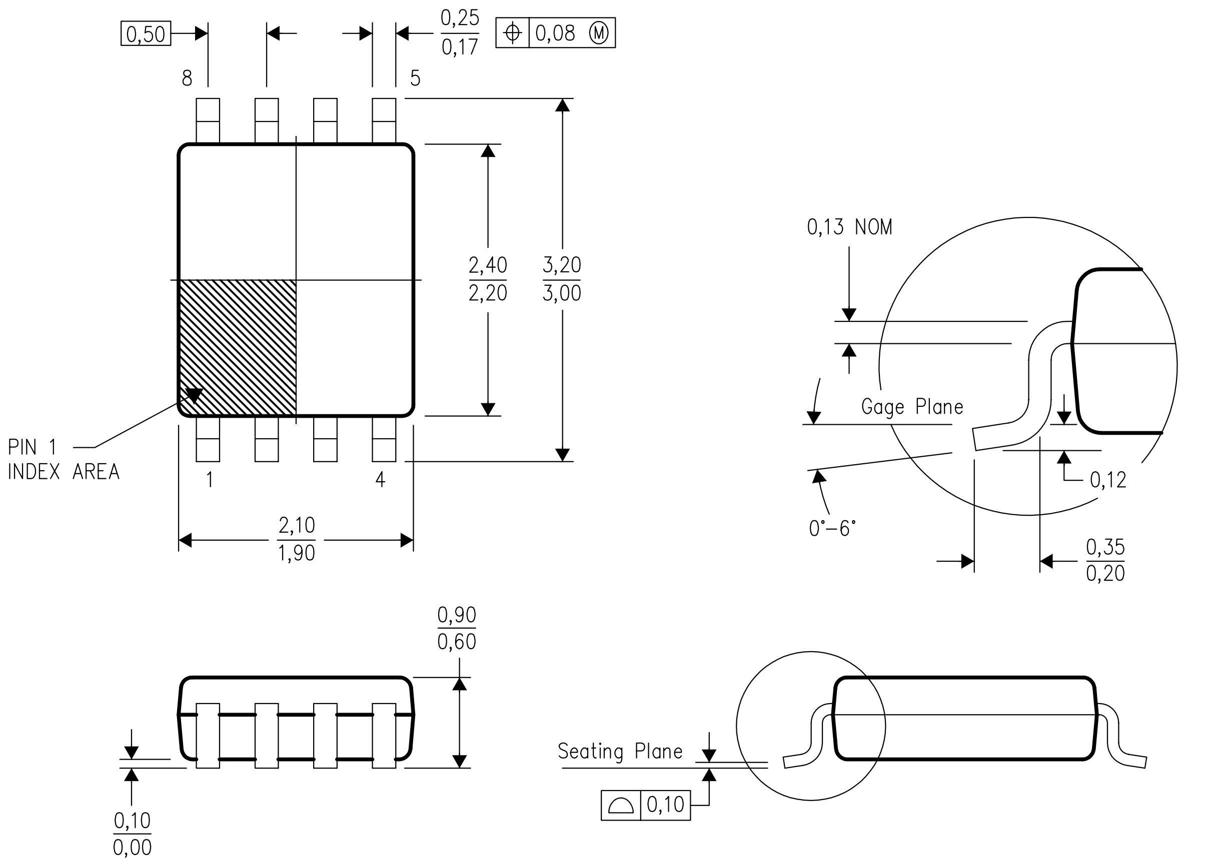
DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

IMPORTANT NOTICE

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