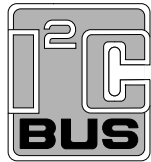


DATA SHEET



TSA5059A 2.7 GHz I²C-bus controlled low phase noise frequency synthesizer

Product specification
Supersedes data of 2000 Sep 19
File under Integrated Circuits, IC02

2000 Oct 24

2.7 GHz I²C-bus controlled low phase noise frequency synthesizer

TSA5059A

FEATURES

- Complete 2.7 GHz single chip system
- Optimized for low phase noise
- Selectable divide-by-two prescaler
- Operation up to 2.3 GHz without divide-by-two prescaler (satellite zero-IF applications) and up to 2.7 GHz with divide-by-two prescaler
- Selectable reference divider ratio
- Selectable crystal or comparison frequency output
- Four selectable charge pump currents
- Four selectable I²C-bus addresses
- Standard and fast mode I²C-bus
- I²C-bus compatible with 3.3 and 5 V microcontrollers
- 5-level Analog-to-Digital Converter (ADC)
- Low power consumption
- Three I/O ports and one output port.

APPLICATIONS

- Satellite zero-IF and non-zero-IF tuning systems
- Digital set-top boxes.

GENERAL DESCRIPTION

The TSA5059A is a single chip PLL frequency synthesizer designed for satellite tuning systems up to 2.7 GHz.

The RF preamplifier drives the 17-bit main divider enabling a step size equal to the comparison frequency, for an input frequency up to 2.3 GHz covering the complete satellite zero-IF frequency range. A fixed divide-by-two additional prescaler can be inserted between the preamplifier and the main divider for a frequency between 2.3 and 2.7 GHz. In this case, the step size is twice the comparison frequency.



The comparison frequency is obtained from an on-chip crystal oscillator that can also be driven from an external source. Either the crystal frequency or the comparison frequency can be switched to the XT/COMP output pin to drive the reference input of another synthesizer or the clock input of a digital demodulation IC.

Both divided and comparison frequency are compared into the fast phase detector which drives the charge pump. The loop amplifier is also on-chip, excepted an external NPN transistor to drive directly the 33 V tuning voltage.

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the main divider ratio, the reference divider ratio, program the four output ports, set the charge pump current, select the prescaler by two, select the signal to switch to the XT/COMP output pin and select a specific test mode. Three of the four output ports can also be used as input ports and a 5-level ADC is provided. Digital information concerning the input ports and the ADC can be read out of the TSA5059A on the SDA line (one status byte) during a READ operation. A flag is set when the loop is 'in-lock' and is read during a READ operation, as well as the Power-on reset flag. The device has four programmable addresses, programmed by applying a specific voltage at pin AS, enabling the use of multiple synthesizers in the same system.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| TSA5059AT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| TSA5059ATS | SSOP16 | plastic shrink small outline package; 16 leads; body width 4.4 mm | SOT369-1 |

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QUICK REFERENCE DATA

$V_{CC} = 4.75$ to 5.25 V; $T_{amb} = -20$ to $+85$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------------|---|------|------|------|------|
| V_{CC} | supply voltage | | 4.75 | 5.0 | 5.25 | V |
| I_{CC} | supply current | $T_{amb} = 25$ °C | 30 | 37 | 45 | mA |
| $f_{i(RF)}$ | RF input frequency | note 1 | 900 | – | 2700 | MHz |
| $V_{i(RF)(rms)}$ | RF input voltage (RMS value) | $f_{i(RF)}$ from 900 to 2200 MHz; note 2 | 7.1 | – | 300 | mV |
| | | | –30 | – | +2.5 | dBm |
| | | $f_{i(RF)}$ from 2.2 to 2.7 GHz; note 2 | 22.4 | – | 300 | mV |
| | | | –20 | – | +2.5 | dBm |
| f_{xtal} | crystal frequency | | 4 | – | 16 | MHz |
| T_{amb} | ambient temperature | | –20 | – | +85 | °C |
| T_{stg} | storage temperature | | –40 | – | +150 | °C |

Notes

1. Bit PE needs to be set to logic 1 for a frequency higher than 2.3 GHz.
2. Asymmetrical drive on pin RFA or RFB; see Fig.3.

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BLOCK DIAGRAM

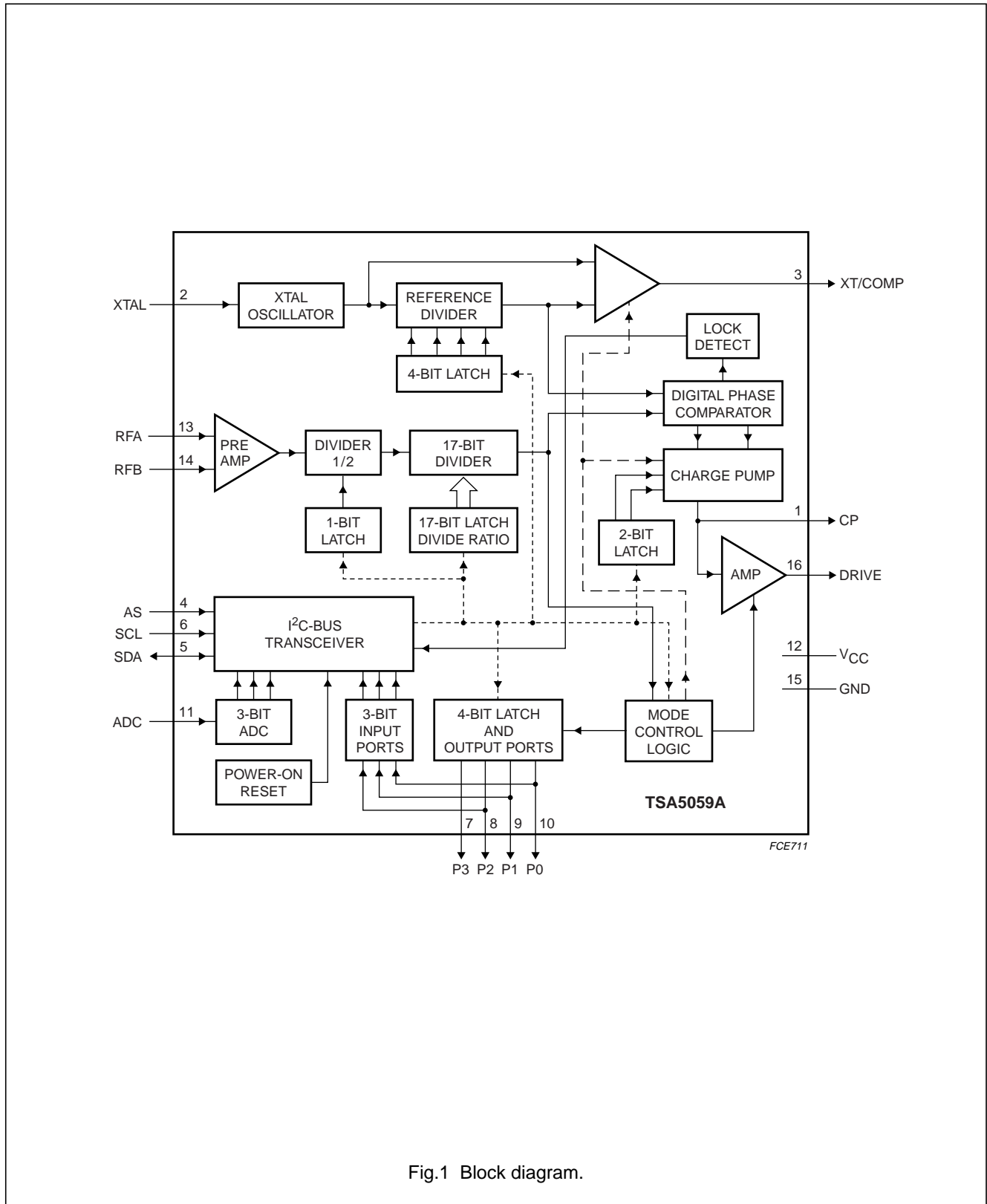


Fig.1 Block diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|-----------------|-----|---|
| CP | 1 | charge pump output |
| XTAL | 2 | crystal oscillator input |
| XT/COMP | 3 | f_{xtal} or f_{comp} signal output |
| AS | 4 | I ² C-bus address selection input |
| SDA | 5 | I ² C-bus serial data input/output |
| SCL | 6 | I ² C-bus serial clock input |
| P3 | 7 | general purpose output Port 3 |
| P2 | 8 | general purpose input/output Port 2 |
| P1 | 9 | general purpose input/output Port 1 |
| P0 | 10 | general purpose input/output Port 0 |
| ADC | 11 | analog-to-digital converter input |
| V _{CC} | 12 | supply voltage |
| RFA | 13 | RF signal input A |
| RFB | 14 | RF signal input B |
| GND | 15 | ground supply |
| DRIVE | 16 | external NPN drive output |

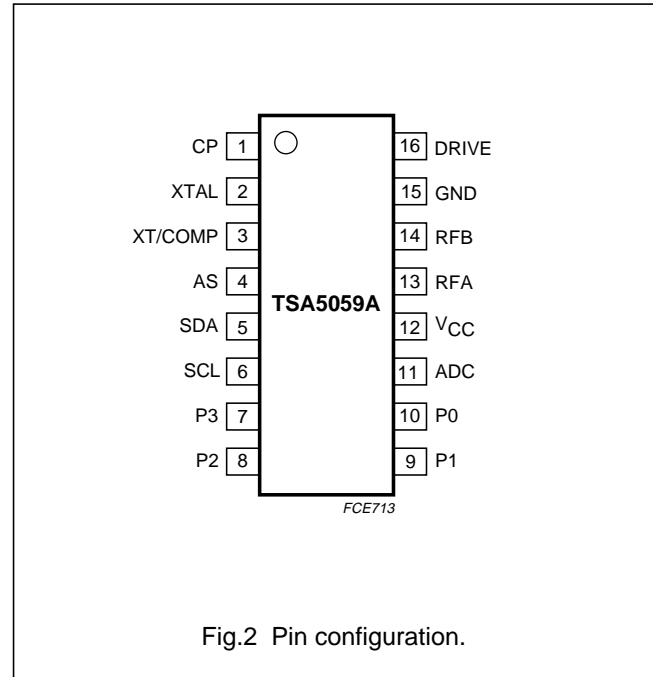


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TSA5059A contains all the necessary elements but a reference source, a loop filter and an external NPN transistor to control a varicap tuned local oscillator forming a phase locked loop frequency synthesized source. The IC is designed in a high speed process with a fast phase detector to allow a high comparison frequency to reach a low phase noise level on the oscillator.

The block diagram is shown in Fig.1. The RF signal is applied at pins RFA and RFB. Thanks to the input preamplifier a good sensitivity is provided. The output of the preamplifier is fed to the 17-bit programmable divider either through a divide-by-two prescaler or directly. Because of the internal high speed process, the RF divider is working for a frequency up to 2.3 GHz, without the need for the divide-by-two prescaler to be used. This prescaler is needed for frequencies above 2.3 GHz.

The output of the 17-bit programmable divider f_{DIV} is fed into the phase comparator, where it is compared in both phase and frequency with the comparison frequency f_{comp} . This frequency is derived from the signal present at pin XTAL, f_{xtal} , divided down in the reference divider. It is possible either to connect a quartz crystal to pin XTAL and then using the on-chip crystal oscillator, or to feed this pin with a reference signal from an external source. The reference divider can have a dividing ratio selected from 16 different values between 2 and 320 (see Table 8).

The output of the phase comparator drives the charge pump and the loop amplifier section. This amplifier requires the use of an external NPN transistor. Pin CP is the output of the charge pump, and pin DRIVE is the pin to connect the base of the external transistor. This transistor has its emitter grounded and the collector drives the tuning voltage to the varicap diode of the Voltage Controlled Oscillator (VCO). The loop filter has to be connected between pin CP and the collector of the external NPN transistor.

In addition, it is possible to drive another PLL synthesizer, or the clock input of a digital demodulation IC, from pin XT/COMP. It is possible to select by software either f_{xtal} , the crystal oscillator frequency or f_{comp} , the frequency present after the reference divider at this pin. It is also possible to switch off this output, in case it is not used.

For test and alignment purposes, it is possible to release the drive output to be able to apply an external voltage on it, to select one of the three charge pump test modes, and to monitor half the f_{DIV} at Port P0. See Table 10 for all possible modes.

Four open-collector output ports are provided on the IC for general purpose; three of these can also be used as input ports. A 3-bit ADC is also available.

The TSA5059A is controlled via the two-wire I²C-bus. For programming, there is one 7-bit module address and bit $\overline{R/\overline{W}}$ for selecting READ or WRITE mode.

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To be able to have more than one synthesizer in an I²C-bus system, one of four possible addresses is selected depending on the voltage applied at pin AS (see Table 3).

The TSA5059A fulfils the fast mode I²C-bus, according to the Philips I²C-bus specification. The I²C-bus interface is designed in such a way that pins SCL and SDA can be connected either to 5 or 3.3 V pulled-up I²C-bus lines, allowing the PLL synthesizer to be connected directly to the bus lines of a 3.3 V microcontroller.

WRITE mode: $\overline{R/W} = 0$

After the address transmission (first byte), data bytes can be sent to the device (see Table 1). Four data bytes are needed to fully program the TSA5059A. The bus transceiver has an auto-increment facility that permits programming of the TSA5059A within one single transmission (address + 4 data bytes).

The TSA5059A can also be partly programmed on the condition that the first data byte following the address is byte 2 or 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether byte 2 (first bit is logic 0) or byte 4 (first bit is logic 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device.

To allow a smooth frequency sweep for fine tuning, and while the data of the dividing ratio of the main divider is in data bytes 2, 3 and 4, it is necessary for changing the frequency to send the data bytes 2 to 5 in a repeated sending, or to finish an incomplete transmission by a STOP condition. Repeated sending of data bytes 2 and 3 without ending the transmission does not change the dividing ratio. To illustrate, the following data sequences will change the dividing ratio:

- Bytes 2, 3, 4 and 5
- Bytes 4, 5, 2 and 3
- Bytes 2, 3, 4 and STOP
- Bytes 4, 5, 2 and STOP
- Bytes 2, 3 and STOP
- Bytes 2 and STOP
- Bytes 4 and STOP.

Table 1 Write data format

| BYTE | DESCRIPTION | MSB | | | | | | | LSB | | CONTROL BIT |
|------|----------------------|-----|-----|-----|-----|-----|-------|-------|-------|---|-------------|
| 1 | address | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 0 | A | |
| 2 | programmable divider | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A | |
| 3 | programmable divider | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A | |
| 4 | control data | 1 | N16 | N15 | PE | R3 | R2 | R1 | R0 | A | |
| 5 | control data | C1 | C0 | XCE | XCS | P3 | P2/T2 | P1/T1 | P0/T0 | A | |

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Table 2 Explanation of Table 1

| BIT | DESCRIPTION |
|---------------|--|
| MA1 and MA0 | programmable address bits; see Table 3 |
| A | acknowledge bit |
| N16 to N0 | programmable main divider ratio control bits; $N = N16 \times 2^{16} + N15 \times 2^{15} + \dots + N1 \times 2^1 + N0$ |
| PE | prescaler enable (prescaler by 2 is active when bit PE = 1) |
| R3 to R0 | programmable reference divider ratio control bits; see Table 8 |
| C1 and C0 | charge pump current select bits; see Table 9 |
| XCE | XT/COMP enable; XT/COMP output active when bit XCE = 1; see Table 10 |
| XCS | XT/COMP select; signal select when bit XCE = 1; test mode enable when bit XCE = 0; see Table 10 |
| T2, T1 and T0 | test mode select when bit XCE = 0 and bit XCS = 1; see Table 10 |
| P3, P2 and P1 | Port P3, P2 and P1 output states |
| P0 | Port P0 output state, except in test mode; see Table 10 |

Address selection

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having up to 4 synthesizers in one system. The relationship between MA1 and MA0 and the input voltage at pin AS is given in Table 3.

Table 3 Address selection

| MA1 | MA0 | VOLTAGE APPLIED TO PIN AS |
|-----|-----|---|
| 0 | 0 | 0 to 0.1V _{CC} |
| 0 | 1 | open-circuit |
| 1 | 0 | 0.4V _{CC} to 0.6V _{CC} ; note 1 |
| 1 | 1 | 0.9V _{CC} to V _{CC} |

Note

1. This address is selected by connecting a 15 kΩ resistor between pin AS and pin V_{CC}.

Status at Power-On Reset (POR)

At power-on or when the supply voltage drops below approximately 2.75 V internal registers are set according to Table 4.

Table 4 Status at Power-on reset; note 1

| BYTE | DESCRIPTION | MSB | | | | | | | LSB | | CONTROL BIT |
|------|----------------------|-----|---|---|---|------------------|------------------|------------------|------------------|------------------|-------------|
| | | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 0 | 0 | |
| 1 | address | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 0 | 0 | A |
| 2 | programmable divider | 0 | X | X | X | X | X | X | X | X | A |
| 3 | programmable divider | X | X | X | X | X | X | X | X | X | A |
| 4 | control data | 1 | X | X | X | X | X | X | X | X | A |
| 5 | control data | 0 | 0 | 0 | 1 | X ⁽²⁾ | 1 ⁽²⁾ | X ⁽²⁾ | X ⁽²⁾ | X ⁽²⁾ | A |

Notes

1. X = don't care.
2. At Power-on reset, all output ports are in high-impedance state.

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READ mode: $R/\overline{W} = 1$

Data can be read out of the TSA5059A by setting bit R/\overline{W} to logic 1 (see Table 5). After the slave address has been recognized, the TSA5059A generates an acknowledge and the first data byte (status word) is transferred on the SDA line. Data is valid on the SDA line during a HIGH-level of the SCL clock signal.

A second data byte can be read out of the TSA5059A if the controller generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the controller occurs. The TSA5059A will then release the data line to allow the controller to generate a STOP condition. When ports P0 to P2 are used as inputs, they must be programmed in their high-impedance state.

The POR flag is set to logic 1 when V_{CC} drops below approximately 2.75 V and at power-on.

It is reset to logic 0 when an end of data is detected by the TSA5059A (end of a READ sequence).

Control of the loop is made possible with the in-lock flag which indicates when the loop is phase-locked (bit FL = 1).

The bits I2, I1 and I0 represent the status of the I/O ports P2, P1 and P0 respectively. A logic 0 indicates a LOW-level and a logic 1 indicates a HIGH-level.

A built-in 5-level ADC is available at pin ADC. This converter can be used to feed AFC information to the microcontroller through the I²C-bus. The relationship between bits A2, A1, A0 and the input voltage at pin ADC is given in Table 7.

Table 5 Read data format

| BYTE | DESCRIPTION | MSB ⁽¹⁾ | | | | | | LSB | | | CONTROL BIT |
|------|-------------|--------------------|----|----|----|----|-----|-----|----|---|-------------|
| 1 | address | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 1 | A | |
| 2 | status byte | POR | FL | I2 | I1 | I0 | A2 | A1 | A0 | – | |

Note

- MSB is transmitted first.

Table 6 Explanation of Table 5

| BIT | DESCRIPTION |
|---------------|--|
| A | acknowledge bit |
| MA1 and MA0 | programmable address bits; see Table 3 |
| POR | Power-on reset flag (bit POR = 1 at power-on) |
| FL | in-lock flag (bit FL = 1 when the loop is phase-locked) |
| I2, I1 and I0 | digital information for I/O ports P2, P1 and P0 respectively |
| A2, A1 and A0 | digital outputs of the 5-level ADC; see Table 7 |

Table 7 ADC levels

| A2 | A1 | A0 | VOLTAGE APPLIED TO PIN ADC ⁽¹⁾ |
|----|----|----|---|
| 1 | 0 | 0 | 0.6V _{CC} to V _{CC} |
| 0 | 1 | 1 | 0.45V _{CC} to 0.6V _{CC} |
| 0 | 1 | 0 | 0.3V _{CC} to 0.45V _{CC} |
| 0 | 0 | 1 | 0.15V _{CC} to 0.3V _{CC} |
| 0 | 0 | 0 | 0 to 0.15V _{CC} |

Note

- Accuracy is $\pm 0.03V_{CC}$.

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Reference divider ratio

The reference divider ratio is set by 4 bits in the WRITE mode, giving 16 different ratios which allow to adjust the comparison frequency to different values, depending on the compromise which has to be found between step size and phase noise.

Table 8 shows the different dividing ratios and the corresponding comparison frequencies and step size, assuming the device is provided with a 4 MHz signal at pin XTAL.

Table 8 Reference dividing ratios

| R3 | R2 | R1 | R0 | RATIO | COMPARISON FREQUENCY ⁽¹⁾ | STEP | |
|----|----|----|----|-------|-------------------------------------|---------------------------|---------------------------|
| | | | | | | BIT PE = 0 ⁽¹⁾ | BIT PE = 1 ⁽¹⁾ |
| 0 | 0 | 0 | 0 | 2 | 2 MHz | 2 MHz | 4 MHz |
| 0 | 0 | 0 | 1 | 4 | 1 MHz | 1 MHz | 2 MHz |
| 0 | 0 | 1 | 0 | 8 | 500 kHz | 500 kHz | 1 MHz |
| 0 | 0 | 1 | 1 | 16 | 250 kHz | 250 kHz | 500 kHz |
| 0 | 1 | 0 | 0 | 32 | 125 kHz | 125 kHz | 250 kHz |
| 0 | 1 | 0 | 1 | 64 | 62.5 kHz | 62.5 kHz | 125 kHz |
| 0 | 1 | 1 | 0 | 128 | 31.25 kHz | 31.25 kHz | 62.5 kHz |
| 0 | 1 | 1 | 1 | 256 | 15.625 kHz | 15.625 kHz | 31.25 kHz |
| 1 | 0 | 0 | 0 | 24 | 166.67 kHz | 166.67 kHz | 333.33 kHz |
| 1 | 0 | 0 | 1 | 5 | 800 kHz | 800 kHz | 1.6 MHz |
| 1 | 0 | 1 | 0 | 10 | 400 kHz | 400 kHz | 800 kHz |
| 1 | 0 | 1 | 1 | 20 | 200 kHz | 200 kHz | 400 kHz |
| 1 | 1 | 0 | 0 | 40 | 100 kHz | 100 kHz | 200 kHz |
| 1 | 1 | 0 | 1 | 80 | 50 kHz | 50 kHz | 100 kHz |
| 1 | 1 | 1 | 0 | 160 | 25 kHz | 25 kHz | 50 kHz |
| 1 | 1 | 1 | 1 | 320 | 12.5 kHz | 12.5 kHz | 25 kHz |

Note

1. Only valid when the IC is used with a 4 MHz crystal.

Charge pump current

The charge pump current can be chosen from 4 different values depending on the value of bits C1 and C0 in the I²C-bus byte 4 according to Table 9.

Table 9 Charge pump current

| C1 | C0 | I _{cp} (μA) (absolute value) | | |
|----|----|---------------------------------------|------|------|
| | | MIN. | TYP. | MAX. |
| 0 | 0 | 100 | 135 | 170 |
| 0 | 1 | 210 | 280 | 350 |
| 1 | 0 | 450 | 600 | 750 |
| 1 | 1 | 920 | 1230 | 1540 |

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XT/COMP frequency output

It is possible to output either the crystal or the comparison frequency at pin XT/COMP to be used in the application. For example, to drive a second PLL synthesizer saving a quartz crystal. To output f_{xtal} it is necessary to set bit XCE to logic 1 and bit XCS to logic 0 or bit XCE to logic 0 and bit XCS to logic 1 during a test mode, while to output f_{comp} it is necessary to set both bits XCE and XCS to logic 1.

If the output signal at this pin is not used it is recommended to disable it by setting both bits XCE and XCS to logic 0. Table 10 shows how this pin is programmed. At power-on the XT/COMP output is set with the f_{xtal} signal selected.

Prescaler enable

The TSA5059A is able to work with the relation $f_{comp} = \text{step size for an input frequency up to 2.3 GHz, covering the complete satellite zero-IF frequency range.}$

For applications with an input frequency higher than 2.3 GHz it is necessary to use the prescaler by 2.

The prescaler is selected by setting bit PE to logic 1 and it is not in use if bit PE is set to logic 0.

For satellite zero-IF applications (frequency between 950 and 2150 MHz), and especially if it is important to reach a low phase noise on the controlled VCO, it is recommended to set bit PE to logic 0 and not to use the prescaler allowing the comparison frequency to be equal to the step size.

Test modes

It is possible to access the test modes by setting bit XCE to logic 0 and bit XCS to logic 1. One specific test mode is then selected using bits T2, T1 and T0 as described in Table 10.

Table 10 XT/COMP and test mode selection; note 1

| XCE | XCS | T2 | T1 | T0 | XT/COMP OUTPUT | TEST MODE |
|-----|-----|----|----|----|----------------|--|
| 0 | 0 | X | X | X | disabled | normal operation |
| 1 | 0 | X | X | X | f_{xtal} | normal operation |
| 1 | 1 | X | X | X | f_{comp} | normal operation |
| 0 | 1 | 0 | 0 | 0 | f_{xtal} | test operation: charge pump sink; status byte bit FL = 1 |
| 0 | 1 | 0 | 0 | 1 | f_{xtal} | test operation: charge pump source; status byte bit FL = 0 |
| 0 | 1 | 0 | 1 | 0 | f_{xtal} | test operation: charge pump disabled; status byte bit FL = 0 |
| 0 | 1 | 0 | 1 | 1 | f_{xtal} | test operation: $\frac{1}{2}f_{DIV}$ switched to Port P0 |
| 0 | 1 | 1 | X | X | f_{xtal} | test operation: drive output (pin DRIVE) is off (low-voltage) to allow the tuning voltage to reach the maximum value; note 2 |

Notes

1. X = don't care.
2. Status at Power-on reset.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------------------|--|------------------|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.3 | +6.0 | V |
| V _n | voltage on pins CP, XTAL, XT/COMP, AS, P0, P1, P2, P3, ADC, RFA and RFB SCL and SDA | | -0.3 | V _{CC} + 0.3 | V |
| I _{O(drive)} | output current on pin DRIVE | | -1 | +1 | mA |
| I _{O(SDA)} | serial data output current | | -1.0 | +10.0 | mA |
| I _{O(Px)} | P0, P1, P2 and P3 output current | port switched on | -1.0 | +20.0 | mA |
| I _{O(ΣPx)} | sum of currents in P0, P1, P2 and P3 | | - | 50.0 | mA |
| T _{amb} | ambient temperature | | -20 | +85 | °C |
| T _{stg} | storage temperature | | -40 | +150 | °C |
| T _{j(max)} | maximum junction temperature | | - | 150 | °C |

Note

- Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|----------------------|---|-------------|-------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | | |
| | TSA5059AT | | 115 | K/W |
| | TSA5059ATS | | 144 | K/W |

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CHARACTERISTICS

$V_{CC} = 4.75$ to 5.25 V; $T_{amb} = -20$ to $+85$ °C; $f_{xtal} = 4$ MHz; measured according to Fig.4; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|------|------|--------|--------|
| Supply (pin V_{CC}) | | | | | | |
| V _{CC} | supply voltage | | 4.75 | 5.0 | 5.25 | V |
| I _{CC} | supply current | T _{amb} = 25 °C | 30 | 37 | 45 | mA |
| V _{CC(POR)} | supply voltage below which POR is active | T _{amb} = 25 °C | – | 2.75 | – | V |
| RF inputs (pins RFA and RFB) | | | | | | |
| f _{i(RF)} | RF input frequency | | 900 | – | 2700 | MHz |
| V _{i(RF)(rms)} | RF input voltage (RMS value) | f _{i(RF)} between 900 and 2200 MHz; note 1 | 7.1 | – | 300 | mV |
| | | | –30 | – | +2.5 | dBm |
| | | f _{i(RF)} between 2.2 and 2.7 GHz; notes 1 and 2 | 22.4 | – | 300 | mV |
| | | | –20 | – | +2.5 | dBm |
| Z _{i(RF)} | RF input impedance | see Fig.6 | – | – | – | Ω |
| C _{i(RF)} | RF input capacitance | see Fig.6 | – | – | – | pF |
| MDR | main divider ratio | prescaler disabled | 64 | – | 131071 | |
| | | prescaler enabled | 128 | – | 262142 | |
| Crystal oscillator (pin XTAL) | | | | | | |
| f _{xtal} | crystal frequency | | 4 | – | 16 | MHz |
| Z _{XTAL} | crystal oscillator negative impedance | 4 MHz crystal | 400 | 680 | – | Ω |
| Z _{XTAL} | recommended crystal series resistance | 4 MHz crystal | – | – | 200 | Ω |
| P _{XTAL} | crystal drive level | 4 MHz crystal; note 3 | – | 40 | – | μW |
| f _{i(ext)} | external reference input frequency | note 4 | 2 | – | 20 | MHz |
| V _{i(ext)(p-p)} | external reference input voltage (peak-to-peak value) | note 4 | 200 | – | 500 | mV |
| Phase comparator and charge pump | | | | | | |
| f _{comp} | comparison frequency | | – | – | 2 | MHz |
| N _{comp} | equivalent phase noise at the phase detector input | f _{comp} = 250 kHz; C1 = C0 = 1; in the loop bandwidth | – | –157 | – | dBc/Hz |
| I _{cp} | charge pump current | C1 = 0; C0 = 0 | 100 | 135 | 170 | μA |
| | | C1 = 0; C0 = 1 | 210 | 280 | 350 | μA |
| | | C1 = 1; C0 = 0 | 450 | 600 | 750 | μA |
| | | C1 = 1; C0 = 1 | 920 | 1230 | 1540 | μA |
| I _{LO(cp)} | charge pump output leakage current | | –10 | 0 | +10 | nA |
| DRIVE output (pin DRIVE) | | | | | | |
| V _{O(drive)} | output voltage when the charge pump is sinking current | XCE = 0; XCS = 1; T2 = 0; T1 = 0; T0 = 0 | – | 140 | 250 | mV |
| I _{O(drive)} | output current when the charge pump is sourcing current | XCE = 0; XCS = 1; T2 = 0; T1 = 0; T0 = 1 | 100 | 250 | – | μA |

2.7 GHz I²C-bus controlled low phase noise frequency synthesizer

TSA5059A

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---|-------------|-------------|----------|----------|
| XT/COMP output (pin XT/COMP) | | | | | | |
| V _{O(p-p)} | AC output voltage (peak-to-peak value) | XCE = 1 | – | 400 | – | mV |
| Input/output and output ports (pins P0, P1, P2 and P3) | | | | | | |
| I _{IO} | port leakage current | port off; V _O = V _{CC} | – | – | 10 | μA |
| V _{O(sat)} | output port saturation voltage | port on; I _{sink} = 10 mA | – | 0.2 | 0.4 | V |
| V _{IL} | LOW-level input voltage | | – | – | 1.5 | V |
| V _{IH} | HIGH-level input voltage | | 3.0 | – | – | V |
| ADC input (pin ADC) | | | | | | |
| I _{LIH} | HIGH-level input leakage current | V _{ADC} = V _{CC} | – | – | 10 | μA |
| I _{LIL} | LOW-level input leakage current | V _{ADC} = 0 V | –10 | – | – | μA |
| Address selection (pin AS) | | | | | | |
| I _{LIH} | HIGH-level input leakage current | V _{AS} = V _{CC} | – | – | 1 | mA |
| I _{LIL} | LOW-level input leakage current | V _{AS} = 0 V | –0.5 | – | – | mA |
| SCL and SDA inputs (pins SCL and SDA) | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.5 | V |
| V _{IH} | HIGH-level input voltage | | 2.3 | – | – | V |
| I _{LIH} | HIGH-level input leakage current | V _{IH} = 5.5 V V _{CC} = 5.5 V V _{CC} = 0 V | – – – | – – – | 10 10 | μA μA |
| I _{LIL} | LOW-level input leakage current | V _{IL} = 0 V; V _{CC} = 5.5 V | –10 | – | – | μA |
| f _{SCL} | SCL clock frequency | | – | – | 400 | kHz |
| SDA output (pin SDA) | | | | | | |
| V _{O(ack)} | output voltage during acknowledge | I _{sink} = 3 mA | – | – | 0.4 | V |

Notes

- Asymmetrical drive on pin RFA or RFB; see Fig.3.
- Bit PE needs to be set to logic 1 for a frequency higher than 2.3 GHz.
- The drive level is expected with the crystal at series resonance with a series resistance of 50 Ω. The value will be different with another crystal.
- To drive pin XTAL from the pin XT/COMP of another TSA5059A, couple the signal using a capacitor of 1 nF (to remove the DC level) in series with an 1.2 kΩ resistor (see Fig.5).

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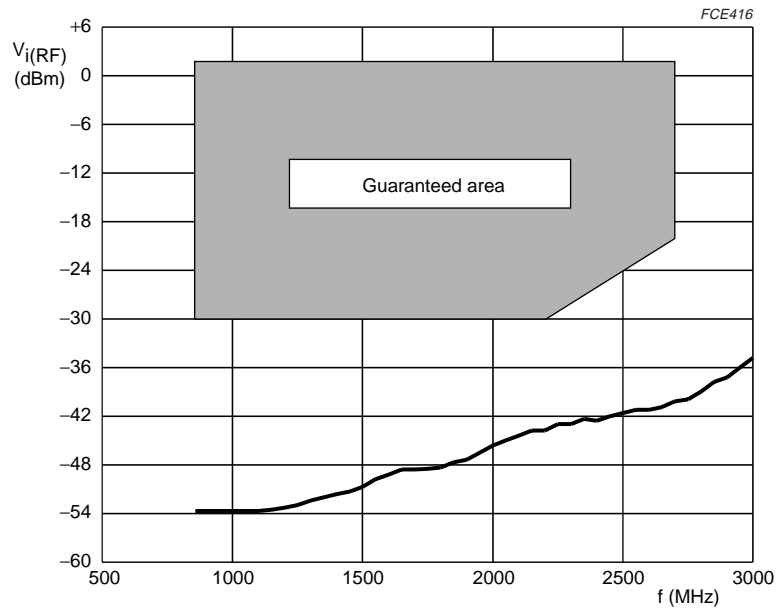


Fig.3 Sensitivity curve.

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APPLICATION INFORMATION

An example of a typical application is given in Fig.4. In this application the VCO centre frequency is 1.5 GHz with a slope of 100 MHz/V. The expected loop bandwidth is 10 kHz with a charge pump current of 555 μ A and f_{comp} of 250 kHz. Filter components need to be adapted to each application depending on the VCO characteristics and the required performance of the loop.

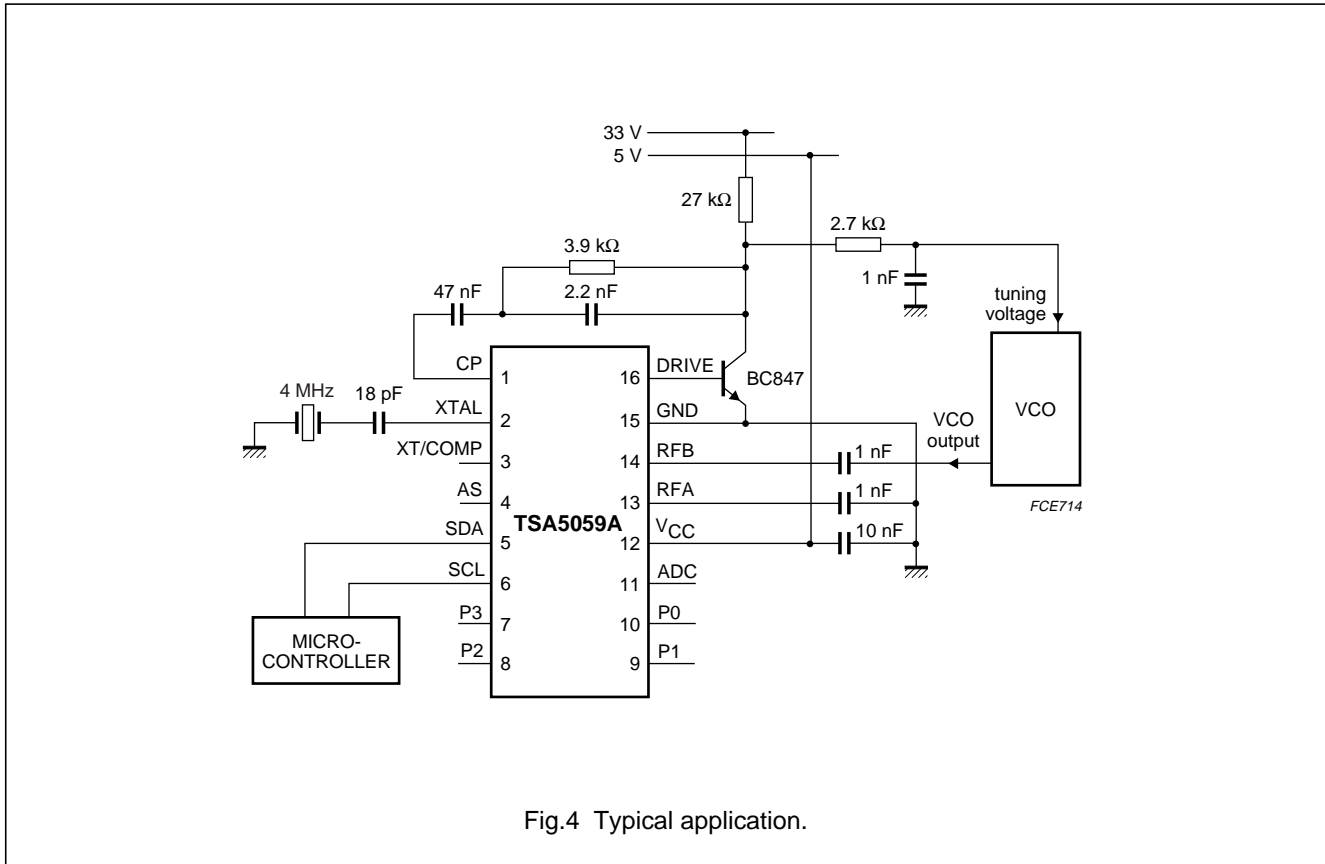


Fig.4 Typical application.

Loop bandwidth

Most of the applications the TSA5059A are dedicated for require a large loop bandwidth, in the order of a few kHz to a few tens of kHz. The calculation of the loop filter elements has to be done for each application, while it depends on the VCO slope and phase noise as well as the reference frequency and charge pump current.

A simulation of the loop can easily be done by using the SIMPATA software from Philips.

Reference source

The TSA5059A is well suited to be used with a 4 MHz crystal connected to pin XTAL. Philips crystal ordering code 4322 143 04093 is recommended in this case.

It is however possible to use a crystal with an higher frequency (up to 16 MHz) to improve the noise performance. When choosing a crystal, one should take notice to select a crystal able to withstand the drive level of the TSA5059A without suffering from accelerated ageing.

It is also possible to feed pin XTAL with an external signal between 2 and 20 MHz, coming from an external oscillator or from the pin XT/COMP of another TSA5059A, when more than one synthesizer is present in the same application. Then the application given in Fig.5 should be used.

If the signal at pin XT/COMP is not used in an application the output should be switched off (XCE = 0 and XCS = 0). This pin should then be left open.

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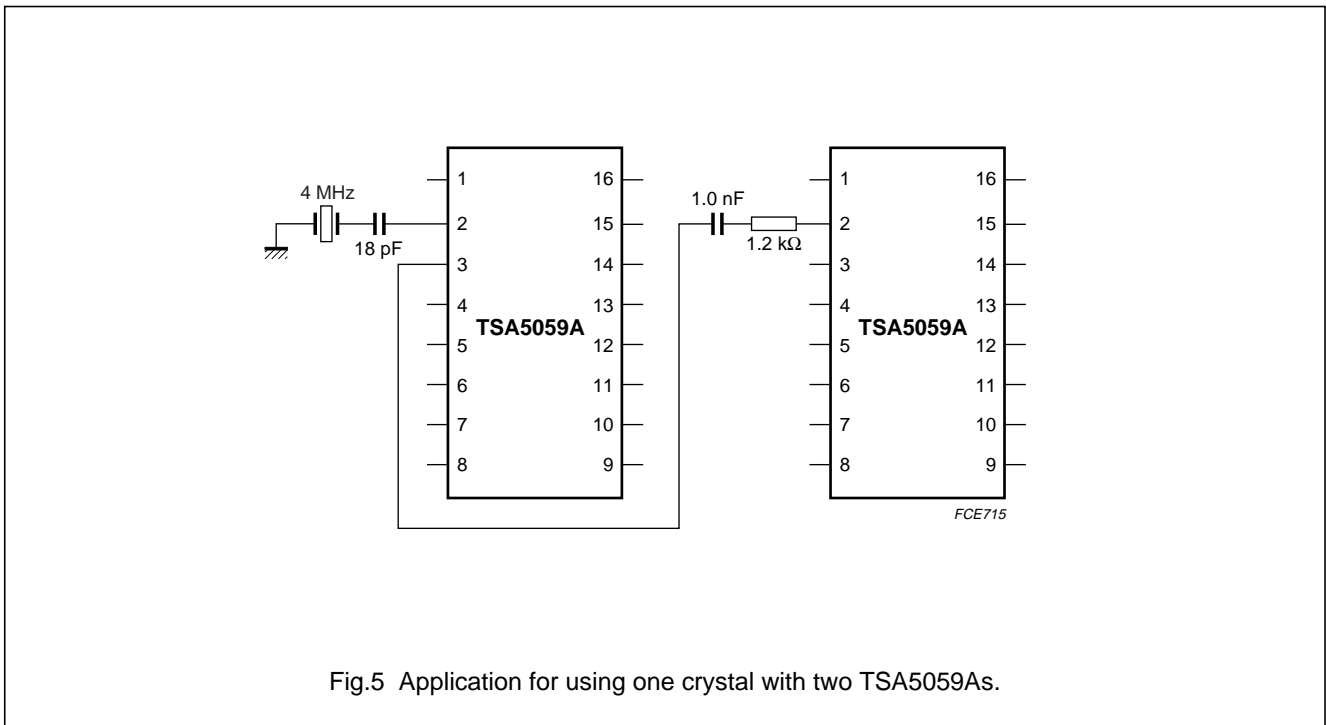


Fig.5 Application for using one crystal with two TSA5059As.

I²C-bus crosstalk

The TSA5059A includes a loop amplifier that requires an external NPN transistor. Care should be taken in the layout of the application to ground the emitter of the NPN transistor as close as possible to the ground of the VCO.

The best way to avoid any I²C-bus crosstalk in the application (i.e. parasitic coupling between the I²C-bus lines and the VCO coil) is to avoid the I²C-bus signal to come in the RF part by using an I²C-bus gate that allows only the messages for the PLL to go to the PLL and to avoid unnecessary repeated sending. Such a gate is integrated in most of the Philips digital demodulators.

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RF input impedance

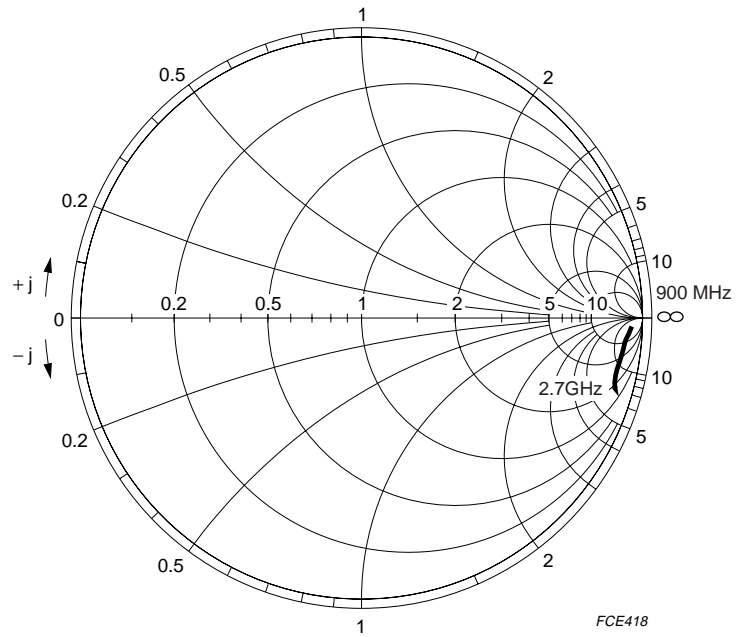


Fig.6 RF input impedance.

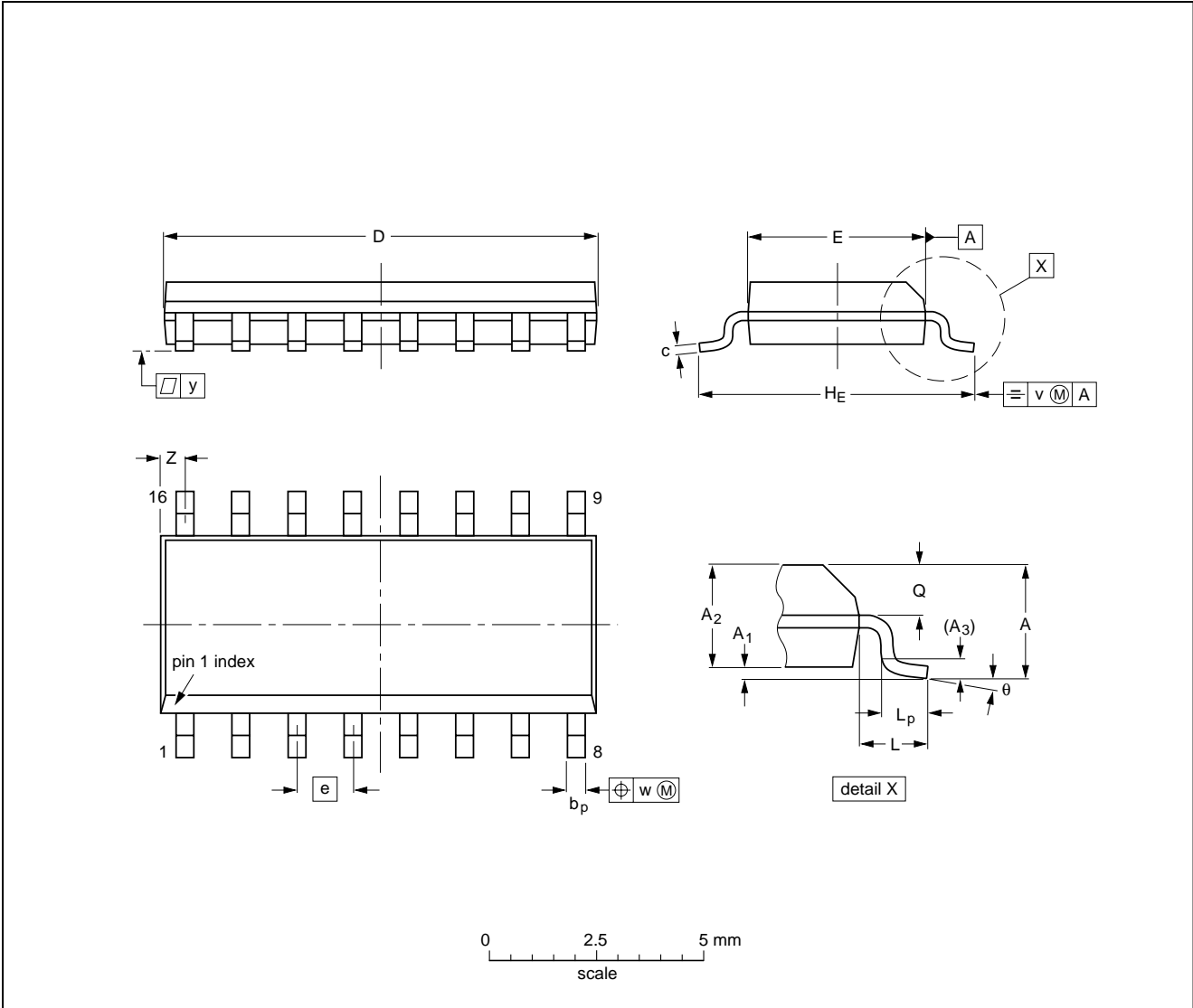
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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.050 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

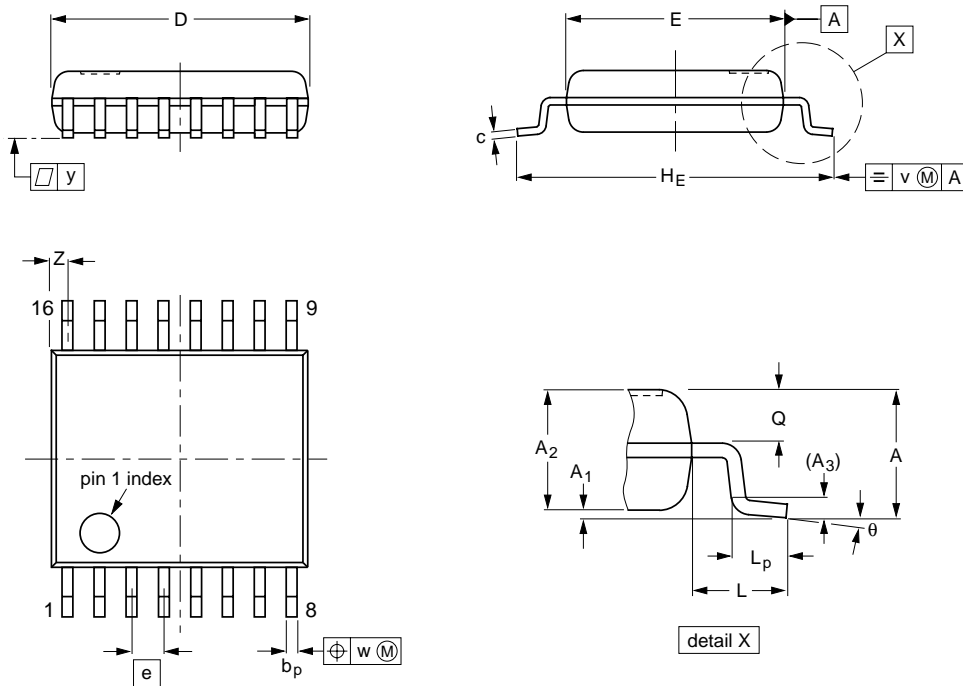
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|---------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT109-1 | 076E07 | MS-012 | | | 97-05-22- 99-12-27 |

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SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm

SOT369-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|-----|----------------|--------------|-----|------|-----|------------------|-----------|
| mm | 1.5 | 0.15 0.00 | 1.4 1.2 | 0.25 | 0.32 0.20 | 0.25 0.13 | 5.30 5.10 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.45 | 0.65 0.45 | 0.2 | 0.13 | 0.1 | 0.48 0.18 | 10° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT369-1 | | MO-152 | | | | 95-02-04 99-12-27 |

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TSA5059A

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|--|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

| DATA SHEET STATUS | PRODUCT STATUS | DEFINITIONS ⁽¹⁾ |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOME BUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

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The Netherlands, Fax. +31 40 27 24825

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