- **Fully Supports Provisions of IEEE 1394–1995 Standard for High Performance Serial Bus† and the P1394a Supplement (Draft 2.0)**
- **Full P1394a Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed concatenation, Arbitration Acceleration, Fly-by Concatenation, Port Disable/Suspend/Resume**
- **Provides Six P1394a Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Power-Down Features to Conserve Energy in Battery Powered Applications include: Automatic Device Power-Down during Suspend, Device Power-Down Pin, Link Interface Disable via LPS, and Inactive Ports Powered Down**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Single 3.3 V Supply Operation**
- **Interface to Link Layer Controller Supports Low Cost TI™ Bus-Holder Isolation and Optional Annex J Electrical Isolation**
- **Data Interface to Link-Layer Controller Through 2/4/8 Parallel Lines at 49.152 MHz**
- **Low Cost 24.576-MHz Crystal Provides Transmit, Receive Data at 100/200/400 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz**
- **Interoperable with Link-Layer Controllers Using 3.3-V and 5-V Supplies**
- **Interoperable with Other Physical Layers (PHY) Using 3.3-V and 5-V Supplies**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias (TPBIAS) for Each Port**
- **Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Bit and P1394a Features**
- **Fully Interoperable with FIreWire™ and i.LINK™ Implementation of IEEE Std 1394**
- **Low Cost, High Performance 100 Pin TQFP (PZP) Thermally Enhanced Package**

description

The TSB41LV06 provides the digital and analog transceiver functions needed to implement a six-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41LV06 is designed to interface with a Link Layer Controller (LLC), such as the TSB12LV22, TSB12LV21, TSB12LV31, TSB12LV41, or TSB12LV01.

The TSB41LV06 requires only an external 24.576 MHz crystal as a reference. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152 MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

†Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.
i.LINK is a trademark of Sony Corporation
FireWire is a trademark of Apple Computers Incorporated.

description (continued)

The TSB41LV06 supports an optional isolation barrier between itself and its LLC. When the $\overline{\text{ISO}}$ input terminal is tied high, the LLC interface outputs behave normally. When the $\overline{\text{ISO}}$ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in IEEE 1394a section 5.9.4. To operate with TI Bus Holder isolation the $\overline{\text{ISO}}$ on the PHY terminal must be tied HIGH.

Data bits to be transmitted through the cable ports are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed) and are latched internally in the TSB41LV06 in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 392.216 Mbits/s (referred to as S100, S200, and S400 speed, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two, four or eight bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB41LV06 provides a 1.86 V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB41LV06 operate in a high-impedance current mode, and are designed to work with external 110 Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.3-kΩ ±0.5%. This may be accomplished by placing a 6.34-kΩ ±0.5% resistor in parallel with a 1-MΩ resistor.

When the power supply of the TSB41LV06 is 0 V while the twisted-pair cables are connected, the TSB41LV06 transmitter and receiver circuitry will present a high impedance to the cable and will not load the TPBIAS voltage at the other end of the cable.

When the TSB41LV06 is used with one or more of the ports not brought out to a connector, the twisted–pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals should be tied together and then pulled to ground, or the TPB+ and TPB– terminals should be connected to the suggested termination network. The TPA+ and TPA– and TPBIAS terminals of an unused port may be left unconnected. The TPBias terminal should be connected to a 1-μF capacitor to ground or left floating.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to V_{DD}, SE should be tied to ground through a 1-kΩ resistor, while SM should be connected directly to ground.

Four package terminals are used as inputs to set the default value for four configuration status bits in the self–ID packet, and are hardwired high or low as a function of the equipment design. The PC0–PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 9 for power-class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for either isochronous resource manager (IRM) or bus manager (BM).

The PHY supports suspend/resume as defined in the IEEE P1394a specification. The suspend mechanism allows pairs of directly–connected ports to be placed into a low power conservation state while maintaining a port–to–port connection between 1394 bus segments. While in a low–power state, a port is unable to transmit or receive data transaction packets. However, a port in a low power state is capable of detecting connection status changes and detecting incoming TPBias. When all six ports of the TSB41LV06 are suspended all circuits except the bandgap reference generator and bias detection circuits are powered down resulting in significant power savings. For additional details of suspend/resume operation refer to the P1394a specification. The use of suspend/resume is recommended for new designs.

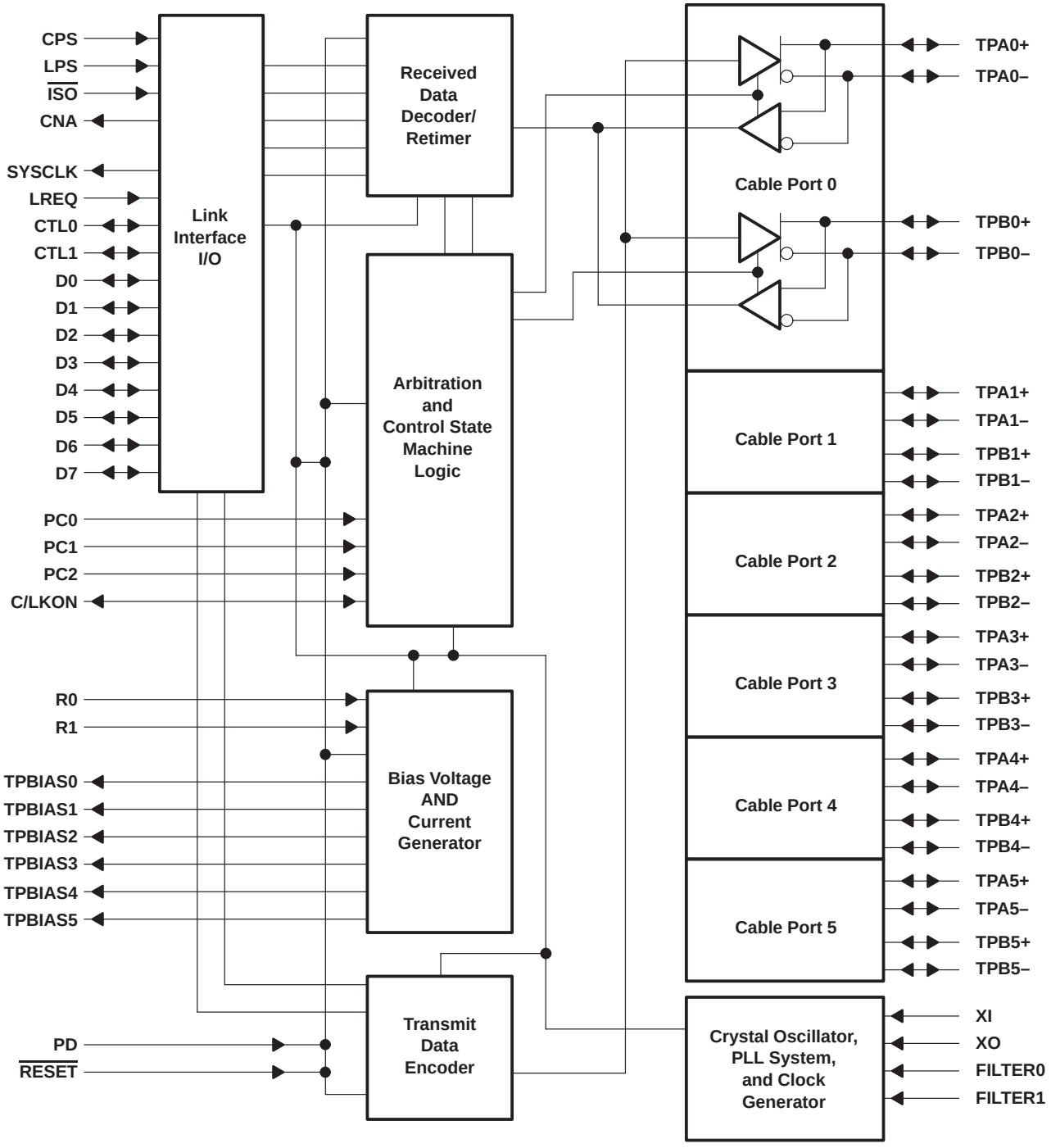
The port transmitter and receiver circuitry is disabled during power-down (when the PD input terminal is asserted high), during reset (when the $\overline{\text{RESET}}$ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The TPBIAS is disabled during power–down, during reset, or when the port is disabled as commanded by the LLC.

The CNA (cable-not-active) terminal provides a high output when all twisted-pair cable ports are disconnected, and can be used along with LPS to determine when to power–down the TSB41LV06. The CNA output is not debounced. In a PD terminal initiated power down, the CNA detection circuitry remains enabled.

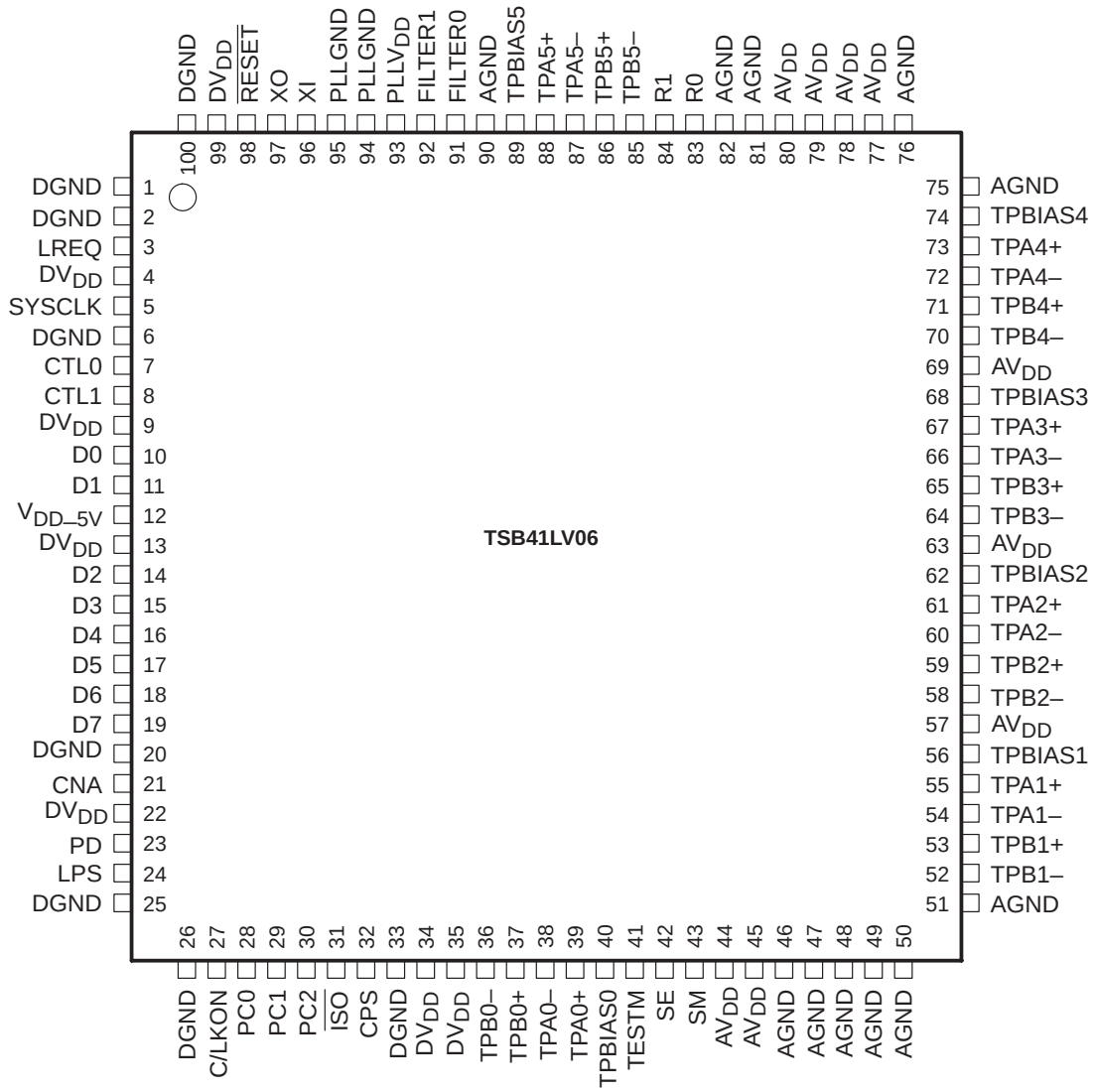
The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC indicates to the PHY that the LLC is powered up and active. During LLC power-down mode, as indicated by the LPS input being low for more than 2.6 μs, the TSB41LV06 deactivates the PHY-LLC interface to save power. The TSB41LV06 will continue the necessary repeater function required for network operation during this low power state.

If the PHY receives a link-on packet from another node, the C/LKON terminal is activated to output a square-wave signal. The LLC recognizes this signal, reactivates any powered-down portions of the LLC, and notifies the PHY of its power-on status via the LPS terminal. The PHY confirms notification by deactivating the square-wave signal on the C/LKON terminal, and then enables the PHY-link interface.

functional block diagram



PZP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	NO.			
AGND	46, 47, 48, 49, 50, 51, 75, 76, 81, 82, 90	Supply	–	Analog circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
AV_{DD}	44, 45, 57, 63, 69, 77, 78, 79, 80	Supply	–	Analog circuit power pins. A combination of high frequency decoupling capacitors near each pin are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from $PLLV_{DD}$ and DV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
C/LKON	27	CMOS	I/O	Bus manager contender programming input and link-on output. On hardware reset, this pin is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the pin through a 10 kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input. Following hardware reset, this pin is the link-on output, which is used to notify the LLC to power-up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (8 SYSCLK cycles) when active. The link-on output is deasserted low when the LPS input pin is active.
CNA	21	CMOS	O	Cable not active output. This pin is asserted high when there are no ports receiving incoming bias voltage.
CPS	32	CMOS	I	Cable power status input. This pin is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power.
CTL0 CTL1	7 8	CMOS 5 V tol	I/O	Control I/Os. These bidirectional signals control communication between the TSB41LV06 and the LLC. Bus holders are built into these terminals.
D0 – D7	10, 11, 14, 15, 16, 17, 18, 19	CMOS 5 V tol	I/O	Data I/O's. These are bidirectional data signals between the TSB41LV06 and the LLC. Bus Holders are built into these terminals.
DGND	1, 2, 6, 20, 25, 26, 33, 100	Supply	–	Digital circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
DV_{DD}	4, 9, 13, 22, 34, 35, 99	Supply	–	Digital circuit power pins. A combination of high frequency decoupling capacitors near each pin are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from $PLLV_{DD}$ and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
FILTER0 FILTER1	91 92	CMOS	I/O	PLL filter pins. These pins are connected to an external capacitance to form a lag-lead filter required for stable operation of the internal frequency multiplier PLL running off of the crystal oscillator. A 0.1 μF ±10% capacitor is the only external component required to complete this filter.
$\overline{ISO}$	31	CMOS	I	Link interface isolation control input. This pin controls the operation of output differentiation logic on the CTL and D pins. If an optional isolation barrier of the type described in Annex J of IEEE Std 1394-1995 is implemented between the TSB41LV06 and LLC, the $\overline{ISO}$ pin should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or TI bus holder Isolation is implemented, the $\overline{ISO}$ pin should be tied high to disable the differentiation logic. For additional information refer to TI application note *Serial Bus Galvanic Isolation*, SLLA011.

Terminal Functions (Continued)

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	NO.			
LPS	24	CMOS 5 V tol	I	Link power status input. This pin is used to monitor the power status of the LLC, and is connected to either the V_{DD} supplying the link layer controller through a 1 kΩ resistor, or to a pulsed output which is active when the LLC is powered. The pulsed output is useful when using an isolation barrier. If this input is low for more than 2.6 μs, the LLC is considered powered-down. If this input is high for more than 20 ns, the LLC is considered powered-up. If the LLC is powered-down, the PHY-LLC interface is disabled, and the TSB41LV06 will perform only the basic repeater functions required for network initialization and operation. Bus holder is built into this terminal.
LREQ	3	CMOS 5 V tol	I	LLC request input. The LLC uses this input to initiate a service request to the TSB41LV06. Bus Holder is built into this terminal.
PC0 PC1 PC2	28 29 30	CMOS	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power–class indicated during self-ID. Programmed is done by tying the pins high or low. Refer to Table 9 for encoding.
PD	23	CMOS 5 V tol	I	Power-down input. A high on this pin turns off all internal circuitry except the cable-active monitor circuits, which control the CNA output. Bus Holder is built into this terminal.
PLLGND	94, 95	Supply	–	PLL circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
$PLLV_{DD}$	93	Supply	–	PLL circuit power pins. A combination of high frequency decoupling capacitors near each pin are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from DV_{DD} and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
$\overline{\text{RESET}}$	98	CMOS	I	Logic reset input. Asserting this pin low resets the internal logic. An internal pull–up resistor to V_{DD} is provided so only an external delay capacitor in parallel with a resistor is required for proper power-up operation (see *power–up reset* in the *applications information section*). This input is otherwise a standard logic input, and may also be driven by an open-drain type driver.
R0 R1	83 84	Bias	–	Current setting resistor pins. These pins are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.30 kΩ ±0.5% is required to meet the IEEE Std 1394-1995 output voltage limits.
SE	42	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41LV06. For normal use this pin should be tied to GND through a 1-kΩ resistor.
SM	43	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41LV06. For normal use this pin should be tied to GND.
SYSCLK	5	CMOS	O	System clock output. Provides a 49.152 MHz clock signal, synchronized with data transfers, to the LLC.
TESTM	41	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41LV06. For normal use this pin should be tied to V_{DD}.
TPA0+ TPA1+ TPA2+ TPA3+ TPA4+ TPA5+	39 55 61 67 73 88	Cable	I/O	Twisted-pair cable A differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.

Terminal Functions (Continued)

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	NO.			
TPA0– TPA1– TPA2– TPA3– TPA4– TPA5–	38 54 60 66 72 87	Cable	I/O	Twisted-pair cable A differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB0+ TPB1+ TPB2+ TPB3+ TPB4+ TPB5+	37 53 59 65 71 86	Cable	I/O	Twisted-pair cable B differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB0– TPB1– TPB2– TPB3– TPB4– TPB5–	36 52 58 64 70 85	Cable	I/O	Twisted-pair cable B differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPBIAS0 TPBIAS1 TPBIAS2 TPBIAS3 TPBIAS4 TPBIAS5	40 56 62 68 74 89	Cable	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted–pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection. Each of these pins must be decoupled with a 1.0 μF capacitor to ground.
V_{DD_5V}	12	Supply	–	5–V V_{DD} pin. This pin should be connected to the LLC V_{DD} supply when a 5–V LLC is used, and should be connected to the PHY DV_{DD} when a 3–V LLC is used. A combination of high frequency decoupling capacitors near this pin is suggested, such as paralleled 0.1 μF and 0.001 μF. When this pin is tied to a 5–V supply, all pin Bus Holders are disabled, regardless of the state of the $\overline{ISO}$ pin. When this pin is tied to a 3–V supply, Bus Holders are enabled when the $\overline{ISO}$ pin is high.
XI XO	96 97	Crystal	–	Crystal oscillator inputs. These pins connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used *(see crystal selection in the applications information section).*

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
5V tolerant I/O supply voltage range, V_{DD_5V} . . . . . –0.3 V to 5.5 V
5V tolerant input voltage range, V_{I_5V} . . . . . –0.5 V to V_{DD_5V} + 0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{DD} + 0.5V
Electrostatic discharge (see Note 2) . . . . . HBM: 2 kV, MM: 200 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature,T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground.
2. HBM is Human Body Model, MM is Machine Model.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PZP‡	4.48 W	56.02 mW/°C	1.96 W
PZP§	2.28 W	35.44 mW/°C	0.685 W

† This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
‡ 1 oz. trace and copper pad with solder.
§ 1 oz. trace and copper pad without solder.
NOTE: For more information, refer to TI application note *PowerPAD Thermally Enhanced Package* TI literature number SLMA002.

recommended operating conditions

PARAMETER		MIN	TYP†	MAX	UNIT
Supply voltage, V_{DD}	Source power node	3	3.3	3.6	V
	Nonsource power node	2.7‡	3	3.6	
High-level input voltage, V_{IH}	Case 1 (Bus Holder): $\overline{ISO}$=V_{DD}, V_{DD_5V} = V_{DD} Case 2 (5V Tol): $\overline{ISO}$=V_{DD}, V_{DD_5V} = 5V LPS, PD, LREQ, CTL0, CTL1, D0–D7	2.6			V
	C/LKON, PC0, PC1, PC2, $\overline{ISO}$	0.7×V_{DD}			V
	$\overline{RESET}$	0.6×V_{DD}			V
Low-level input voltage, V_{IL}	Case 1 (Bus Holder): $\overline{ISO}$=V_{DD}, V_{DD_5V} = V_{DD} Case 2 (5V Tol): $\overline{ISO}$=V_{DD}, V_{DD_5V} = 5 V LPS, PD, LREQ, CTL0, CTL1, D0–D7			1.2	V
	C/LKON, PC0, PC1, PC2, $\overline{ISO}$			0.2×V_{DD}	V
	$\overline{RESET}$			0.3×V_{DD}	V
Output current, I_O	TPBIAS outputs	–5.6		1.3	mA
Maximum junction temperature T_J (see $R_{\theta JA}$ values listed in thermal characteristics table)	$R_{\theta JA}$= 17.85°C/W, T_A=70°C			99	°C
	$R_{\theta JA}$ =28.22°C/W, T_A=70°C			116	
Differential input voltage, V_{ID}	Cable inputs, during data reception	118		260	mV
	Cable inputs, during arbitration	168		265	
Common-mode input voltage, V_{IC}	TPB cable inputs, Source power node	0.4706		2.515	V
	TPB cable inputs, Nonsource power node	0.4706		2.015‡	
Power-up reset time, t_{pu}	$\overline{RESET}$ input	2			ms
Receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
	TPA, TPB cable inputs, S200 operation			±0.5	
	TPA, TPB cable inputs, S400 operation			±0.315	
Receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
	Between TPA and TPB cable inputs, S200 operation			±0.55	
	Between TPA and TPB cable inputs, S400 operation			±0.5	

† All typical values are at V_{DD} = 3.3 V and T_A = 25°C.
‡ For a node that does not source power, see Section 4.2.2.2 in IEEE 1394a.

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω load, See Figure 1	172		265	mV
I_{DIFF}	Driver difference current, TPA+, TPA–, TPB+, TPB–	Driver enabled, speed signaling off	–1.05†		1.05†	mA
I_{SP}	Common mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled	–4.84‡		–2.53‡	mA
I_{SP}	Common mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled	–12.4‡		–8.10‡	mA
V_{OFF}	Off state differential voltage	Drivers disabled, See Figure 1			20	mV

† Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
‡ Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

receiver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Driver disabled	10	14		kΩ
					4	pF
Z_{IC}	Common mode impedance	Driver disabled	20			kΩ
					24	pF
$V_{TH–R}$	Receiver input threshold voltage	Drivers disabled	–30		30	mV
$V_{TH–CB}$	Cable bias detect threshold, TPBx cable inputs	Driver disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Driver disabled	89		168	mV
$V_{TH–}$	Negative arbitration comparator threshold voltage	Driver disabled	–168		–89	mV
$V_{TH–SP200}$	Speed signal threshold	TPBIAS-TPA common mode voltage, drivers disabled	49		131	mV
$V_{TH–SP400}$			314		396	

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (continued)

device

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	See Note 3		273		mA
		See Note 4		166		
$I_{CC–PD}$	Supply current – sleep power mode	V_{CC} = 3.3 V, T_A = 25°C		7		mA
V_{TH}	Power status threshold, CPS input†	400 KΩ resistor†	4.7		7.5	V
V_{OH}	High-level output voltage	V_{DD} = 2.7 V, I_{OH} = –4 mA	2.2			V
		V_{DD} = 3 V to 3.6 V, I_{OH} = –4 mA	2.8			
		Annex J; I_{OH} = –9 mA, $\overline{ISO}$ = 0 V, V_{DD_5V} = V_{DD}	V_{DD}–0.4			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
		Annex J; I_{OH} = 9 mA, $\overline{ISO}$ = 0 V, V_{DD_5V} = V_{DD}			0.4	
I_{BH+}	Positive peak bus holder current (D0 – D7, CTL0, CTL1, LREQ, LPS, PD)	ISO = 3.6 V, V_{DD} = 3.6 V, V_I = 0 V to V_{DD}, V_{DD_5V} = V_{DD}	0.05		1	mA
$I_{BH–}$	Negative peak bus holder current (D0 – D7, CTL0, CTL1, LREQ, LPS, PD)		–1		–0.05	
I_I	Input current, LREQ, LPS, PD, TESTM, SE, SM, PC0–PC2 inputs	$\overline{ISO}$ = 0 V, V_{DD} 3.6 V			5	µA
I_{OZ}	Off-state output current, CTL0, CTL1, D0–D7, C/LKON I/Os	V_O= V_{DD} or 0 V			±5	µA
I_{IRST}	Pullup current, RESET input	V_I = 1.5 V	–80	–40	–20	µA
		V_I = 0 V	–90	–45	–22	
V_{IT+}	Positive input threshold voltage, LREQ, CTL0, CTL1, D0–D7 inputs‡	$\overline{ISO}$ = 0 V ,V_{DD_5V} = V_{DD}	V_{DD}/2+0.3		V_{DD}/2+0.9	V
	Positive input threshold voltage, LPS inputs	$\overline{ISO}$ = 0 V, V_{DD_5V} = V_{DD}, V_{ref} = V_{DD} × 0.42			V_{ref}+1	
$V_{IT–}$	Negative input threshold voltage, LREQ, CTL0, CTL1, D0–D7 inputs‡	$\overline{ISO}$ = 0 V,V_{DD_5V} = V_{DD}	V_{DD}/2–0.9		V_{DD}/2–0.3	V
	Negative input threshold voltage, LPS inputs	$\overline{ISO}$ = 0 V, V_{DD_5V} = V_{DD}, V_{ref} = V_{DD} × 0.42	V_{ref}+0.2			
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V

† Measured at cable power side of resistor.
‡ This parameter applicable only when $\overline{ISO}$ low.

NOTES: 3. Repeat (receive on port0, transmit on ports 1 through 5, full ISO payload of 84 µs, S400, data value of CCCCCCCCh), V_{DD} = 3.3 V T_A = 25°C
4. Idle (receive cycle start on port0, xmt cycle start on ports 1 through 5), V_{DD} = 3.3 V, T_A = 25°C.

thermal characteristics

PARAMETER		TEST CONDITION†	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow, High conductivity TI recommended test board, Chip soldered or greased to thermal land with 1 oz. copper		17.85		°C/W
$R_{\theta JC}$	Junction-to-case-thermal resistance			0.12		
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow, High conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land with 1 oz. copper		28.22		°C/W
$R_{\theta JC}$	Junction-to-case-thermal resistance			0.12		

† Usage of thermally enhanced PowerPad PZP package is assumed in all three test conditions.

switching characteristics

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
	Jitter, transmit	Between TPA and TPB				±0.15	ns
	Skew, transmit	Between TPA and TPB				±0.10	ns
t_r	TP differential rise time, transmit	10% to 90%,	At 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit	90% to 10%,	At 1394 connector	0.5		1.2	ns
t_{su}	Setup time, CTL0, CTL1, D0–D7, LREQ to SYSCLK	50% to 50%	See Figure 2	5			ns
t_h	Hold time, CTL0, CTL1, D0–D7, LREQ after SYSCLK	50% to 50%	See Figure 2	2			ns
t_d	Delay time, SYSCLK to CTL0, CTL1, D0–D7	50% to 50%	See Figure 3	2		11	ns

PARAMETER MEASUREMENT INFORMATION

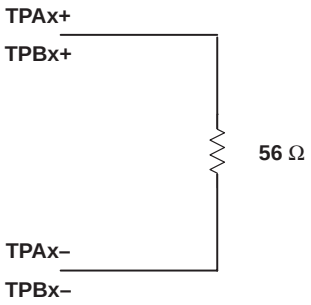


Figure 1. Test Load Diagram

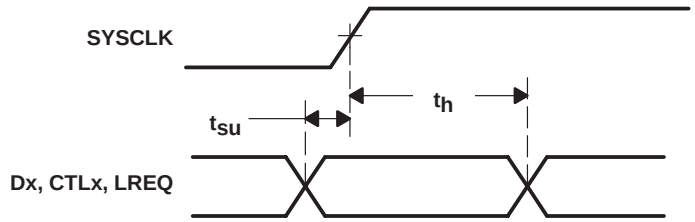


Figure 2. Dx, CTLx, LREQ Input Setup and Hold Time Waveforms

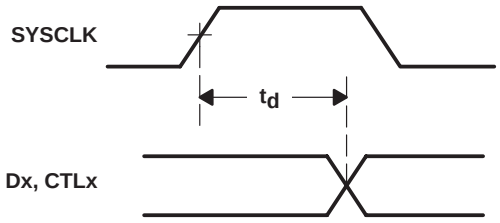


Figure 3. Dx and CTLx Output Delay Relative to SYSCLK Waveforms

APPLICATION INFORMATION

internal register configuration

There are 16 accessible internal registers in the TSB41LV06. The configuration of the registers at addresses 0 through 7 (the base registers) is fixed, while the configuration of the registers at addresses 8 through Fh (the paged registers) is dependent upon which one of eight pages, numbered 0 through 7, is currently selected. The selected page is set in base register 7.

The configuration of the base registers is shown in Table 1 and corresponding field descriptions given in Table 2. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the register configuration tables below) is read as 0, but is subject to future usage. All registers in pages 2 through 6 are reserved.

Table 1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Rsvd	Num_Ports (0110b)			
0011	PHY_Speed (010b)			Rsvd	Delay (0000b)			
0100	L	C	Jitter (000)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Rsvd	Port_Select			

Table 2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus-reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus-reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input pin. The CPS pin is normally tied to serial bus cable power through a 400 kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for guaranteed reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus-reset. The RHB bit is reset to 0 by hardware reset and is unaffected by bus-reset.
IBR	1	Rd/Wr	Initiate bus-reset. This bit instructs the PHY to initiate a long (166 μs) bus-reset at the next opportunity. Any receive or transmit operation in progress when this bit is set will complete before the bus-reset is initiated. The IBR bit is reset to 0 by hardware reset or bus-reset.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value is used to set the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count may be set either by a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is set to 3Fh by hardware reset or after two consecutive bus-resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	Rd	Extended register definition. For the TSB41LV06 this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the TSB41LV06 this field is 6.
PHY_Speed	3	Rd	PHY speed capability. For the TSB41LV06 PHY this field is 010b, indicating S400 speed capability.

APPLICATION INFORMATION

Table 2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
Delay	4	Rd	PHY repeater data delay. This field indicates the worst case repeater data delay of the PHY, expressed as 144+(delay × 20) ns. For the TSB41LV06 this field is 0.
L	1	Rd/Wr	Link-active status. This bit indicates that this node's link is active. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. This bit is set to 1 by hardware reset and is unaffected by bus-reset.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to the state specified by the C/LKON input pin upon hardware reset and is unaffected by bus-reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (JITTER+1) × 20 ns. For the TSB41LV06 this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node's power consumption and source characteristics, and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is set to the state specified by the PC0–PC2 input pins upon hardware reset and is unaffected by bus-reset. See Table 9.
RPIE	1	Rd/Wr	Resuming port interrupt enable. This bit, if set to 1, enables the port event interrupt (PIE) bit to be set whenever resume operations begin on any port. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus-reset. This bit, if set to 1, instructs the PHY to initiate a short (1.30 μs) arbitrated bus-reset at the next opportunity. This bit is reset to 0 by bus-reset. NOTE: Legacy IEEE Std 1394-1995 compliant PHYs may not be capable of performing short bus-resets. Therefore, initiation of a short bus-reset in a network that contains such a legacy device will result in a long bus-reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times-out during tree-ID start, and may indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. NOTE: If the network is configured in a loop, only those nodes that are part of the loop should generate a configuration time-out interrupt. All other nodes should instead time-out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in P1394a (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The EAA bit should be set only if the attached LLC is P1394a compliant. If the LLC is not P1394a compliant, use of the arbitration acceleration enhancements may interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multi-speed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in P1394a. This bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The use of multi-speed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multi-speed concatenation requires that the attached LLC be P1394a compliant.

APPLICATION INFORMATION

Table 2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
Page_Select	3	Rd/Wr	Page-select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by hardware reset and is unaffected by bus-reset.
Port_Select	4	Rd/Wr	Port-select. This field selects the port when accessing per-port status or control (e.g., when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus-reset.

The Port Status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. The configuration of the Port Status page registers is shown in Table 3 and corresponding field descriptions given in Table 4. If the selected port is un-implemented, all registers in the Port Status page are read as 0.

Table 3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	AStat		Bstat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	Rd	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: Code — Line State 11 — Z 01 — 1 10 — 0 00 — invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the ASTAT field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus–reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but the port is not necessarily active.
Bias	1	Rd	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 μs for the Bias bit to be set to 1.
Dis	1	Rd/Wr	Port disabled control. If 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus-reset.

APPLICATION INFORMATION

Table 4. Page 0 (Port Status) Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
Peer_Speed	3	Rd	Port peer speed. This field indicates the highest speed capability of the peer PHY connected to the selected port, encoded as follows: Code — Peer Speed 000 — S100 001 — S200 010 — S400 011–111 — invalid The Peer_Speed field is invalid after a bus-reset until self-ID has completed. NOTE: Peer speed codes higher than 010b (S400) are defined in P1394a. However, the TSB41LV06 is only capable of detecting peer speeds up to S400.
PIE	1	Rd/Wr	Port event interrupt enable. When set to 1, a port event on the selected port will set the port event interrupt (PEI) bit and notify the link. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.

The Vendor Identification page is used to identify the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. The configuration of the Vendor Identification page is shown in Table 5 and corresponding field descriptions given in Table 6.

Table 5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 6. Page 1 (Vendor ID) Register Field Description

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB41LV06 this field is 01h, indicating compliance with the P1394a specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB41LV06 this field is 08_00_28h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the TSB41LV06 this field is 46_xx_xxh (the MSB is at register address 1101b).

The Vendor-Dependent page provides access to the special control features of the TSB41LV06, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. The configuration of the Vendor-Dependent page is shown in Table 7 and corresponding field descriptions given in Table 8.

APPLICATION INFORMATION

Table 7. Page 7 (Vendor Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	NPA	Reserved					Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

Table 8. Page 7 (Vendor Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
NPA	1	Rd/Wr	Null-packet actions flag. This bit instructs the PHY to not clear fair and priority requests when a null packet is received with arbitration acceleration enabled. If 1, then fair and priority requests are cleared only when a packet of more than 8 bits is received; ACK packets (exactly 8 data bits), null packets (no data bits), and malformed packets (less than 8 data bits) will not clear fair and priority requests. If 0, then fair and priority requests are cleared when any non-ACK packet is received, including null-packets or malformed packets of less than 8 bits. This bit is cleared to 0 by hardware reset and is unaffected by bus-reset.
Link_Speed	2	Rd/Wr	Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows: Code Speed 00 S100 01 S200 10 S400 11 illegal This field is replicated in the sp field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the TSB41LV06 PHY identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to 10b (S400) by hardware reset and is unaffected by bus-reset.

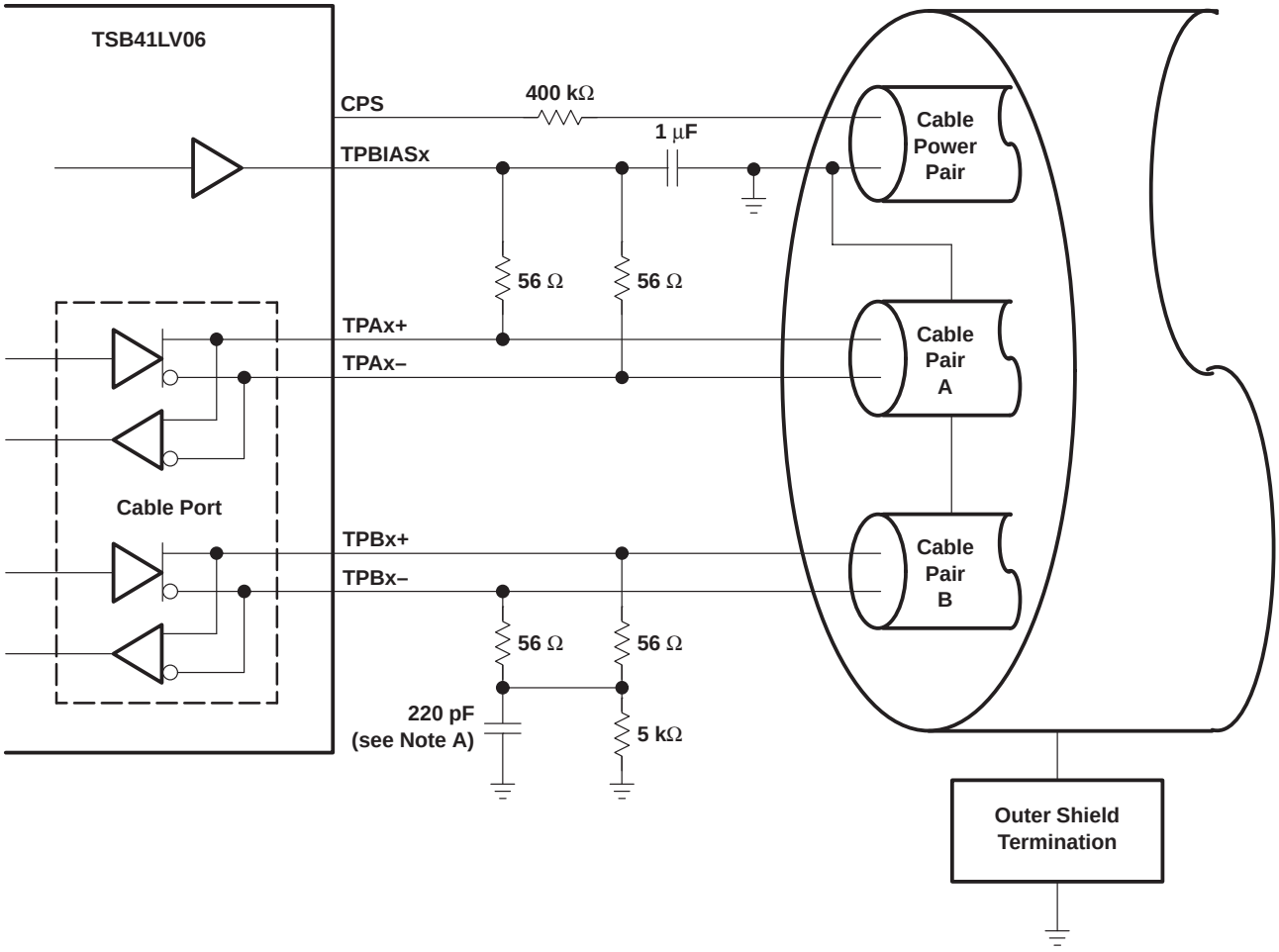
power-class programming

The PC0–PC2 pins are programmed to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in Table 9 The default power-class value is loaded following a hardware reset, but is overriden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 9. Power-Class Description

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus for the PHY only using up to 3W and may also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Node is powered from the bus and uses up to 3 W. An additional 2 W is needed to enable the link and higher layers of the node.
110	Node is powered from the bus and uses up to 3W. An additional 3W is needed to enable the link.
111	Node is powered from the bus and uses up to 3W. An additional 7W is needed to enable the link.

APPLICATION INFORMATION



NOTE A: The IEEE Std 1394-1995 calls for a 250 pF capacitor, which is a non-standard component value. A 220 pF capacitor is recommended.

Figure 4. TP Cable Connections

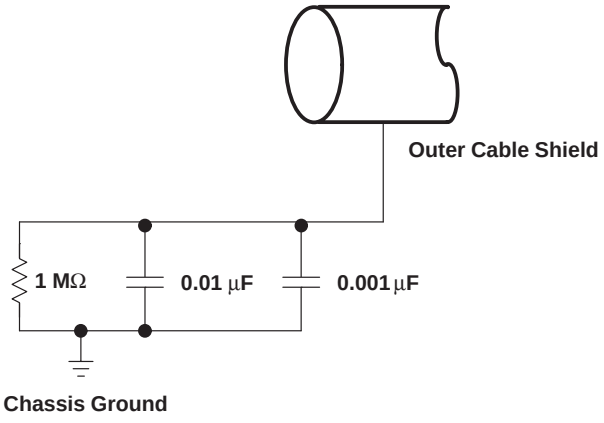


Figure 5. Compliant DC Isolated Outer Shield Termination

APPLICATION INFORMATION

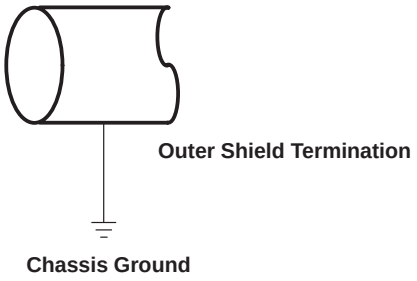


Figure 6. Non-Isolated Outer Shield Termination

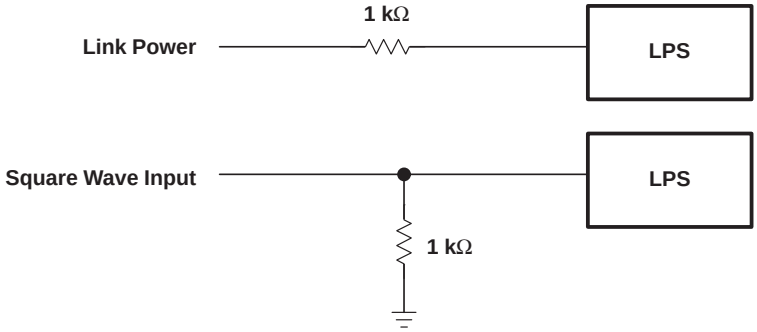


Figure 7. Non-Isolated Connection Variations for LPS

APPLICATION INFORMATION

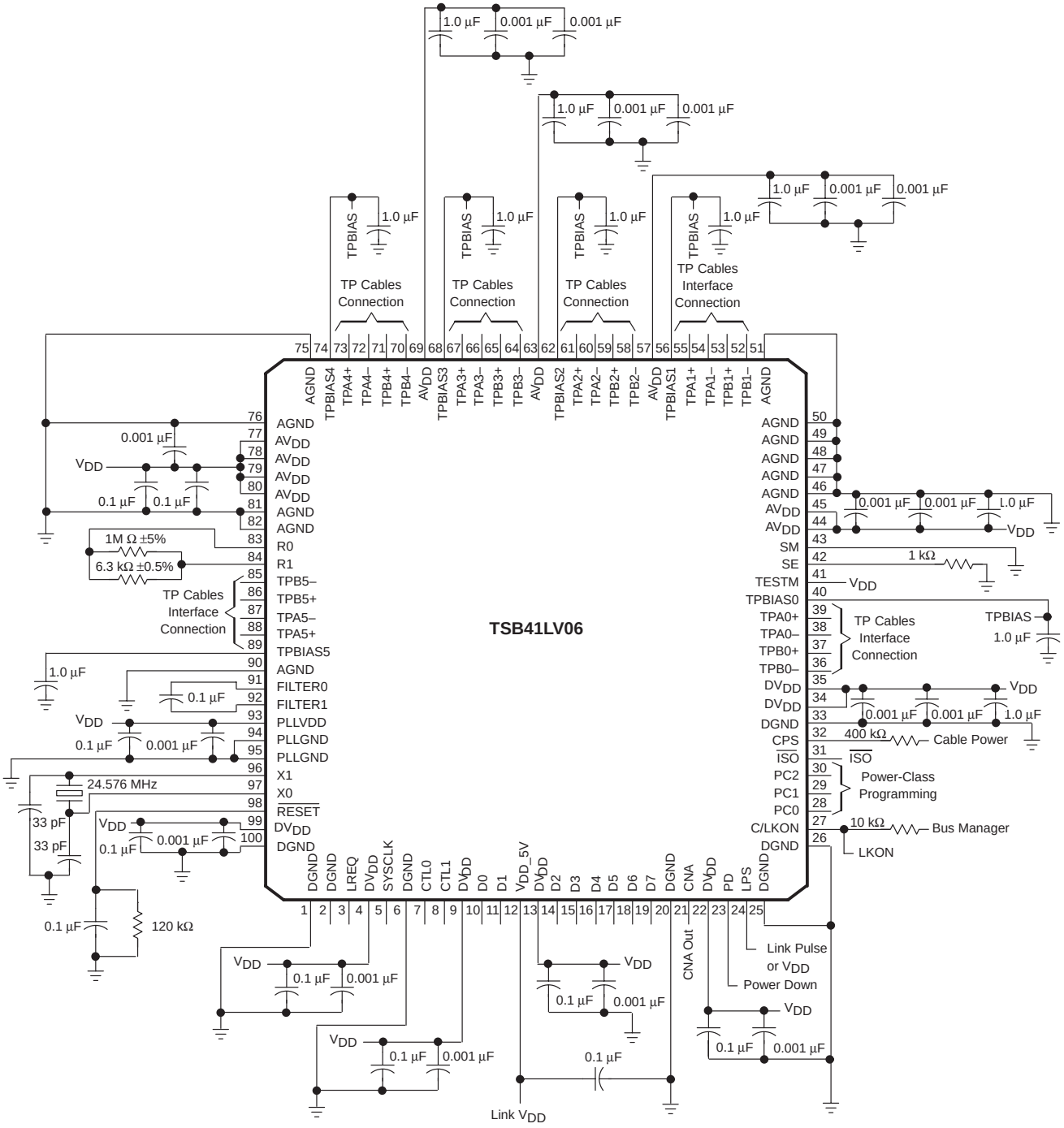


Figure 8. External Component Connections

APPLICATION INFORMATION

designing with PowerPAD

The TSB41LV06 is housed in a high performance, thermally enhanced, 100-pin PZP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 100-pin PZP PowerPAD package is 12 mm $\times$ 12 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land will vary in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com.

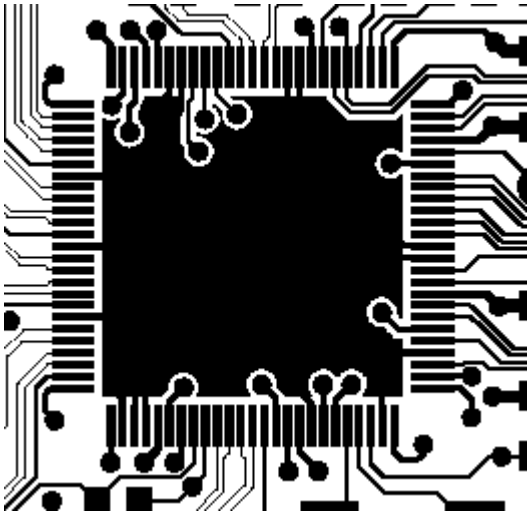


Figure 9. Example of a Thermal Land for the TSB41LV06 PHY

For the TSB41LV06, this thermal land should be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal pins. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

using the TSB41LV06 with a non-P1394a link layer

The TSB41LV06 implements the PHY-LLC interface specified in the P1394a Supplement. This interface is based upon the interface described in informative Annex J of IEEE Std 1394–1995, which is the interface used in older TI PHY devices. The PHY-LLC interface specified in P1394a is completely compatible with the older Annex J interface.

APPLICATION INFORMATION

using the TSB41LV06 with a non-P1394a link layer (continued)

The P1394a Supplement includes enhancements to the Annex J interface that must be comprehended when using the TSB41LV06 with a non-P1394a LLC device.

- A new LLC service request was added which allows the LLC to temporarily enable and disable asynchronous arbitration accelerations. If the LLC does not implement this new service request, the arbitration enhancements should not be enabled (see the EAA bit in PHY register 5).
- The capability to perform multispeed concatenation (the concatenation of packets of differing speeds) was added in order to improve bus efficiency (primarily during isochronous transmission). If the LLC does not support multispeed concatenation, multispeed concatenation should not be enabled in the PHY (see the EMC bit in PHY register 5).
- In order to accommodate the higher transmission speeds expected in future revisions of the standard, P1394A extended the speed code in bus requests from 2 bits to 3 bits, increasing the length of the bus request from 7 bits to 8 bits. The new speed codes were carefully selected so that new P1394a PHY and LLC devices would be compatible, for speeds from S100 to S400, with legacy PHY and LLC devices that use the 2-bit speed codes. The TSB41LV06 will correctly interpret both 7-bit bus requests (with 2-bit speed codes) and 8-bit bus requests (with 3-bit speed codes). Moreover, if a 7-bit bus request is immediately followed by another request (e.g., a register read or write request), the TSB41LV06 will correctly interpret both requests. Although the TSB41LV06 will correctly interpret 8-bit bus requests, a request with a speed code exceeding S400 will result in the TSB41LV06 transmitting a null packet (data-prefix followed by data-end, with no data in the packet).

More explanation is included in the TI application note *IEEE 1394a Features Supported by TI TSB41LV0X Physical Layer Devices,* TI literature number SLL019.

using the TSB41LV06 with a lower-speed link layer

Although the TSB41LV06 is an S400 capable PHY, it may be used with lower speed LLCs, such as the S200 capable TSB12LV31. In such a case, the LLC has fewer data terminals than the PHY, and some Dn terminals on the TSB41LV06 will be unused. Unused Dn terminals should be pulled to ground through 10 kΩ resistors.

The TSB41LV06 transfers all received packet data to the LLC, even if the speed of the packet exceeds the capability of the LLC to accept it. Some lower speed LLC designs do not properly ignore packet data in such cases. On the rare occasions that the first 16 bits of partial data accepted by such a LLC match a node's bus and node ID, spurious header CRC or tcode errors may result.

During bus initialization following a bus-reset, each PHY transmits a self-ID packet that indicates, among other information, the speed capability of the PHY. The bus manager (if one exists) builds a speed-map from the collected self-ID packets. This speed-map gives the highest possible speed that can be used on the node-to-node communication paths between every pair of nodes in the network.

In the case of a node consisting of a higher-speed PHY and a lower-speed LLC, the speed capability of the node (PHY and LLC in combination) is that of the lower-speed LLC. A sophisticated bus manager may be able to determine the LLC speed capability by reading the configuration ROM Bus_Info_Block, or by sending asynchronous request packets at different speeds to the node and checking for an acknowledge; the speed-map may then be adjusted accordingly. The speed-map should reflect that communication to such a node must be done at the lower speed of the LLC, instead of the higher speed of the PHY. However, speed-map entries for paths that merely pass through the node's PHY, but do not terminate at that node, should not be restricted by the lower speed of the LLC.

APPLICATION INFORMATION

using the TSB41LV06 with a lower-speed link layer (continued)

To assist in building an accurate speed-map, the TSB41LV06 has the capability of indicating a speed capability other than S400 in its transmitted self-ID packet. This is controlled by the Link_Speed field in register 8 of the Vendor-Dependent page (page 7). Setting the Link_Speed field affects only the speed indicated in the self-ID packet; it has no effect on the speed signaled to peer PHYs during self-ID. The TSB41LV06 identifies itself as S400 capable to its peers regardless of the value in the Link_Speed field.

Generally, the Link_Speed field should not be changed from its power-on default value of S400 unless it is determined that the speed-map (if one exists) is incorrect for path entries terminating in the local node. If the speed-map is incorrect, it can be assumed that the bus manager has used only the self-ID packet information to build the speed-map. In this case, the node may update the Link_Speed field to reflect the lower speed capability of the LLC and then initiate another bus-reset to cause the speed-map to be rebuilt. Note that in this scenario any speed-map entries for node-to-node communication paths that pass through the local node's PHY will be restricted by the lower speed.

In the case of a leaf node (which has only one active port) the Link_Speed field may be set to indicate the speed of the LLC without first checking the speed–map. Changing the Link_Speed field in a leaf node can only affect those paths that terminate at that node, since no other paths can pass through a leaf node. It can have no effect on other paths in the speed-map. For hardware configurations which can only be a leaf node (all ports but one are unimplemented), it is recommended that the Link_Speed field be updated immediately after power-on or hardware reset.

power-up reset

To ensure proper operation of the TSB41LV06 the $\overline{\text{RESET}}$ pin must be asserted low for a minimum of 2 ms from the time that PHY power reaches the minimum required supply voltage. When using a passive capacitor on the $\overline{\text{RESET}}$ pin to generate a power-on reset signal, the minimum reset time will be assured if the capacitor has a minimum value of 0.1 μF and also satisfies the following equation:

$$C_{min} = 0.0077 \times T + 0.085$$

where C_{min} is the minimum capacitance on the $\overline{\text{RESET}}$ pin in μF, and T is the V_{DD} ramp time, 10%–90%, in ms.

Additionally, an approximately 120-kΩ resistor should be connected in parallel with the reset capacitor from the $\overline{\text{RESET}}$ terminal to GND to ensure that the capacitor is discharged when PHY power is removed. An alternative to the passive reset is to actively drive $\overline{\text{RESET}}$ low for the minimum reset time following power on.

crystal selection

TI PHYs may use an external 24.576 MHz crystal connected between the XI and XO pins on the PHY to provide the PHY clock. The following are some typical specifications for the crystals used with the Physical Layers from TI. The clock resulting from the input from the crystal must be within the tolerance of ±100 parts per million for the PHYs to function correctly. This is required by the 1394 standard. This frequency tolerance for the PHY clocks on each node must be maintained over the variation introduced over production runs of boards and environment the machines operate. Every board must have an SYSCLK (clock generated by the PHY) within ±100 ppm of 49.152 MHz to be compliant to the 1394 standard. If adjacent nodes are more than 200ppm away from one another then long packets sent across the 1394 bus may be corrupted, with the final bits of the packet being lost. TI PHYs are designed with a maximum of margin, but must still adhered to the limits imposed by 1394.

APPLICATION INFORMATION

crystal selection (continued)

1. Crystal Mode of operation:
   Fundamental

2. Frequency Tolerance at 25°C:
   Total variation specification for the complete circuit is 100ppm. The crystal is specified at less than 100 ppm. It is currently recommended ours at ±30 ppm.

3. Frequency stability (over temperature):
   Total variation specification for the complete circuit is 100 ppm. The crystal is specified at less than 100 ppm. It is currently recommended ours at ±30ppm.

   NOTE:
   The total variation must be kept below 100 ppm with some allowance for variation introduced by variations in board builds and device tolerances. So the sum of the frequency tolerance and the frequency stability must be less than 100 ppm. This can be traded between the two, for example the frequency tolerance may be specified at 50 ppm and the temperature may be specified at 30 ppm to give a total of 80 ppm possible variation just due to the crystal. Aging of the crystal also contributes to the net ppm.

4. Load capacitance: [Parallel (pF)]
   Parallel mode crystal circuits have been used since they should be matched to the onchip oscillator. Load capacitance will be a function of the board layout and circuit. The total load capacitance (CL) will affect the frequency the crystal oscillates at. Consult with a crystal vendor and iterate the design to get an SYSCLK supplied by the PHY to less than 100 ppm from 49.152 MHz . It is recommended that a maximum of ±5% tolerance load capacitors be used. For our OHCI + 41LV03 Evaluation Module (EVM) with a crystal specified for 20pF loading, a value of 33 pF for each load capacitor (C9 = C10 below) was found to be appropriate with the layout used for the board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY pins (C_{PHY}), and the loading of the board itself (C_{BD}). To summarize: C_L =[(C9 × C10) / (C9+C10)] + C_{PHY} + C_{BD}. Representative values for C_{PHY} are ~1 pF and for C_{BD} are about 0.8 pF per centimeter of board etch, a typical board can have from 3 pF to 6 pF or more. The capacitance of load capacitors C9 and C10 combine as capacitors in series.

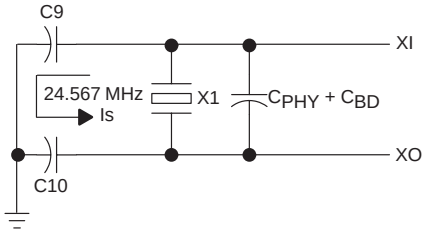


Figure 10. Load Capacitance for the TSB41LV06 PHY

APPLICATION INFORMATION

crystal selection (continued)

NOTE:

The layout of the crystal portion of the PHY circuit is important for getting the correct frequency from the crystal, minimizing the noise introduced into the PHY Phase Lock Loop, and minimizing any emissions from the circuit. The crystal and the two load capacitors should be considered a unit during layout. The crystal and the load capacitors should be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors may help in this. Minimizing the loop area minimizes the effect of the resonant current (Is) that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY XI and XO pins to minimize etch lengths.

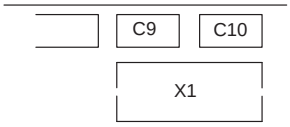


Figure 11. Recommended Crystal and Capacitor Layout for the TSB41LV06 PHY

It is strongly recommend that part of the verification process for the design be to measure the frequency of the SYSCLK put out by the PHY. This should be done with a frequency counter with an accuracy of 6 digits or better. If the SYSCLK is more than the crystal tolerance away from 49.152 MHz, the load capacitance of the crystal may be varied to see if this brings it into line. If the frequency is too high add more load capacitance, if the frequency is too low decrease load capacitance. Typically changes should be done to both load capacitors (C9 and C10 above) at the same time to the same value. It is suggested that a consultation with the crystal vendors for a more detailed understanding of what is required. In order for a 1394 bus to operate correctly each SYSCLK on each node on the bus must be within 200 ppm of the adjacent SYSCLK on the bus. The 1394 standard requires this by specifying a center frequency of 49.152 MHz and a ±100 ppm tolerance around 49.152 MHz.

bus reset

To initiate a bus reset from software (SW) for a 1394-1995 PHY layer, the link layer uses the PHY chip access register to write into PHY register 0001b. This changes the state of the initiate bus reset (IBR) bit. This bit is in the same register as the gap count and root hold–off bit (RHB). Anytime the IBR bit is set, the gap count and RHB are also set. The following is the recommended IBR sequence: read the PHY register 0001b, change only the bits that need to be changed making sure to keep all other bits the same, and finally write a new value to the PHY register 0001b. There is only one case in which a value other than 3Fh should ever be written into the gap count field. This case occurs during the initiation of a bus reset immediately after a PHY configuration packet. The PHY configuration packet is sent to set the gap counts of each node to the same value. In this case, during the write to set the IBR bit, the gap count should be the same as the gap count written by the immediately previous PHY configuration packet. This is required since after every two bus resets (unless a gap count register write occurs between the bus resets) all gap counts are reset to the default value of 3Fh.

PRINCIPLES OF OPERATION

The TSB41LV06 is designed to operate with a LLC such as the Texas Instruments TSB12LV21, TSB12LV31, TSB12LV41, TSB12LV01, or TSB12LV22. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface.

The interface to the LLC consists of the SYSCLK, CTL0–CTL1, D0–D7, LREQ, LPS, C/LKON, and $\overline{\text{ISO}}$ terminals on the TSB41LV06, as shown in Figure 12.

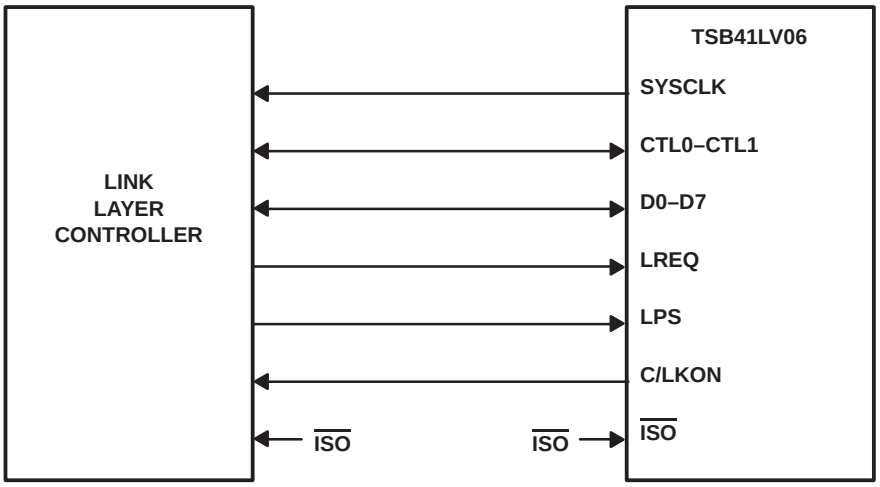


Figure 12. PHY-LLC Interface

The SYSCLK terminal provides a 49.152 MHz interface clock. All control and data signals are synchronized to, and sampled on, the rising edge of SYSCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB41LV06 and LLC.

The D0–D7 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the devices. The TSB41LV06 supports S100, S200, and S400 data transfers over the D0–D7 data bus. In S100 operation only the D0 and D1 terminals are used; in S200 operation only the D0–D3 terminals are used; and in S400 operation all D0–D7 terminals are used for data transfer. When the TSB41LV06 is in control of the D0–D7 bus, unused Dn terminals are driven low during S100 and S200 operations. When the LLC is in control of the D0–D7 bus, unused Dn terminals are ignored by the TSB41LV06.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to the serial-bus for packet transmission, read or write PHY registers, or control arbitration acceleration.

The LPS and C/LKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and may be used to reset the PHY-LLC interface or to disable SYSCLK. The C/LKON terminal is used to send a wake-up notification to the LLC and to indicate an interrupt to the LLC when either LPS is inactive or the PHY register L bit is zero.

The /ISO terminal is used to enable the output differentiation logic on the CTL0–CTL1 and D0–D7 terminals. Output differentiation is required when an isolation barrier of the type described in Annex J of IEEE Std 1394–1995 is implemented between the PHY and LLC.

The TSB41LV06 normally controls the CTL0–CTL1 and D0–D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

There are four operations that may occur on the PHY–LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register, to request the PHY to gain control of the serial-bus in order to transmit a packet, or to control arbitration acceleration.

PRINCIPLES OF OPERATION

The PHY may initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation whenever a packet is received from the serial-bus.

The PHY initiates a transmit operation after winning control of the serial-bus following a bus-request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

The encoding of the CTL0–CTL1 bus is shown in Table10 and Table 11.

Table 10. CTL Encoding When PHY Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC
1	0	Receive	An incoming packet is being sent from the PHY to the LLC
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet

Table 11. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL0	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed)
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission, or indicating that another packet is to be transmitted (concatenated) without arbitrating
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY
1	1	Reserved	None

LLC service request

To request access to the bus, to read or write a PHY register, or to control arbitration acceleration, the LLC sends a serial bit stream on the LREQ terminal as shown in Figure 13.

NOTE: Each cell represents one clock sample time, and n is the number of bits in the request stream.

Figure 13. LREQ Request Stream

The length of the stream will vary depending on the type of request as shown in Table 12.

Table 12. LLC Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus Request	7 or 8
Read Register Request	9
Write Register Request	17
Acceleration Control Request	6

PRINCIPLES OF OPERATION

LLC service request (continued)

Regardless of the type of request, a start-bit of 1 is required at the beginning of the stream, and a stop-bit of 0 is required at the end of the stream. The second through fourth bits of the request stream indicate the type of the request. In the descriptions below, bit 0 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Encoding for the request type is shown in Table 13.

Table 13. Request Type Encoding

LR1–LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. Upon detection of idle, the PHY takes control of the bus immediately without arbitration.
001	IsoReq	Isochronous bus request. Upon detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq	Priority bus request. The PHY arbitrates for the bus after a subaction gap, ignores the fair protocol.
011	FairReq	Fair bus request. The PHY arbitrates for the bus after a subaction gap, follows the fair protocol.
100	RdReg	The PHY returns the specified register contents through a status transfer.
101	WrReg	Write to the specified register.
110	AccelCtl	Enable or disable asynchronous arbitration acceleration.
111	Reserved	Reserved

For a Bus Request the length of the LREQ bit stream is 7 or 8 bits as shown in Table 14.

Table 14. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1-3	Request Type	Indicates the type of bus request. See Table 13.
4-6	Request Speed	Indicates the speed at which the PHY will send the data for this request. See Table 15 for the encoding of this field.
7	Stop Bit	Indicates the end of the transfer (always 0). If bit 6 is 0, this bit may be omitted.

The 3-bit Request Speed field used in bus requests is shown in Table 15.

Table 15. Bus Request Speed Encoding

LR4–LR6	DATA RATE
000	S100
010	S200
100	S400
All Others	Invalid

NOTE:
The TSB41LV06 will accept a bus request with an invalid speed code and process the bus request normally. However, during packet transmission for such a request, the TSB41LV06 will ignore any data presented by the LLC and will transmit a null packet.

PRINCIPLES OF OPERATION

LLC service request (continued)

For a Read Register Request the length of the LREQ bit stream is 9 bits as shown in Table 16.

Table 16. LLC Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1-3	Request Type	A 100 indicating this is a read register request.
4-7	Address	Identifies the address of the PHY register to be read.
8	Stop Bit	Indicates the end of the transfer (always 0).

For a Write Register Request the Length of the LREQ data stream is 17 bits as shown in Table 17.

Table 17. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1-3	Request Type	A 101 indicating this is a write register request.
4-7	Address	Identifies the address of the PHY register to be written to.
8-15	Data	Gives the data that is to be written to the specified register address.
16	Stop Bit	Indicates the end of the transfer (always 0).

For an Acceleration Control Request the Length of the LREQ data stream is 6 bits as shown in Table 18.

Table 18. Acceleration Control Request

BIT(s)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1-3	Request Type	A 110 indicating this is an acceleration control request.
4	Control	Asynchronous period arbitration acceleration is enabled if 1, and disabled if 0.
5	Stop Bit	Indicates the end of the transfer (always 0).

For fair or priority access, the LLC sends the bus request (FairReq or PriReq) at least one clock after the PHY-LLC interface becomes idle. If the CTL terminals are asserted to the Receive state (10b) by the PHY, then any pending fair or priority request is lost (cleared). Additionally, the PHY ignores any fair or priority requests if the Receive state is asserted while the LLC is sending the request. The LLC may then reissue the request one clock after the next interface idle.

The cycle master node uses a priority bus request (PriReq) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY will clear an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required in order to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the receive packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released the LLC may proceed with another request.

PRINCIPLES OF OPERATION

LLC service request (continued)

The LLC may make only one bus request at a time. Once the LLC issues any request for bus access (ImmReq, IsoReq, FairReq, or PriReq), it cannot issue another bus request until the PHY indicates that the bus request was lost (bus arbitration lost and another packet received), or won (bus arbitration won and the LLC granted control). The PHY ignores new bus requests while a previous bus request is pending. All bus requests are cleared upon a bus reset.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a status transfer. If a received packet interrupts the status transfer, then the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request may be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

The TSB41LV06 includes several arbitration acceleration enhancements, which allow the PHY to improve bus performance and throughput by reducing the number and length of interpacket gaps. These enhancements include autonomous (fly-by) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. The enhancements are enabled when the EAA bit in PHY register 5 is set.

The arbitration acceleration enhancements may interfere with the ability of the cycle master node to transmit the cycle start message under certain circumstances. The acceleration control request is therefore provided to allow the LLC to temporarily enable or disable the arbitration acceleration enhancements of the TSB41LV06 during the asynchronous period. The LLC typically disables the enhancements when its internal cycle counter rolls over indicating that a cycle start message is imminent, and then re-enables the enhancements when it receives a cycle start message. The acceleration control request may be made at any time, however, and is immediately serviced by the PHY. Additionally, a bus reset or isochronous bus request will cause the enhancements to be re-enabled, if the EAA bit is set.

status transfer

A status transfer is initiated by the PHY when there is status information to be transferred to the LLC. The PHY waits until the interface is idle before starting the transfer. The transfer is initiated by the PHY asserting *Status* (01b) on the CTL terminals, along with the first two bits of status information on the D[0:1] terminals. The PHY maintains CTL = *Status* for the duration of the status transfer. The PHY may prematurely end a status transfer by asserting something other than *Status* on the CTL terminals. This occurs if a packet is received before the status transfer completes. The PHY continues to attempt to complete the transfer until all status information has been successfully transmitted. There is at least one idle cycle between consecutive status transfers.

The PHY normally sends just the first four bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The PHY sends an entire 16-bit status packet to the LLC after a read register request, or when the PHY has pertinent information to send to the LLC or transaction layers. The only defined condition where the PHY automatically sends a register to the LLC is after self-ID, where the PHY sends the physical–ID register that contains the new node address. All status transfers are either 4 or 16 bits unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the LLC immediately upon being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent, or if a register transfer has not yet completed.

PRINCIPLES OF OPERATION

status transfer (continued)

The definition of the bits in the status transfer are shown in Figure 14 Table 19 and the timing is shown in Figure 14.

Table 19. Status Bits

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time (as defined in the IEEE 1394–1995 standard). This bit is used by the LLC in the busy/retry state machine.
1	Subaction Gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in the IEEE 1394–1995 standard). This bit is used by the LLC to detect the completion of an isochronous cycle.
2	Bus Reset	Indicates that the PHY has entered the bus reset state.
3	Interrupt	Indicates that a PHY interrupt event has occurred. An interrupt event may be a configuration time-out, cable-power voltage falling too low, a state time-out, or a port status change.
4–7	Address	This field holds the address of the PHY register whose contents are being transferred to the LLC.
8–15	Data	This field holds the register contents.

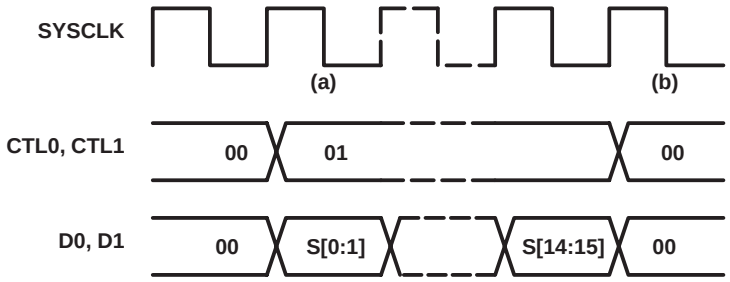


Figure 14. Status Transfer Timing

The sequence of events for a status transfer is as follows:

1. Status transfer initiated. The PHY indicates a status transfer by asserting status on the CTL lines along with the status data on the D0 and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by a receive operation), a status transfer will be either 2 or 8 cycles long. A 2-cycle (4 bit) transfer occurs when only status information is to be sent. An 8-cycle (16 bit) transfer occurs when register data is to be sent in addition to any status information.
2. Status transfer terminated. The PHY normally terminates a status transfer by asserting Idle on the CTL lines. The PHY may also interrupt a status transfer at any cycle by asserting receive on the CTL lines to begin a receive operation. The PHY shall assert at least one cycle of Idle between consecutive status transfers. The PHY may also assert Grant on the CTL lines immediately following a complete status transfer.

receive

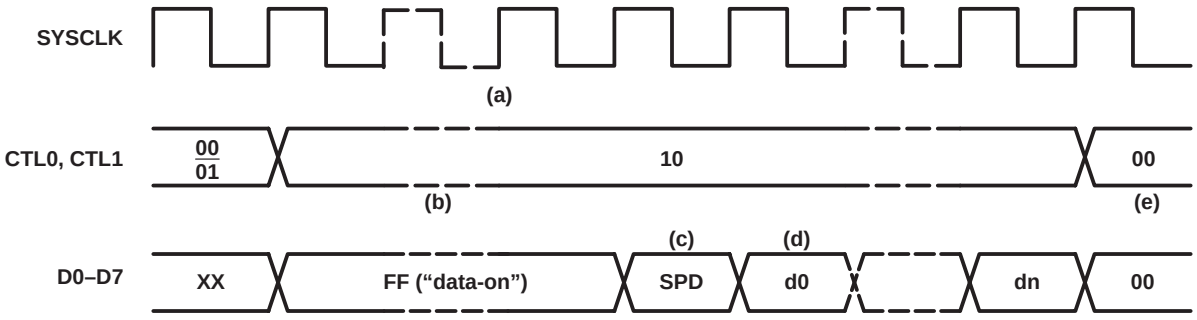
Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting Receive on the CTL terminals and a logic 1 on each of the D terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 5 on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting Idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

PRINCIPLES OF OPERATION

receive (continued)

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY will assert Receive on the CTL terminals with the data-on indication (all 1s) on the D terminals, followed by Idle on the CTL terminals, without any speed code or data being transferred. In all cases, the TSB41LV06 sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB41LV06 also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet it transferred to the LLC just as any other received self-ID packet.



NOTE B: SPD = Speed code, see Table 20 d0–dn = Packet data

Figure 15. Normal Packet Reception Timing

The sequence of events for a normal packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is Idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening Idle.
2. Data-on indication. The PHY may assert the data-on indication code on the D lines for zero or more cycles preceding the speed-code.
3. Speed-code. The PHY indicates the speed of the received packet by asserting a speed-code on the D lines for one cycle immediately preceding packet data. The link decodes the speed-code on the first receive cycle for which the D lines are not the data-on code. If the speed-code is invalid, or indicates a speed higher that that which the link is capable of handling, the link should ignore the subsequent data.
4. Receive data. Following the data-on indication (if any) and the speed-code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.
5. Receive operation terminated. The PHY terminates the receive operation by asserting Idle on the CTL lines. The PHY asserts at least one cycle of Idle following a receive operation.

PRINCIPLES OF OPERATION

receive (continued)

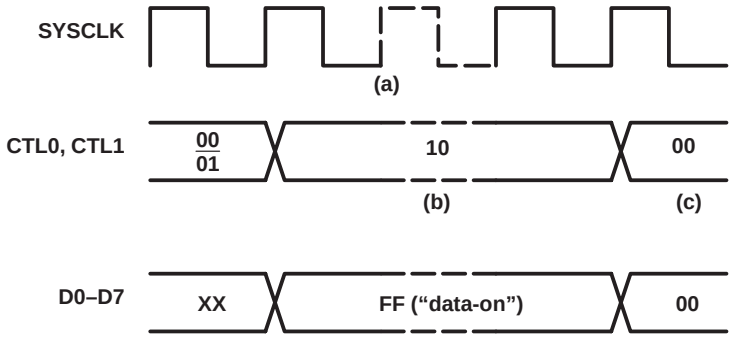


Figure 16. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting Receive on the CTL lines. Normally, the interface is Idle when Receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from Status to Receive without an intervening Idle.
2. Data–on indication. The PHY asserts the data–on indication code on the D lines for one or more cycles.
3. Receive operation terminated. The PHY terminates the receive operation by asserting Idle on the CTL lines. The PHY shall assert at least one cycle of Idle following a receive operation.

Table 20. Receive Speed Codes

D0–D7	DATA RATE
00XX XXXX	S100
0100 XXXX	S200
0101 0000	S400
1YYY YYYY	“data–on” indication

NOTE: X = Output as 0 by PHY, ignored by LLC.
Y = Output as 1 by PHY, ignored by LLC

transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, the PHY-LLC interface bus is granted to the LLC by asserting the Grant state (11b) on the CTL terminals for one SYSCLK cycle, followed by Idle for one clock cycle. The LLC then takes control of the bus by asserting either Idle (00b), hold (01b) or transmit (10b) on the CTL terminals. Unless the LLC is immediately releasing the interface, the LLC may assert the Idle state for at most one clock before it must assert either hold or transmit on the CTL terminals. The hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC may assert hold for zero or more clock cycles (i.e., the LLC need not assert hold before transmit). The PHY asserts data-prefix on the serial bus during this time.

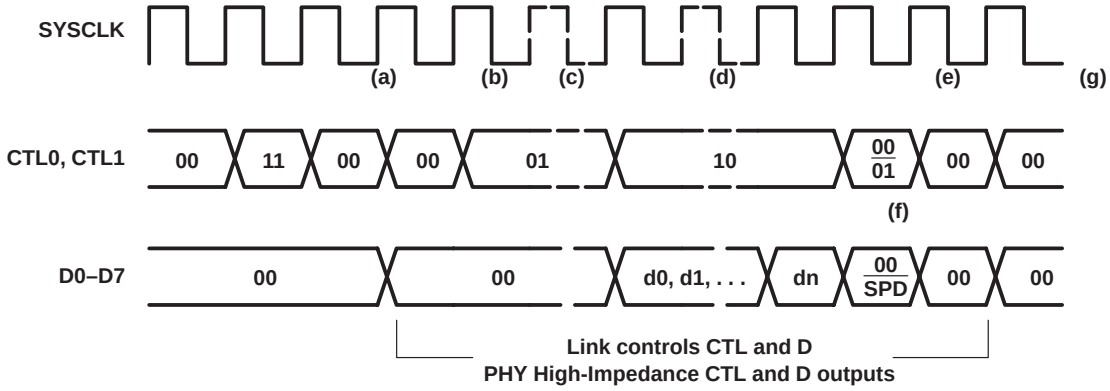
PRINCIPLES OF OPERATION

transmit (continued)

When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either Hold or Idle on the CTL terminals for one clock cycle, and then asserts Idle for one additional cycle before releasing the interface bus and 3-stating the CTL and D terminals. The PHY then regains control of the interface bus.

The hold state asserted at the end of packet transmission indicates to the PHY that the LLC requests to send another packet (concatenated packet) without releasing the serial bus. The PHY responds to this concatenation request by waiting the required minimum packet separation time and then asserting Grant as before. This function may be used to send a unified response after sending an acknowledge, or to send consecutive isochronous packets during a single isochronous period. Unless multispeed concatenation is enabled, all packets transmitted during a single bus ownership must be of the same speed (since the speed of the packet is set before the first packet). If multispeed concatenation is enabled (when the EMSC bit of PHY register 5 is set), the LLC must specify the speed code of the next concatenated packet on the D terminals when it asserts hold on the CTL terminals at the end of a packet. The encoding for this speed code is the same as the speed code that precedes received packet data as given in Table 20.

After sending the last packet for the current bus ownership, the LLC releases the bus by asserting Idle on the CTL terminals for two clock cycles. The PHY begins asserting idle on the CTL terminals one clock after sampling idle from the link. Note that whenever the D and CTL terminals change direction between the PHY and the LLC, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals.



NOTE A: SPD = Speed code, see Table 20 d0–dn = Packet data

Figure 17. Normal Packet Transmission Timing

PRINCIPLES OF OPERATION

transmit (continued)

The sequence of events for a normal packet transmission is as follows:

1. Transmit operation initiated. The PHY asserts Grant on the CTL lines followed by Idle to hand over control of the interface to the link so that the link may transmit a packet. The PHY releases control of the interface (i.e., it 3-states the CTL and D outputs) following the Idle cycle.
2. Optional idle cycle. The link may assert at most one idle cycle preceding assertion of either hold or transmit. This idle cycle is optional; the link is not required to assert Idle preceding either hold or transmit.
3. Optional hold cycles. The link may assert hold for up to 47 cycles preceding assertion of transmit. These hold cycle(s) are optional; the link is not required to assert hold preceding transmit.
4. Transmit data. When data is ready to be transmitted, the link asserts transmit on the CTL lines along with the data on the D lines.
5. Transmit operation terminated. The transmit operation is terminated by the link asserting hold or idle on the CTL lines. The link asserts hold to indicate that the PHY is to retain control of the serial bus in order to transmit a concatenated packet. The link asserts Idle to indicate that packet transmission is complete and the PHY may release the serial bus. The link then asserts Idle for one more cycle following this cycle of hold or idle before releasing the interface and returning control to the PHY.
6. Concatenated packet speed-code. If multispeed concatenation is enabled in the PHY, the link shall assert a speed-code on the D lines when it asserts hold to terminate packet transmission. This speed-code indicates the transmission speed for the concatenated packet that is to follow. The encoding for this concatenated packet speed-code is the same as the encoding for the received packet speed-code (see Table 20. The link may not concatenate an S100 packet onto any higher-speed packet.
7. After regaining control of the interface, the PHY shall assert at least one cycle of Idle before any subsequent status transfer, receive operation, or transmit operation.

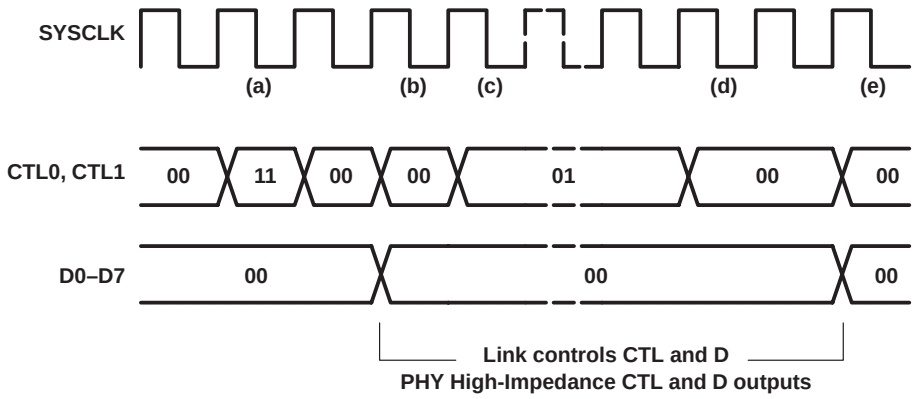


Figure 18. Cancelled/Null packet Transmission

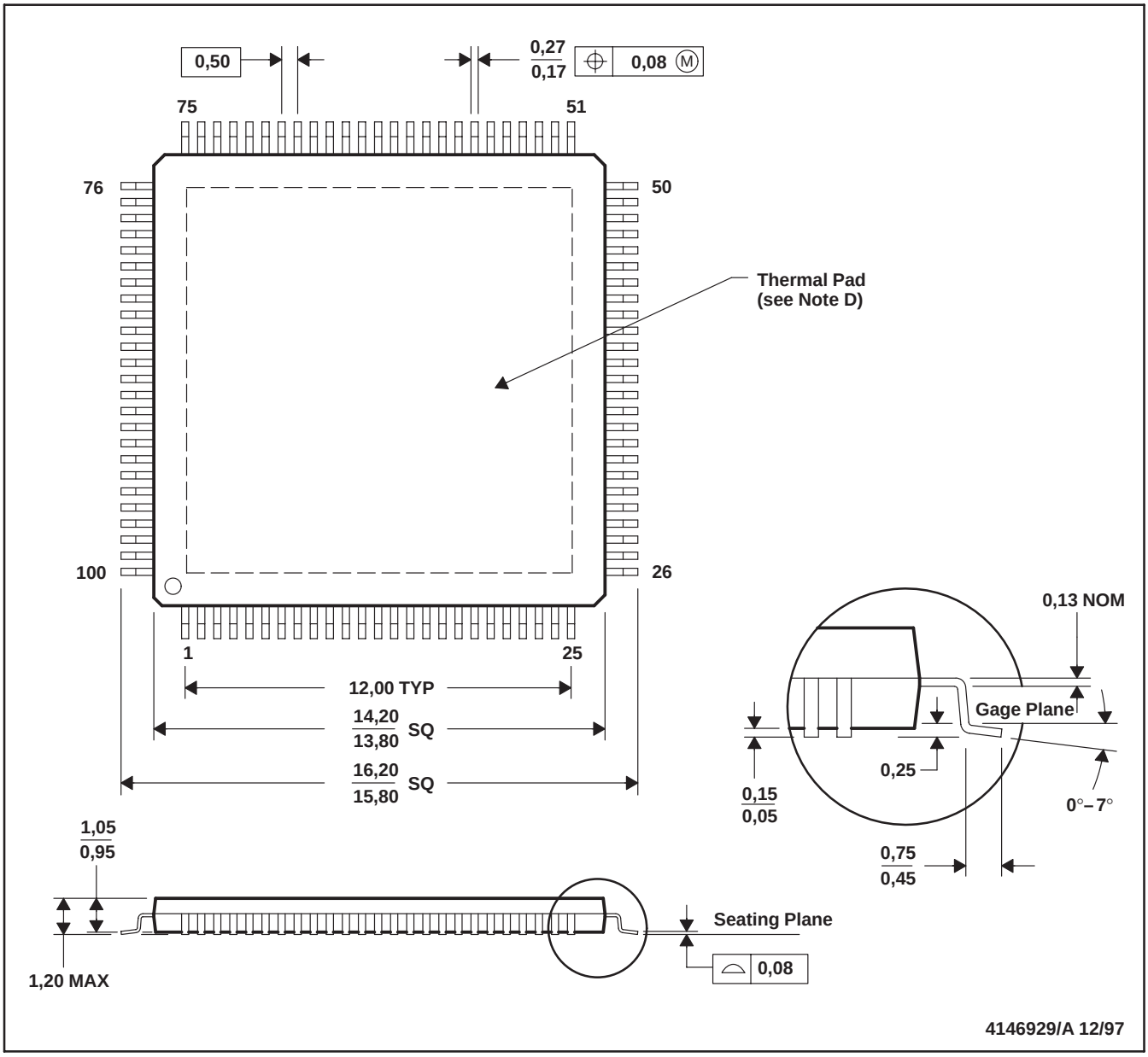
transmit (continued)

The sequence of events for a cancelled/null packet transmission is as follows:

1. Transmit operation initiated. PHY asserts Grant on the CTL lines followed by Idle to hand over control of the interface to the link.
2. Optional idle cycle. The link may assert at most one Idle cycle preceding assertion of hold. This idle cycle is optional; the link is not required to assert Idle preceding hold.
3. Optional hold cycles. The link may assert hold for up to 47 cycles preceding assertion of Idle. These hold cycle(s) are optional; the link is not required to assert hold preceding idle.
4. Null transmit termination. The null transmit operation is terminated by the link asserting two cycles of Idle on the CTL lines and then releasing the interface and returning control to the PHY. Note that the link may assert idle for a total of 3 consecutive cycles if it asserts the optional first idle cycle but does not assert hold. (It is recommended that the link assert 3 cycles of Idle to cancel a packet transmission if no hold cycles are asserted. This guarantees that either the link or PHY controls the interface in all cycles.)
5. After regaining control of the interface, the PHY shall assert at least one cycle of idle before any subsequent status transfer, receive operation, or transmit operation.

MECHANICAL DATA

PZP (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments Incorporated.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.