

400 μ A High-Speed Operational Amplifier

- OptimWatt™ device featuring ultra-low consumption, 2mW, and low quiescent current, 400 μ A
- Bandwidth: 120MHz (Gain=2)
- Slew rate: 115V/ μ s
- Specified on 1k Ω
- Input noise: 7.5nV/ \sqrt Hz
- Tested on 5V power supply

Description

The TSH310 is a very low-power, high-speed operational amplifier. A bandwidth of 120MHz is achieved while drawing only 400 μ A of quiescent current. This low-power characteristic is particularly suitable for high-speed, battery-powered equipment requiring dynamic performance.

The TSH310 is a single operator available in SO8 and the tiny SOT23-5 plastic package, saving board space as well as providing excellent thermal performances.

Applications

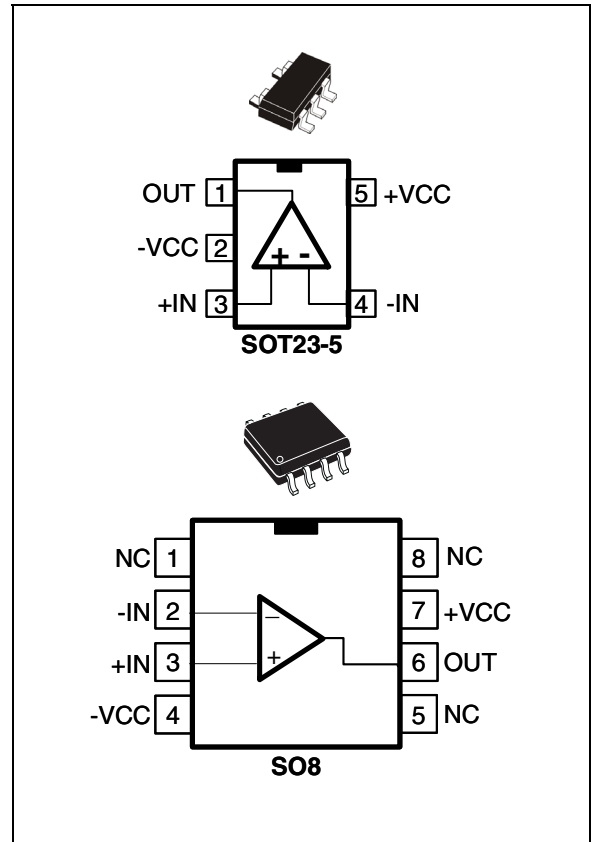
- Battery-powered and high-speed systems
- Communication & video test equipment
- Portable medical instrumentation
- ADC drivers

Order Codes

Part Number	Temperature Range	Package	Conditioning	Marking
TSH310ILT	-40°C to +85°C	SOT23-5	Tape&Reel	K304
TSH310ID		SO-8	Tube	TSH310I
TSH310IDT		SO-8	Tape&Reel	TSH310I

Note: OptimWatt™ is an STMicroelectronics registered trademark that applies to products with specific features that optimize energy efficiency.

Pin Connections (top view)



1 Absolute Maximum Ratings

Table 1: Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage ¹	6	V
V_{id}	Differential Input Voltage ²	+/-0.5	V
V_{in}	Input Voltage Range ³	+/-2.5	V
T_{oper}	Operating Free Air Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient		
	SOT23-5 SO8	250 150	°C/W
R_{thjc}	Thermal Resistance Junction to Case		
	SOT23-5 SO8	80 28	°C/W
P_{max}	Maximum Power Dissipation ⁴ (@ $T_a=25^{\circ}C$) for $T_j=150^{\circ}C$		
	SOT23-5 SO8	500 830	mW
ESD	HBM: Human Body Model ⁵ (pins 1, 4, 5, 6, 7 and 8)	2	kV
	HBM: Human Body Model (pins 2 and 3)	0.5	kV
	MM: Machine Model ⁶ (pins 1, 4, 5, 6, 7 and 8)	200	V
	MM: Machine Model (pins 2 and 3)	60	V
	CDM: Charged Device Model (pins 1, 4, 5, 6, 7 and 8)	1.5	kV
	CDM: Charged Device Model (pins 2 and 3)	1.5	kV
	Latch-up Immunity	200	mA

- 1) All voltages values are measured with respect to the ground pin.
- 2) Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
- 3) The magnitude of input and output voltage must never exceed $V_{CC} + 0.3V$.
- 4) Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.
- 5) Human body model, 100pF discharged through a 1.5k Ω resistor into pMin of device.
- 6) This is a minimum Value. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin to pin of device.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage ¹	4.5 to 5.5	V
V_{icm}	Common Mode Input Voltage	- $V_{CC}+1.5V$, + $V_{CC}-1.5V$	V

- 1) Tested in full production at 5V ($\pm 2.5V$) supply voltage.

2 Electrical Characteristics

Table 3: Electrical characteristics for $V_{CC} = \pm 2.5\text{Volts}$, $T_{amb} = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input Offset Voltage Offset Voltage between both inputs	T_{amb}		1.7	6.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		2.1		
ΔV_{io}	V_{io} drift vs. Temperature	$T_{min.} < T_{amb} < T_{max.}$		4		$\mu\text{V}/^\circ\text{C}$
I_{ib+}	Non Inverting Input Bias Current DC current necessary to bias the input +	T_{amb}		3.1	12	μA
		$T_{min.} < T_{amb} < T_{max.}$		3.5		
I_{ib-}	Inverting Input Bias Current DC current necessary to bias the input -	T_{amb}		0.1	5	μA
		$T_{min.} < T_{amb} < T_{max.}$		0.3		
CMR	Common Mode Rejection Ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$\Delta V_{ic} = \pm 1\text{V}$	-57	-61		dB
		$T_{min.} < T_{amb} < T_{max.}$		-59		
SVR	Supply Voltage Rejection Ratio $20 \log (\Delta V_{cc}/\Delta V_{io})$	$\Delta V_{cc} = 3.5\text{V to } 5\text{V}$	-65	-82		dB
		$T_{min.} < T_{amb} < T_{max.}$		-79		
PSR	Power Supply Rejection Ratio $20 \log (\Delta V_{cc}/\Delta V_{out})$	$A_V = +1$, $\Delta V_{cc} = \pm 100\text{mV}$ at 1kHz		-50		dB
		$T_{min.} < T_{amb} < T_{max.}$		46		
I_{CC}	Positive Supply Current DC consumption with no input signal	No load		400	530	μA
Dynamic performance and output characteristics						
R_{OL}	Transimpedance Output Voltage/Input Current Gain in open loop of a CFA. For a VFA, the analog of this feature is the Open Loop Gain (A_{VD})	$R_L = 1\text{k}\Omega$, $V_{out} = \pm 1\text{V}$	0.6	1.45		$\text{M}\Omega$
		$T_{min.} < T_{amb} < T_{max.}$		1.36		$\text{M}\Omega$
BW	-3dB Bandwidth Frequency where the gain is 3dB below the DC gain A_V Note: Gain Bandwidth Product criterion is not applicable for Current-Feedback-Amplifiers	Small Signal $V_{out} = 20\text{mVp-p}$ $R_L = 1\text{k}\Omega$ $A_V = +1$, $R_{fb} = 3\text{k}\Omega$ $A_V = +2$, $R_{fb} = 3\text{k}\Omega$ $A_V = +10$, $R_{fb} = 510\Omega$	80	230 120 26		MHz
		Gain Flatness @ 0.1dB Band of frequency where the gain variation does not exceed 0.1dB	Small Signal $V_{out} = 20\text{mVp-p}$ $A_V = +2$, $R_L = 1\text{k}\Omega$		25	
SR	Slew Rate Maximum output speed of sweep in large signal	$V_{out} = 2\text{Vp-p}$, $A_V = +2$, $R_L = 1\text{k}\Omega$	75	115		$\text{V}/\mu\text{s}$
V_{OH}	High Level Output Voltage	$R_L = 1\text{k}\Omega$	1.55	1.65		V
		$T_{min.} < T_{amb} < T_{max.}$		1.58		
V_{OL}	Low Level Output Voltage	$R_L = 1\text{k}\Omega$		-1.66	-1.55	V
		$T_{min.} < T_{amb} < T_{max.}$		-1.60		

Table 3: Electrical characteristics for $V_{CC} = \pm 2.5\text{Volts}$, $T_{amb} = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{out}	Isink Short-circuit Output current coming in the op-amp. See fig-8 for more details	Output to GND	70	110		mA
		$T_{min.} < T_{amb} < T_{max.}$		100		
	Isource Output current coming out from the op-amp. See fig-11 for more details	Output to GND	60	100		
		$T_{min.} < T_{amb} < T_{max.}$		85		
Noise and distortion						
eN	Equivalent Input Noise Voltage see application note on page 13	F = 100kHz		7.5		nV/ $\sqrt{\text{Hz}}$
iN	Equivalent Input Noise Current (+) see application note on page 13	F = 100kHz		13		pA/ $\sqrt{\text{Hz}}$
	Equivalent Input Noise Current (-) see application note on page 13	F = 100kHz		6		pA/ $\sqrt{\text{Hz}}$
SFDR	Spurious Free Dynamic Range The highest harmonic of the output spectrum when injecting a filtered sine wave	$V_{out} = 2\text{Vp-p}$, $A_V = +2$, $R_L = 1\text{k}\Omega$ F = 1MHz F = 10MHz		-87 -55		dBc dBc

Table 4: Closed-loop gain and feedback components

V_{CC} (V)	Gain	R_{fb} (Ω)	-3dB Bw (MHz)	0.1dB Bw (MHz)
± 2.5	+10	510	26	4
	-10	510	23	4
	+2	3k	120	6
	-2	1.5k	80	10
	+1	3k	210	5
	-1	1.3k	120	60

Figure 1: Frequency Response, positive Gain

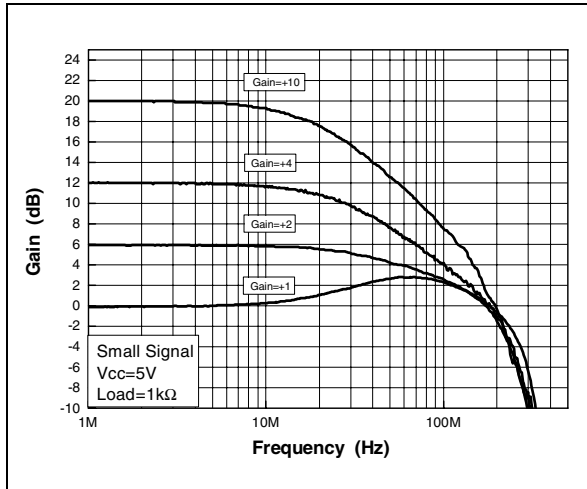


Figure 4: Frequency response, negative gain

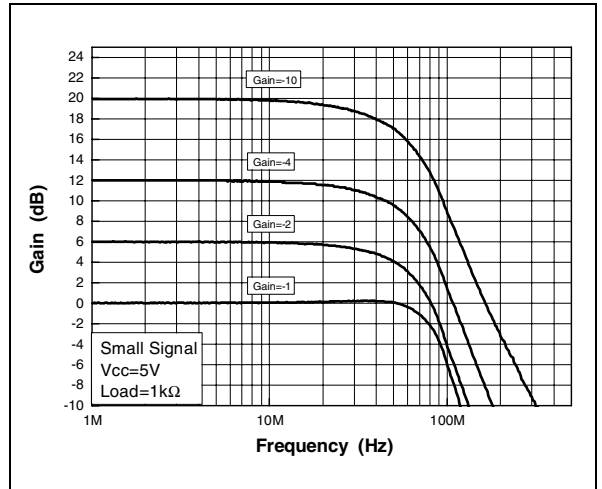


Figure 2: Gain Flatness, gain=+4

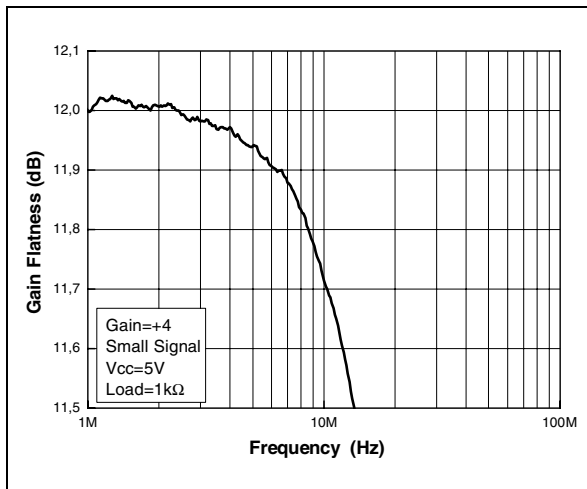


Figure 5: Gain flatness, gain=+2

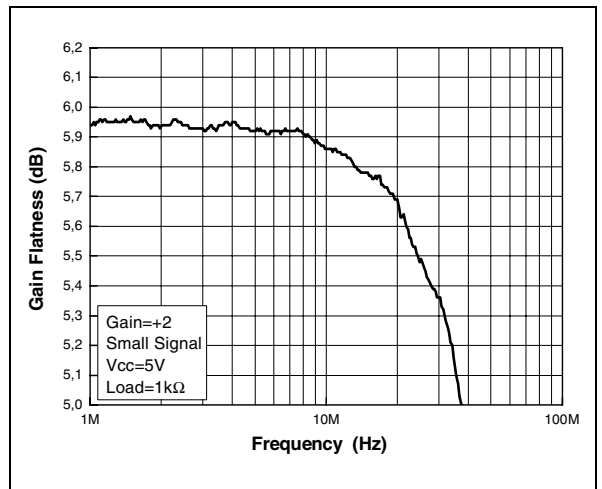


Figure 3: Frequency response vs. capa-load

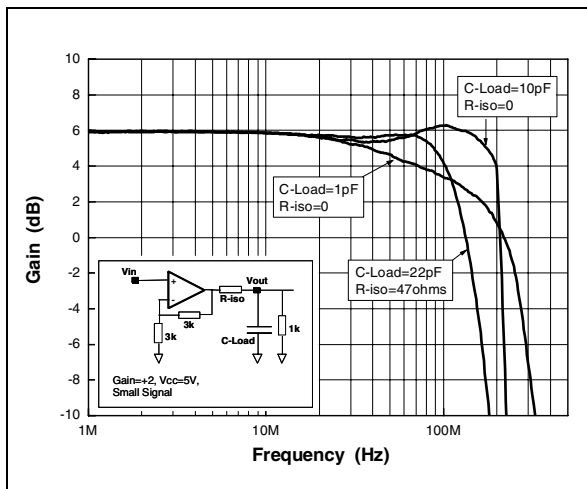


Figure 6: Step response vs. capa-load

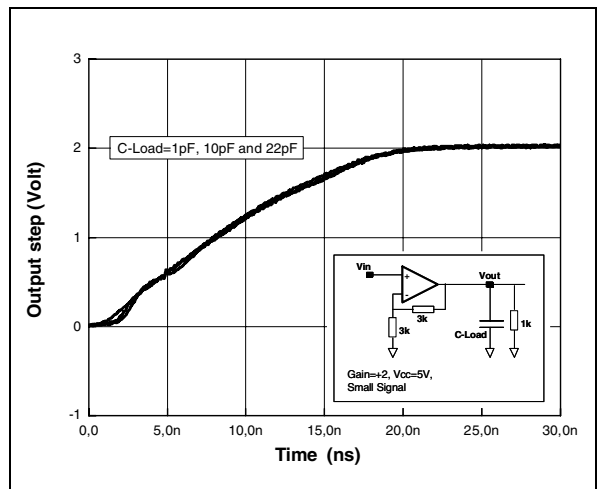


Figure 7: Slew rate

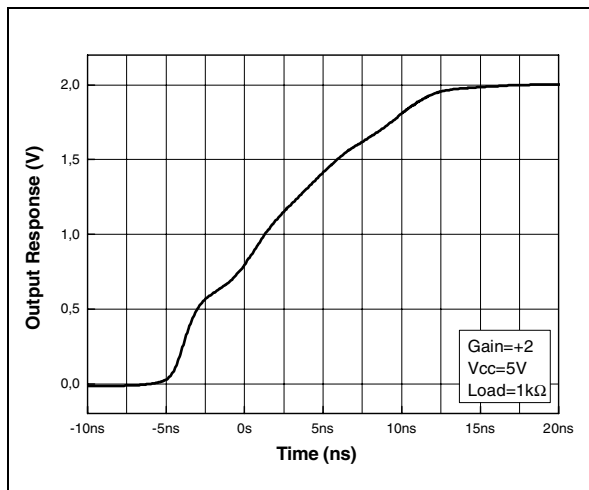


Figure 10: Quiescent current vs. Vcc

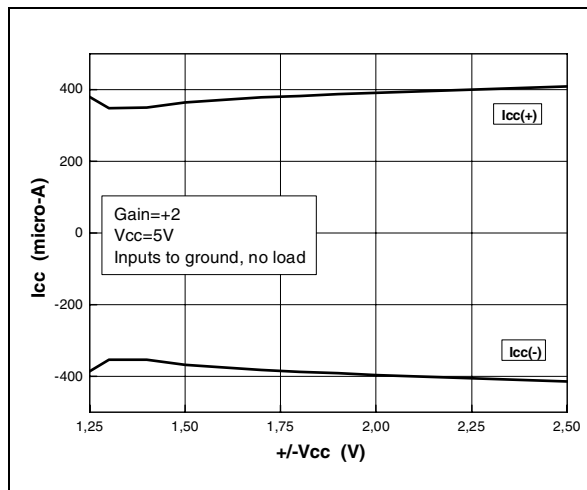


Figure 8: Isink

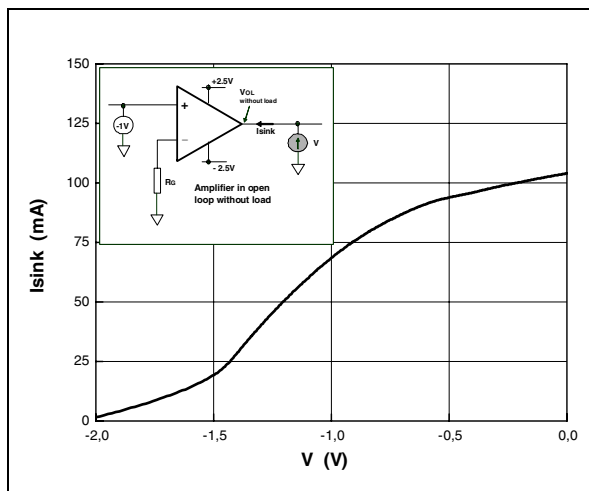


Figure 11: Isource

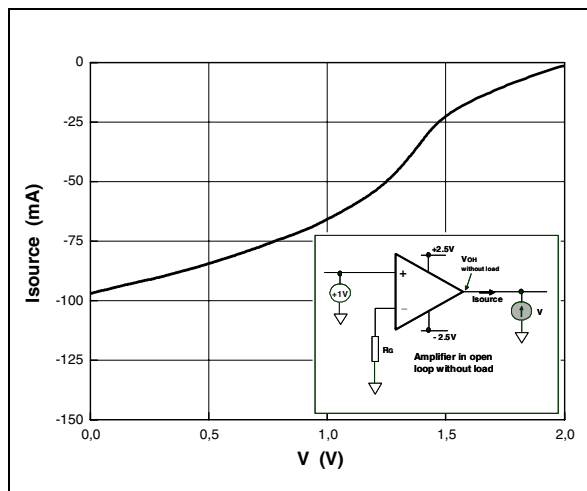


Figure 9: Output amplitude vs. load

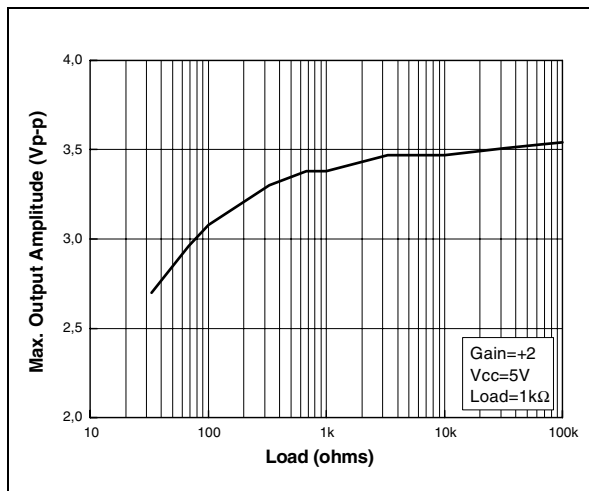


Figure 12: Input voltage noise vs. frequency

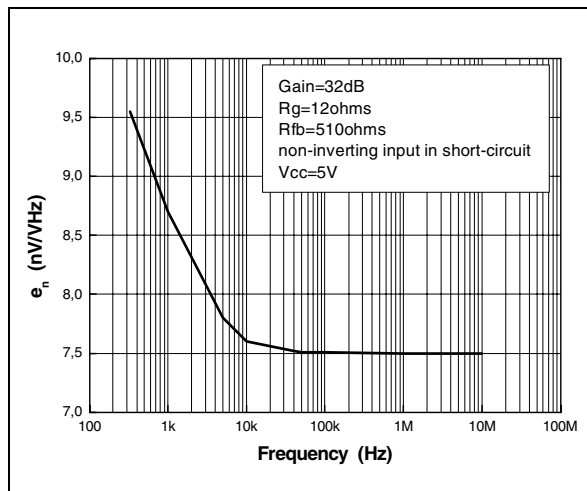


Figure 13: Distortion vs. output amplitude

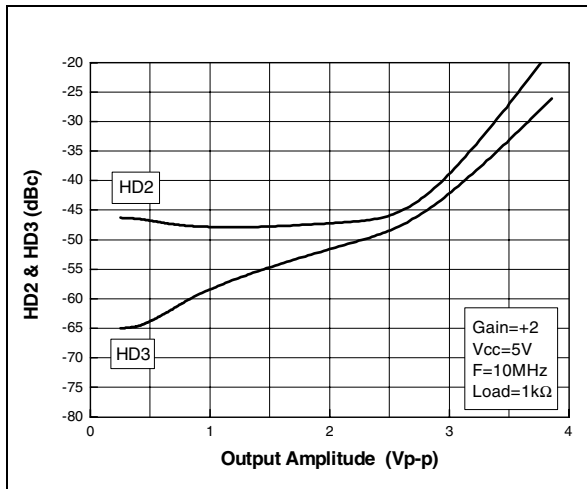


Figure 16: CMR vs. temperature

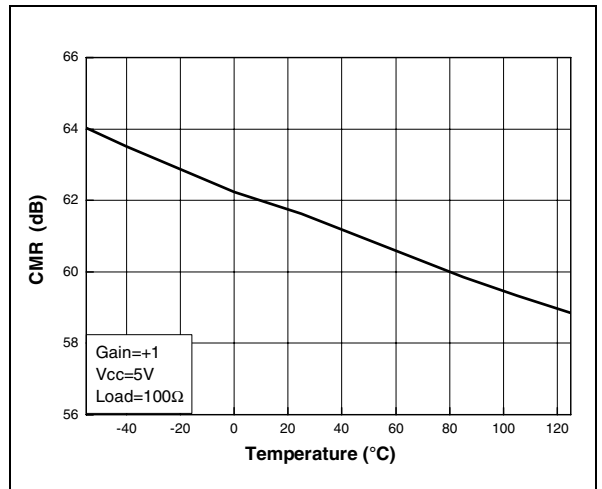


Figure 14: Output amplitude vs. frequency

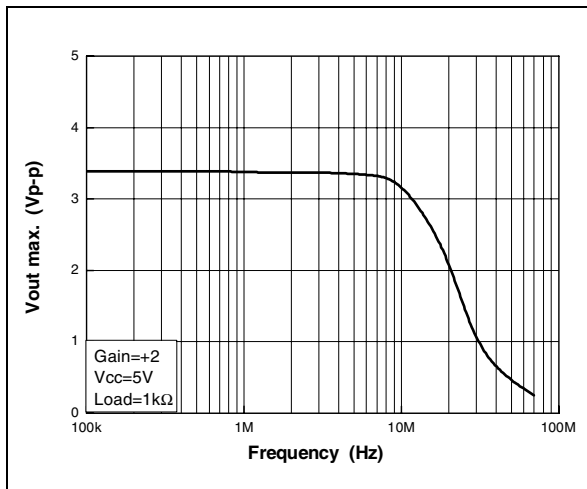


Figure 17: SVR vs. temperature

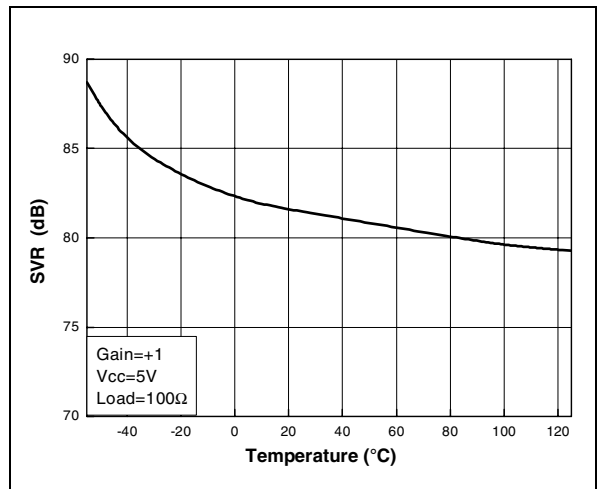


Figure 15: Bandwidth vs. temperature

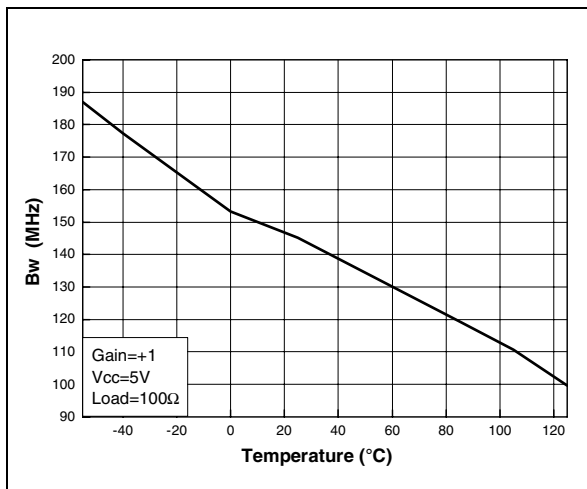


Figure 18: Slew-Rate vs. temperature

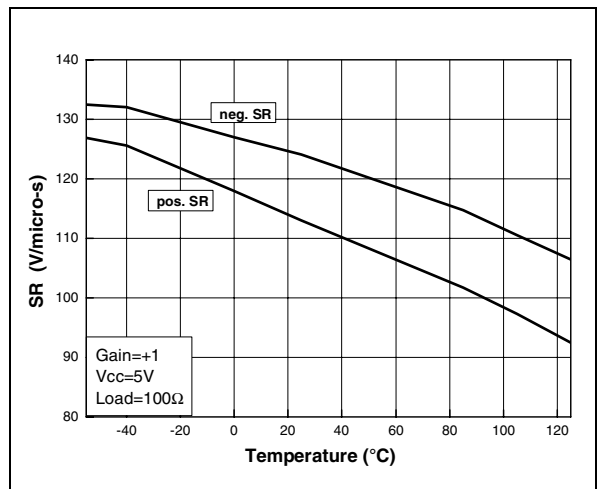


Figure 19: R_{OL} vs. temperature

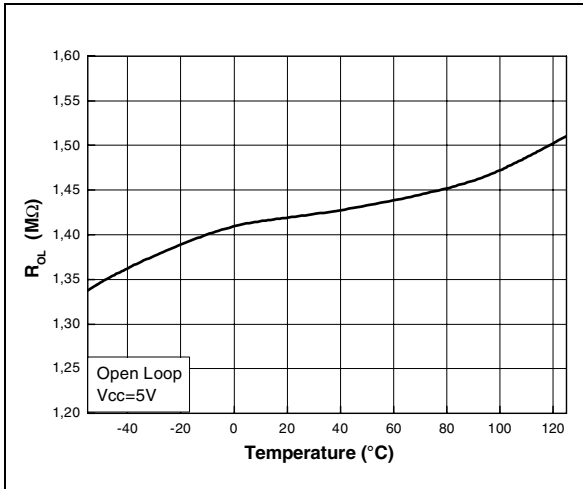


Figure 22: V_{OH} & V_{OL} vs. temperature

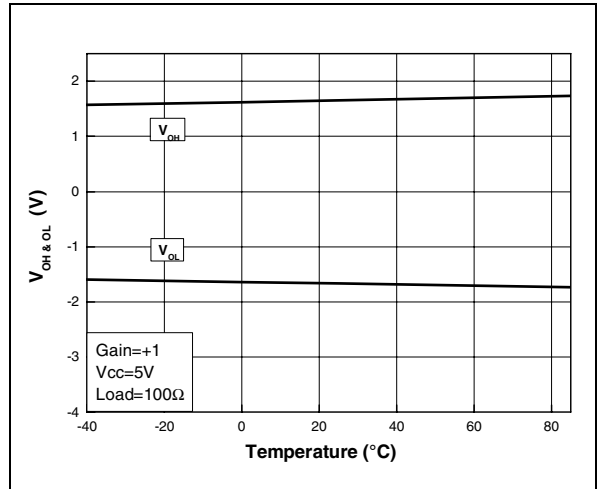


Figure 20: I_{BIAS} vs. temperature

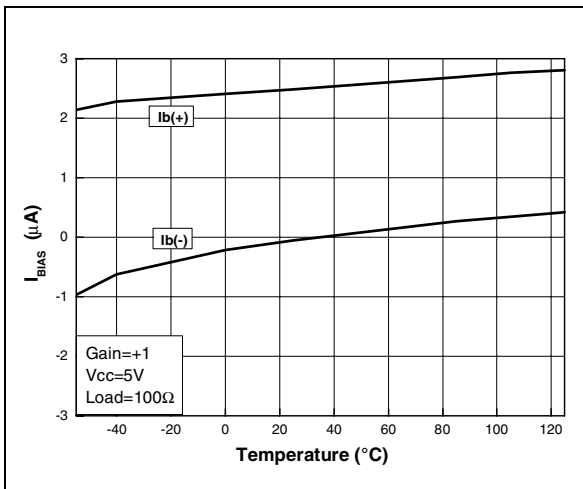


Figure 23: I_{CC} vs. temperature

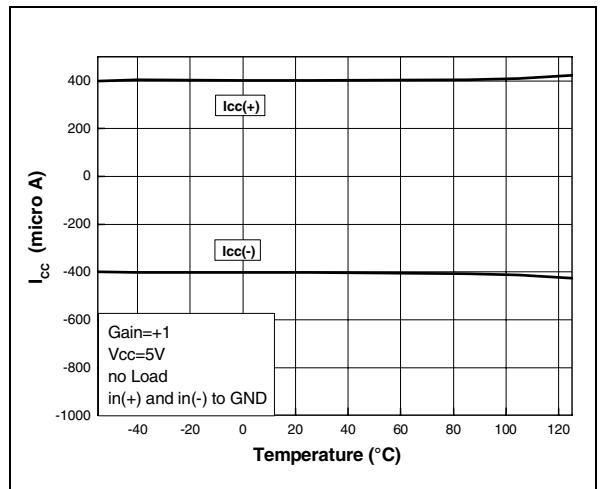


Figure 21: V_{IO} vs. temperature

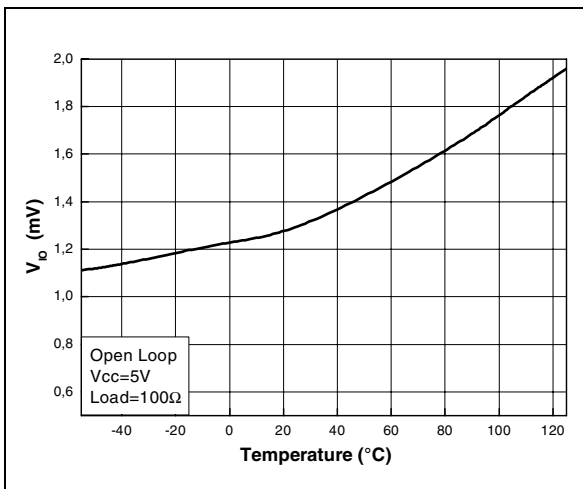
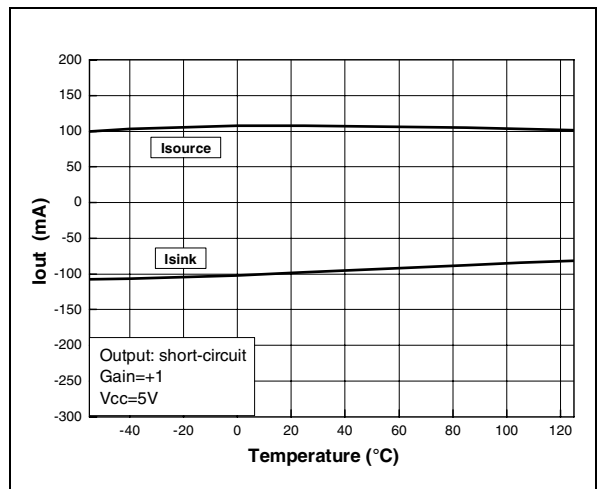


Figure 24: I_{OUT} vs. temperature



3 Evaluation Boards

An evaluation board kit optimized for high-speed operational amplifiers is available (order code: KITHSEVAL/STDL). The kit includes the following evaluation boards, as well as a CD-ROM containing datasheets, articles, application notes and a user manual:

- SOT23_SINGLE_HF BOARD: Board for the evaluation of a single high-speed op-amp in SOT23-5 package.
- SO8_SINGLE_HF: Board for the evaluation of a single high-speed op-amp in SO8 package.
- SO8_DUAL_HF: Board for the evaluation of a dual high-speed op-amp in SO8 package.
- SO8_S_MULTI: Board for the evaluation of a single high-speed op-amp in SO8 package in inverting and non-inverting configuration, dual and single supply.
- SO14_TRIPLE: Board for the evaluation of a triple high-speed op-amp in SO14 package with video application considerations.

Board material:

- 2 layers
- FR4 ($\epsilon_r=4.6$)
- epoxy 1.6mm
- copper thickness: 35 μ m

Figure 25: Evaluation kit for high-speed op-amps

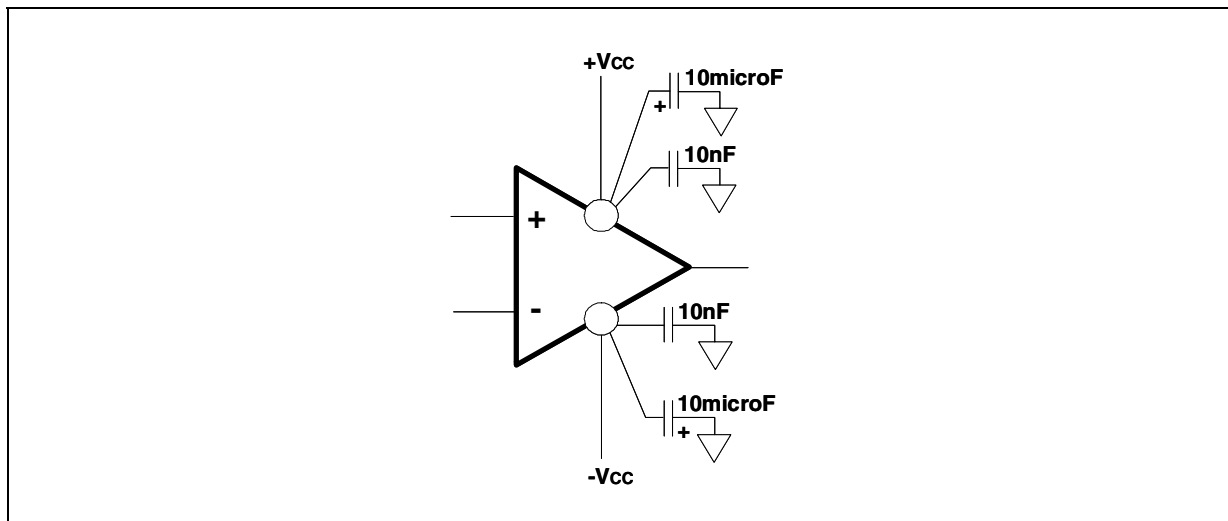


4 Power Supply Considerations

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than $1\mu\text{F}$ is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10nF can be added using the same implementation conditions. Bypass capacitors must be incorporated for both the negative and the positive supply.

For example: on the SO8_SINGLE_HF board, these capacitors are C6, C7, C8, C9.

Figure 26: Circuit for power supply bypassing



Single power supply

In the event that a single supply system is used, new biasing is necessary to assume a positive output dynamic range between 0V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL} , the amplifier will provide an output dynamic from $+0.9\text{V}$ to $+4.1\text{V}$ on $1\text{k}\Omega$ load.

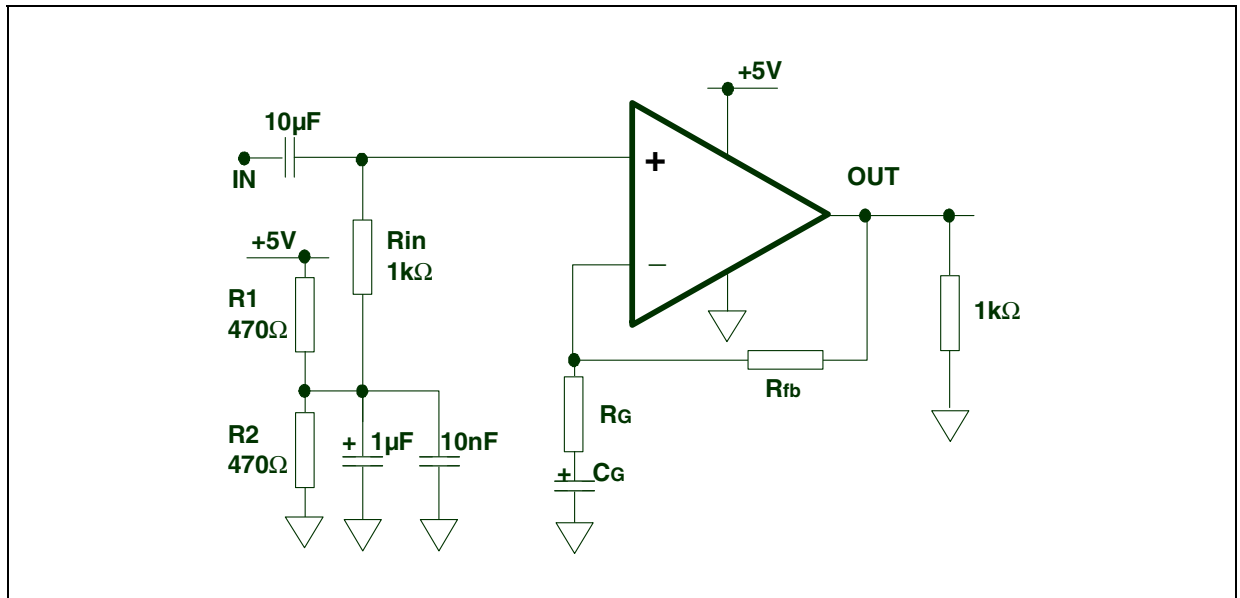
The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current ($55\mu\text{A}$ max.) as the 1% of the current through the resistance divider to keep a stable mid-supply, two resistances of 470Ω can be used.

The input provides a high pass filter with a break frequency below 10Hz which is necessary to remove the original 0V DC component of the input signal, and to fix it at $+V_{CC}/2$.

[Figure 27](#) illustrates a 5V single power supply configuration for the SO8_SINGLE evaluation board (see [Evaluation Boards](#) on page 9).

A capacitor C_G is added in the gain network to ensure a unity gain in low frequency to keep the right DC component at the output. C_G contributes to a high-pass filter with R_{fb}/R_G and its value is calculated with a consideration of the cut-off frequency of this low-pass filter.

Figure 27: Circuit for +5V single supply

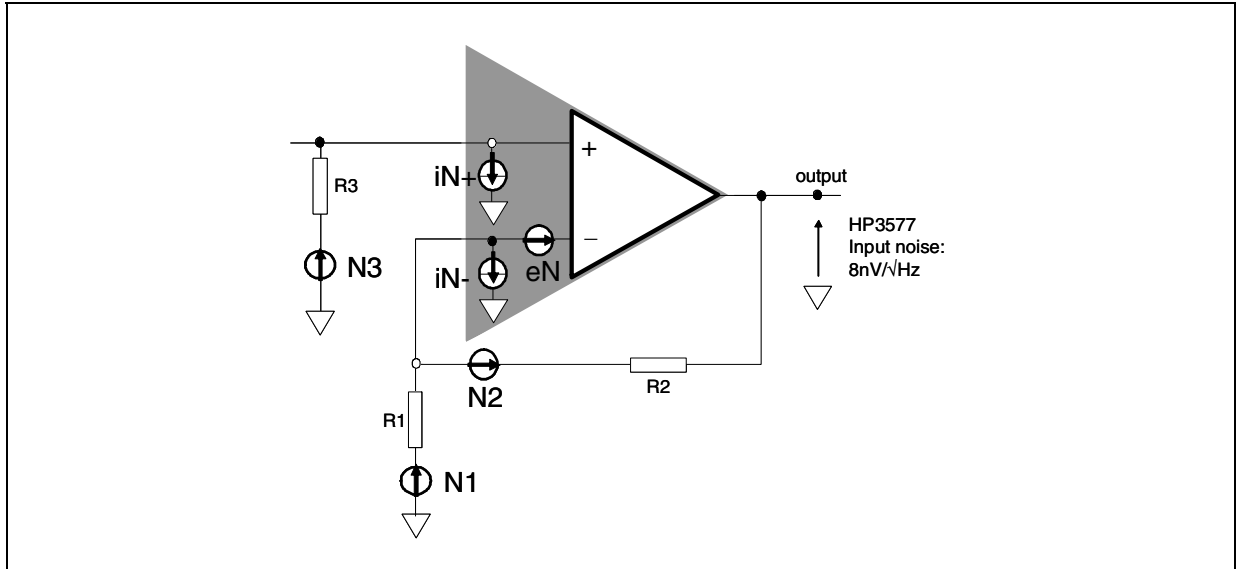


5 Noise Measurements

The noise model is shown in [Figure 28](#), where:

- eN : input voltage noise of the amplifier
- iNn : negative input current noise of the amplifier
- iNp : positive input current noise of the amplifier

Figure 28: Noise model



The thermal noise of a resistance R is:

$$\sqrt{4kTR\Delta F}$$

where ΔF is the specified bandwidth.

On a 1Hz bandwidth the thermal noise is reduced to

$$\sqrt{4kTR}$$

where k is the Boltzmann's constant, equal to $1,374.10^{-23} \text{J}/^\circ\text{K}$. T is the temperature ($^\circ\text{K}$).

The output noise eNo is calculated using the Superposition Theorem. However eNo is not the simple sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in [Equation 1](#):

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2} \quad \text{Equation 1}$$

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3 \quad \text{Equation 2}$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2} \quad \text{Equation 3}$$

The input noise is called the Equivalent Input Noise as it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of [Equation 2](#) we obtain:

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3 \quad \text{Equation 4}$$

Measurement of the input voltage noise eN

If we assume a short-circuit on the non-inverting input ($R3=0$), from [Equation 4](#) we can derive:

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2} \quad \text{Equation 5}$$

In order to easily extract the value of eN , the resistance $R2$ will be chosen to be as low as possible. In the other hand, the gain must be large enough:

$$R3=0, \text{ gain: } g=100$$

Measurement of the negative input current noise iNn

To measure the negative input current noise iNn , we set $R3=0$ and use [Equation 5](#). This time the gain must be lower in order to decrease the thermal noise contribution:

$$R3=0, \text{ gain: } g=10$$

Measurement of the positive input current noise iNp

To extract iNp from [Equation 3](#), a resistance $R3$ is connected to the non-inverting input. The value of $R3$ must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution:

$$R3=100\Omega, \text{ gain: } g=10$$

6 Intermodulation Distortion Product

The non-ideal output of the amplifier can be described by the following series:

$$V_{out} = C_0 + C_1 V_{in} + C_2 V_{in}^2 + \dots + C_n V_{in}^n$$

due to non-linearity in the input-output amplitude transfer, where the input is $V_{in} = A \sin \omega t$, C_0 is the DC component, $C_1(V_{in})$ is the fundamental and C_n is the amplitude of the harmonics of the output signal V_{out} .

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A \sin \omega_1 t + A \sin \omega_2 t$$

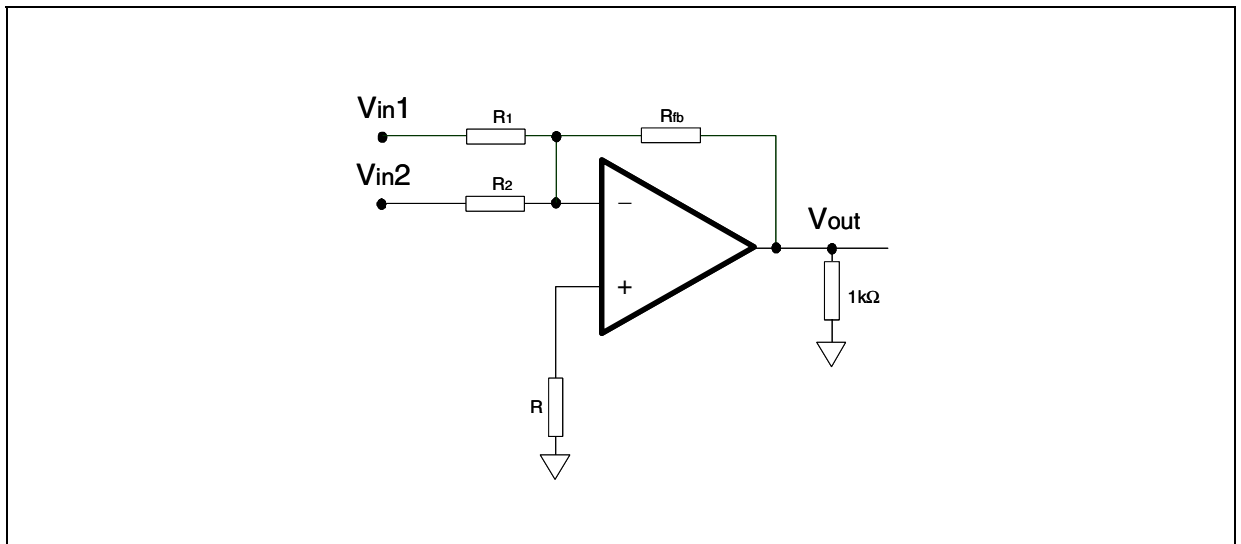
then:

$$V_{out} = C_0 + C_1 (A \sin \omega_1 t + A \sin \omega_2 t) + C_2 (A \sin \omega_1 t + A \sin \omega_2 t)^2 \dots + C_n (A \sin \omega_1 t + A \sin \omega_2 t)^n$$

From this expression, we can extract the distortion terms, and the intermodulation terms form a single sine wave: second-order intermodulation terms IM2 by the frequencies $(\omega_1 - \omega_2)$ and $(\omega_1 + \omega_2)$ with an amplitude of $C_2 A^2$ and third-order intermodulation terms IM3 by the frequencies $(2\omega_1 - \omega_2)$, $(2\omega_1 + \omega_2)$, $(-\omega_1 + 2\omega_2)$ and $(\omega_1 + 2\omega_2)$ with an amplitude of $(3/4)C_3 A^3$.

The measurement of the intermodulation product of the driver is achieved by using the driver as a mixer by a summing amplifier configuration (see [Figure 29](#)). In this way, the non-linearity problem of an external mixing device is avoided.

Figure 29: Inverting summing amplifier (using evaluation board SO8_S_MULTI)



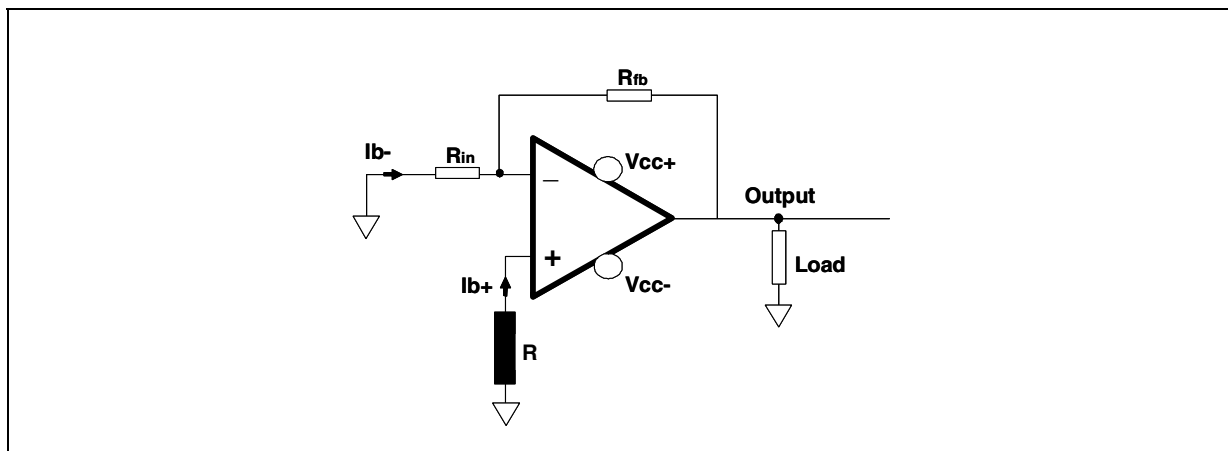
7 The Bias of an Inverting Amplifier

A resistance is necessary to achieve a good input biasing, such as resistance R shown in [Figure 30](#).

The magnitude of this resistance is calculated by assuming the negative and positive input bias current. The aim is to compensate for the offset bias current, which could affect the input offset voltage and the output DC component. Assuming I_{b-} , I_{b+} , R_{in} , R_{fb} and a zero volt output, the resistance R will be:

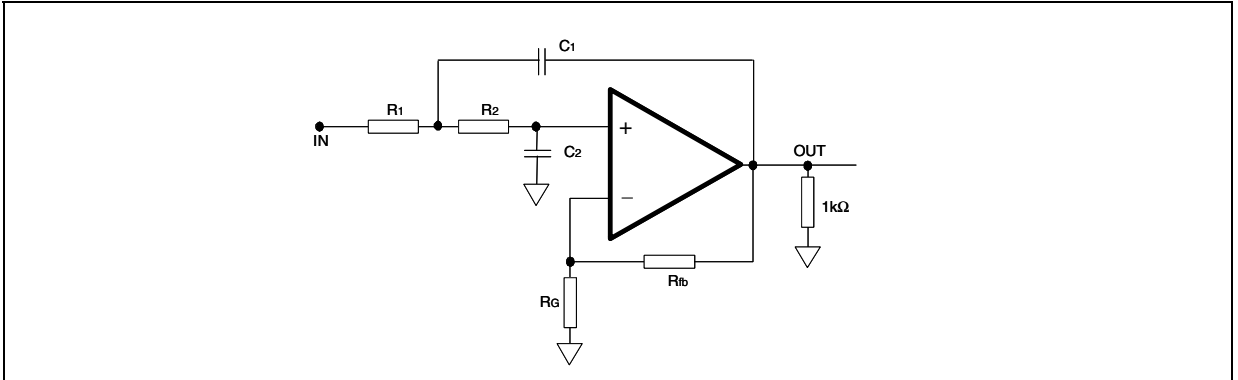
$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

Figure 30: Compensation of the input bias current



8 Active Filtering

Figure 31: Low-pass active filtering, Sallen-Key



From the resistors R_{fb} and R_G we can directly calculate the gain of the filter in a classical non-inverting amplification configuration:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression as the response of the system:

$$T_{j\omega} = \frac{V_{out,j\omega}}{V_{in,j\omega}} = \frac{g}{1 + 2\zeta \frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

The damping factor is calculated by the following expression:

$$\zeta = \frac{1}{2} \omega_c (C_1 R_1 + C_1 R_2 + C_2 R_1 - C_1 R_1 g)$$

The higher the gain, the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use some very stable resistor and capacitor values. In the case of $R_1=R_2=R$:

$$\zeta = \frac{2C_2 - C_1 \frac{R_{fb}}{R_g}}{2\sqrt{C_1 C_2}}$$

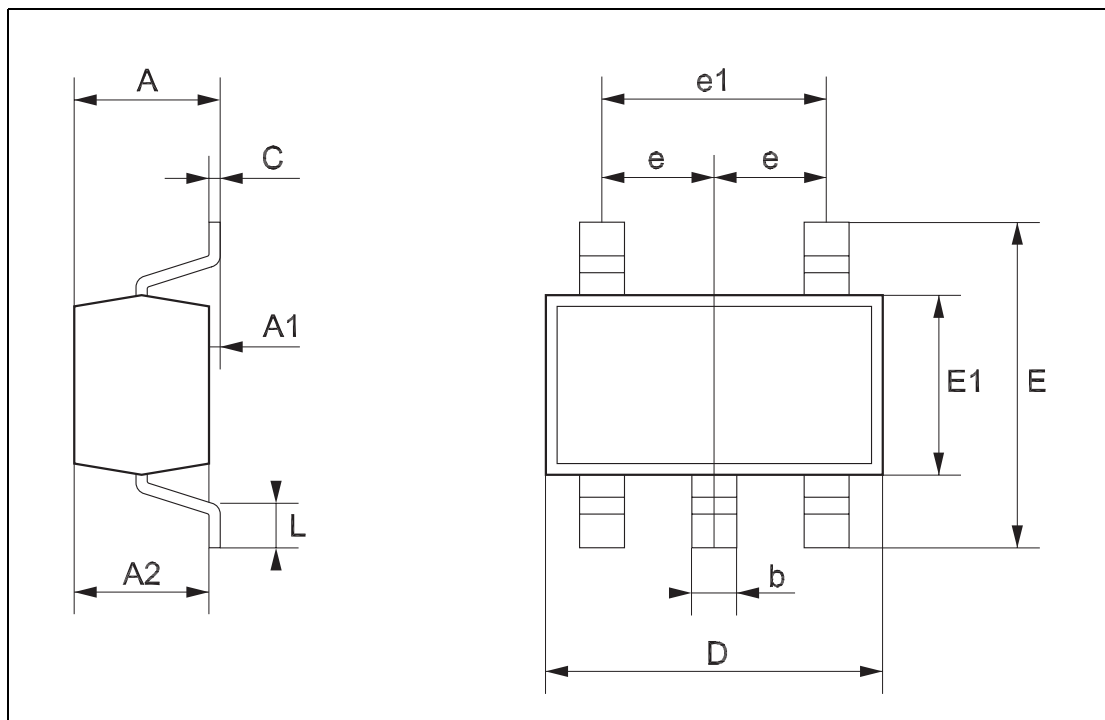
Due to a limited selection of values of capacitors in comparison with resistors, we can fix $C_1=C_2=C$, so that:

$$\zeta = \frac{2R_2 - R_1 \frac{R_{fb}}{R_g}}{2\sqrt{R_1 R_2}}$$

9 Package Mechanical Data

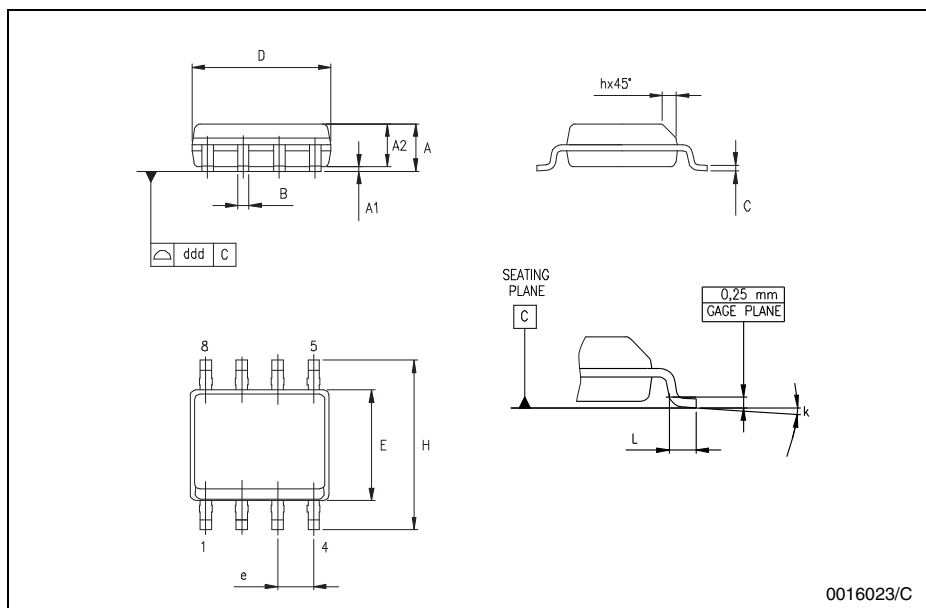
SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	g' (max.)					
ddd			0.1			0.04



10 Revision History

Date	Revision	Description of Changes
01 Oct 2004	1	First release corresponding to Preliminary Data version of datasheet.
December 2004	2	Release of mature product datasheet.

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