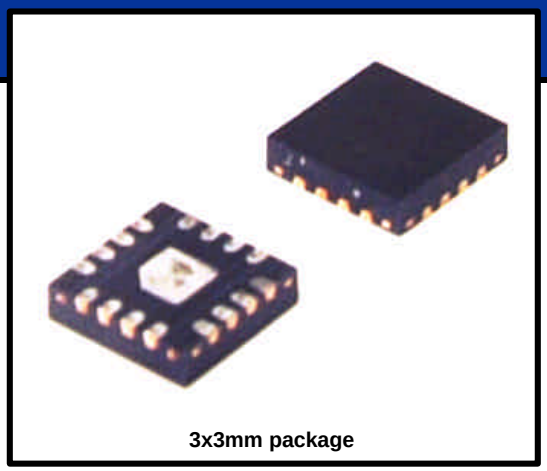
TXC100
300-450MHz
RFIC Transmitter

RF Monolithics, Inc.

Complies with Directive 2002/95/EC (RoHS)



3x3mm package

I. Product Overview

TXC100 is a rugged, single chip OOK/ASK/FSK Transmitter IC in the 300-450 MHz frequency range. This chip is highly integrated and has all required RF functions including a complete PLL circuit and power amplifier, thus requiring very few external components. The TXC100 is feature rich and is very small in size with high output power and low current consumption and is ideal for various short range wireless applications in the industrial, automotive and consumer markets.

II. Key Features

- Operating Frequency Range: 300-450 MHz
- Modulation Types: OOK/ASK/FSK
- Operation supply voltage: 2.1V - 3.6V
- High Date rate:
  - ASK: 100 kbps
  - FSK: 20 kbps
- Low current consumption:
  - ASK mode: 7 mA typical
  - FSK mode: 10 mA typical
- Low Stand by current: < 1 nA
- Adjustable Output power: -10dBm to +10dBm
- Adjustable FSK Shift
- Programmable Clock Output
- Very Low external component count
- Extended temperature range: -40°C to +125°C.
- Small Package: 3X3 mm 16-pin TQFN package
- Standard 13 inch reel, 2500 pieces

III. Popular applications

- Active RFID tags
- Automated Meter reading
- Wireless sensor nodes
- Home Automation
- Security systems
- Tire pressure monitoring
- Remote keyless entry
- Automobile Immobilizers
- Sports & Performance monitoring
- Wireless Toys
- Medical equipment
- Command & Control systems

Electrical Characteristics

Characteristics	Sym	Min	Typical	Max	Units
Operating Frequency	fo	300		450	MHz
Modulation Types			OOK/ASK/ FSK		
ASK Data Rate				100	Kbps
FSK Data Rate				20	Kbps
Peak RF Output Power			10		dBm
Standby Current				1	nA
Supply Voltage Range	V_{DD}	2.1		3.6	Vdc
Operating Temperature	Ta	-40		+125	°C

Crystal Parameters

Characteristics	Sym	Min	Typical	Max	Units
Crystal Frequency	fc		fo/32		MHz
Load Capacitance	Cl			10	pF
Tolerance	Tol		30		ppm

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Dallas, Texas 75244 **(800) 704-6079 toll-free in U.S. and Canada** **www.rfm.com** **Email: info@rfm.com**

IV. TXC100 Block Diagram and Typical Application Circuit

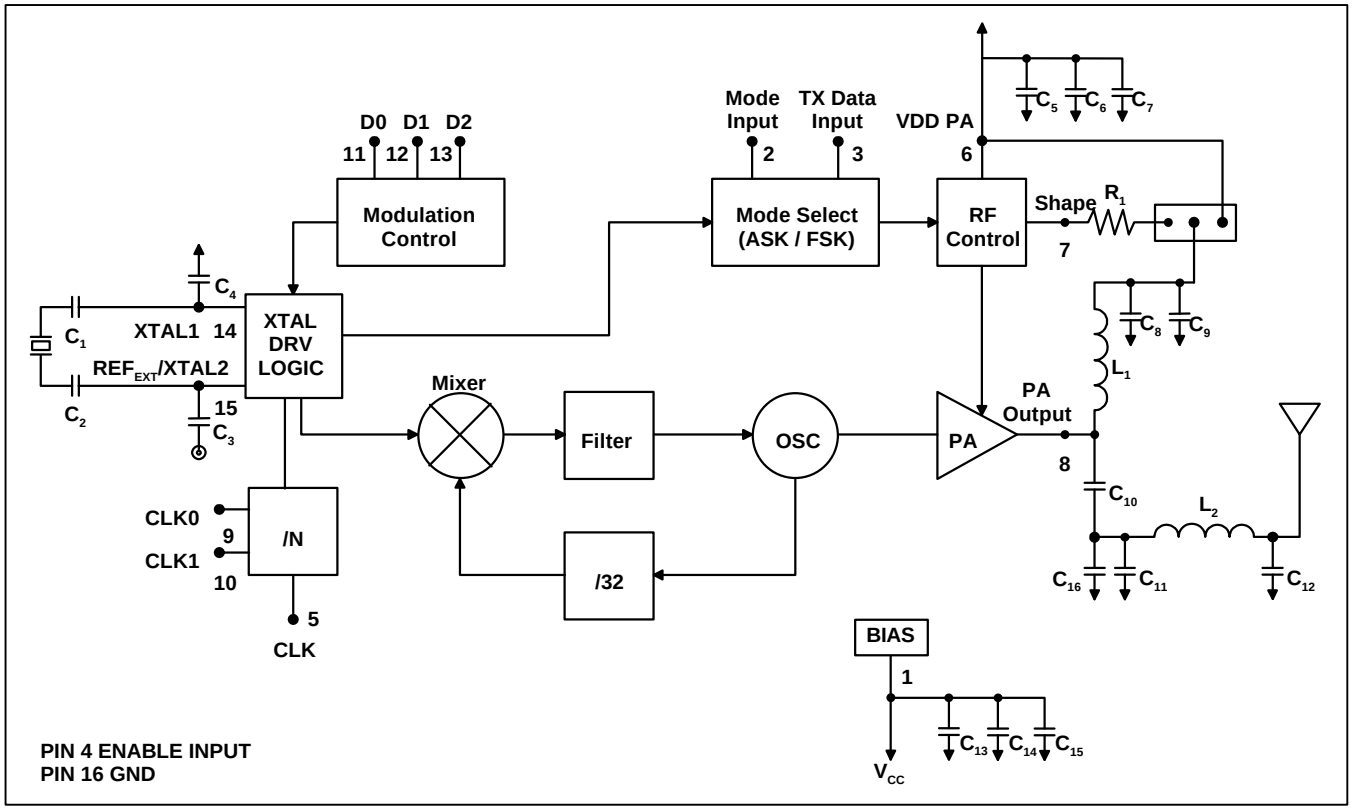
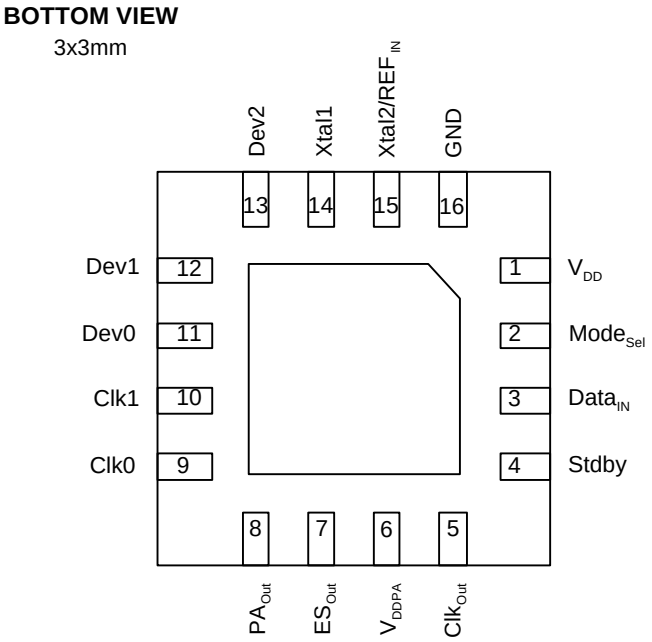


Table 1:
Component Values for Typical Application Circuit

	315MHz Band	433MHz Band
C1	100pF	100pF
C2	100pF	100pF
C3[3]	DNP	DNP
C4[3]	DNP	DNP
C5	1uF	1uF
C6	.01uF	.01uF
C7	220pF	220pF
C8	100pF	100pF
C9	680pF	680pF
C10[1]	15pF	6.8pF
C11[1]	22pF	1pF
C12[1]	15pF	6.8pF
C13	1uF	1uF
C14	.01uF	.01uF
C15	220pF	220pF
C16[1]	2.2pF	1pF
L1[1][2]	27nH	22nH
L2[1][2]	22nH	18nH
X1	9.84375MHz	13.5600MHZ

[1]Matched to 50 Ohms
[2]Use wirewound inductors ONLY
[3]Use for External Reference Input
DNP - Do Not Populate

V. Pin Configuration



VI. Pin Description

Pin	Name	Description
1	V_{DD}	V_{DD} is the supply voltage for the PLL and Logic. Bypass as close as possible to pin with 1µF, .01µF, 220pf.
2	$Mode_{Sel}$	Mode Select enables the chip to be set in ASK or FSK mode Low: ASK mode High: FSK mode **ASK, FSK Mode Selection** The Mode Select pin (2) sets the transmit mode of the device. A logic low sets the mode to ASK modulation. A logic high sets the device to FSK modulation. In ASK mode, data driven onto the $Data_{IN}$ pin (3) gates the internal power amplifier. A data "High" turns the power amplifier on and thus drives the RF signal to the antenna. A data "Low" turns off the power amplifier. In FSK mode, data driven onto the $Data_{IN}$ pin shifts the carrier frequency by the amount programmed through the DEV[2..0] pins (13,12,11). A data "Low" performs no shift. The frequency of a data "Low" in FSK mode is the same frequency of a data "High" in ASK mode. The FSK deviation is achieved by pulling the crystal frequency. See *Crystal Reference* section (pin 15) for more details. The maximum deviation for the 315MHz band and 433MHz band is approximately 55 kHz and 80 kHz, respectively.
3	$Data_{IN}$	Data Input enables the turning on and off of the Power Amplifier in ASK mode and selection of high or low frequency in FSK mode. Low (ASK mode): Power Amplifier off High (ASK mode): Power Amplifier on Low (FSK mode): Low frequency High (FSK mode): High frequency
4	Stdby	Standby enables selection of low power shutdown/standby mode Low or if left unconnected: Sets device in Standby mode High: Sets device in Ready for transmission mode Note: Lowest current consumption achieved when all config pins at Logic Low. **Standby Mode** The Standby pin (4) sets the device in low power shutdown, pulling only 0.2nA. When the device is brought out of standby with a logic "High", it is ready for operation within 200us. The Standby pin has an internal pull-down resistor so this pin can be pulled low or left unconnected. The 200us turn-on time is due to crystal start-up. An optimally matched crystal will minimize this turn-on time. See *Crystal Reference* section (pin 15) for details on crystal load matching.

<table>
<tr>
<td>5</td>
<td>Clk_{Out}</td>
<td>Clock output is a buffered version of the crystal frequency which may be used to drive external logic or a microprocessor. The frequency is programmable thru pins 9 (Clk0) and 10(Clk1) as below:

<table>
<tr><th>Clk0</th><th>Clk1</th><th>Clk_{Out}</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>fc/4</td></tr>
<tr><td>0</td><td>1</td><td>fc/8</td></tr>
<tr><td>1</td><td>1</td><td>fc/16</td></tr>
</table>

NB: fc = (Crystal Frequency)</td>
</tr>
<tr>
<td>6</td>
<td>V_{DDPA}</td>
<td>Supply voltage for the Power amp.
Bypass as close as possible to the pin with a .01µF and 220pf capacitor.</td>
</tr>
<tr>
<td>7</td>
<td>ES_{Out}</td>
<td>Envelope-Shaping Output controls the on/off ramp time of the power amp in ASK mode. This reduces the spectral width of the output signal when modulated. Placing a small resistor in series with the output, as close as possible to the chip to minimize circuit parasitics, will enable control of output power. A potentiometer may be used to adjust the output power to the desired level. Bypass as close to the pin as possible with a 680pF and 220pF capacitor.

Note: By using the ES_{OUT} pin there is approx a 0.6dB drop in max output power.

Spectral Shaping/Output Power Adjust
The ES_{OUT} pin (7) can serve a dual function. Use of the ES_{OUT} pin will allow for a softer turn-on/turn-off of the power amplifier resulting in reduced spectral spreading of the ASK signal. Inserting a series resistor between the ES_{OUT} pin and the pull-up inductor will allow for adjustment of the carrier output power. Typically a resistance of 5K Ohms or less will allow adjustment down to -10dBm.</td>
</tr>
<tr>
<td>8</td>
<td>PA_{Out}</td>
<td>The envelope-shaping resistor allows for a turn on / turn-off of the Power Amp in ASK mode.
Power-Amplifier Output. - Requires a DC path to the supply voltage, thru a series inductor which can be part of the output matching network to an antenna

Power Amplifier
The power amp is an open-drain, Class C amplifier with optimal impedance at PA_{OUT} (pin 8) of about 250 Ohms. A matching network can optimize the output to drive typical 50 Ohm antennas. An output matching network with component values is shown in the Typical Application Circuit (section IV). Additionally, the matching network aids in suppressing carrier harmonics to aid in compliance testing.</td>
</tr>
<tr>
<td>10, 9</td>
<td>Clk[1..0]</td>
<td>See description for Pin 5</td>
</tr>
<tr>
<td>13, 12, 11</td>
<td>FreqDev[2..0]</td>
<td>Frequency Deviation configuration pins set the amount of deviation desired between data logic states in FSK mode. Frequency deviation is programmable through pins 13, 12, 11 as below:

<table>
<tr><th>DEV D</th><th>DEV 2</th><th>DEV 1</th><th>DEV 0</th></tr>
<tr><td>.125 x max</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>.250 x max</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>.375 x max</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>.500 x max</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>.625 x max</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>.750 x max</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>.875 x max</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>max</td><td>1</td><td>1</td><td>1</td></tr>
</table>

Note: Deviation values are approx for properly loaded crystal. Crystal characteristics and loading will differ with other manufacturers.</td>
</tr>
<tr>
<td>14</td>
<td>Xtal1</td>
<td>External Crystal input 1 presents a capacitance of 3pF to GND in ASK and FSK($Data_{IN}$=0V) mode. Additional circuit parasitics add to the package capacitance which increases the presented load to about 4.5pF.</td>
</tr>
<tr>
<td>15</td>
<td>$Xtal2/REF_{IN}$</td>
<td>External Crystal input 2 presents a capacitance of 3pF to GND in ASK and FSK($Data_{IN}$=0V) mode. Additional circuit parasitics add to the package capacitance which increases the presented load to about 4.5pF.

External Ref Input enables a custom frequency to be applied to obtain the desired transmit frequency. Unconnected Xtal1 input must be bypassed with a .01µF capacitor and additional .01µF series capacitance should be added into External Reference input.

Crystal Reference
The crystal drive circuit in the TXC100 is designed to present a 3pF load to GND to the reference crystal. Including PCB parasitic capacitances, this increases to about 4.5pF. In ASK mode, the full 3pF load is applied to the crystal allowing it to oscillate at the desired frequency. In FSK mode, a portion of the 3pF load is removed in response to a data logic “High” applied to the $Data_{IN}$ (pin 2) and the programmed frequency deviation pins DEV[0..2] (13,12,11). For larger frequency deviations use a crystal with larger motional capacitance or reduce PCB parasitic capacitance as much as possible.

NOTE: Use a crystal with the same load capacitance as that presented by the TXC100. If not, additional matching will be necessary to achieve the desired carrier frequency and the added matching will reduce the desired FSK deviation.</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>Ground. Connect to system ground.

Note: The exposed ground pad is the power amp ground. It must be connected to system ground thru a low inductance path.</td>
</tr>
</table>

VII. Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		Min	Max	
Operating Temperature	T_O	-40	+125	°C
Junction Temperature	T_J	-40	+150	°C
Storage Temperature	T_S	-60	+150	°C
Supply Voltage – Vdd to GND	V_S	-0.3	+4	V
All pins to GND		-0.3	Vdd + 0.3	V
Note: Maximum ratings must not be exceeded under any circumstances and can cause permanent damage to the IC				

VIII. DC Electrical Characteristic

(Typical values taken at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted)

Characteristic	Sym	Notes	Limit Values			Unit	Test Conditions	
			min	typ	max			
Supply Voltage	V_{DD}		2.1		3.6	V		
Current Consumption								
Standby	I_{STDBY}			0.2	1	nA	T_A = +25 deg C	
				120	300		T_A = +85 deg C	
				700	1600		T_A = +125 deg C	
Supply	I_{DD}	1,4		2.9	4.3	mA	PA off, Data=0V (ASK)	315 Mhz Band
				7	10.7		50% duty cycle (ASK)	
				10.5	17.1		Data=+V_{DD} (FSK and ASK)	
				3.3	4.8		PA off, Data=0V (ASK)	433 Mhz Band
				7.3	11.4		50% duty cycle (ASK)	
				10	18.1		Data=+V_{DD} (FSK and ASK)	
Digital Inputs								
Data Input Low	V_{IL}				0.25	V		
Data Input High	V_{IH}		V_{DD}-0.25			V		
Max Input Current	I_I			15.5	20	µa		
Digital Outputs								
Output Voltage Low	V_{OL}				0.25	V	Clkout, Load = 10pF	
Output Voltage High	V_{OH}		V_{DD}-0.25			V	Clkout, Load = 10pF	

IX. AC Electrical Characteristic

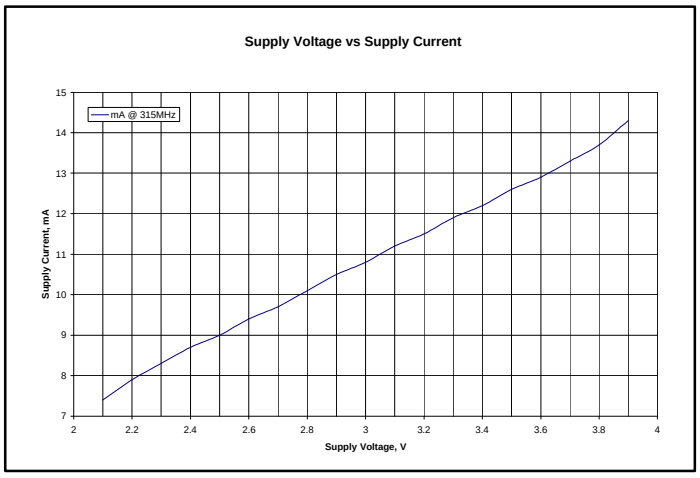
(Typical values taken at V_{DD} = +3.0V, T_A = +25°C, unless otherwise noted)

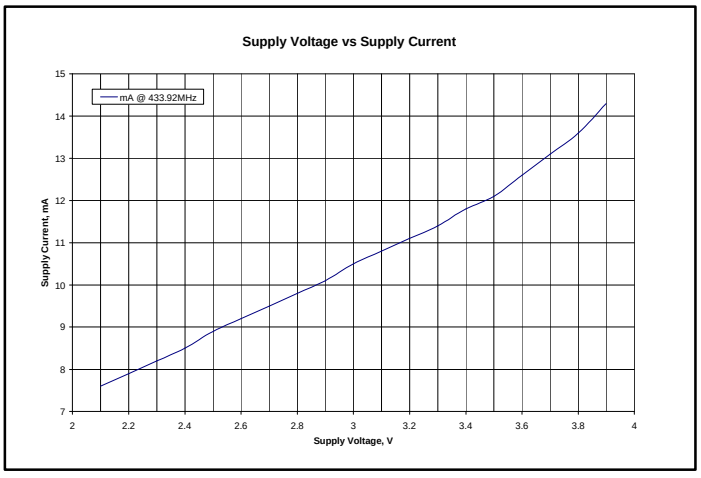
Parameter	Sym	Notes	Limit Values			Unit	Test Conditions	
			min	typ	max			
PLL Performance								
VCO Gain	K_{VCO}			280		MHz/V		
Phase Noise				-75		dBc/Hz	315 Mhz Band	Freq Offset = 100kHz
				-74			433 Mhz Band	
				-98			315 Mhz Band	Freq Offset = 1MHz
				-98			433 Mhz Band	
Loop BW	BW			300		kHz		
Reference Spur				-40		dBc		
2nd Harmonic				-56		dBc	315 Mhz Band	
				-52			433 Mhz Band	
3rd Harmonic				-56		dBc	315 Mhz Band	
				-65			433 Mhz Band	
Crystal								
Frequency Range	f_{REF}			f_{RF}/32		MHz	fundamental mode, AT	
Tolerance		3		50		ppm		
Internal Load Capacitance		2		3		pF		
Clock Output Frequency	CLK_{OUT}			F_{XTAL}/N		MHz	Determined by CLK1 and CLK2	
System Characteristics								
Frequency Range			300		450	MHz		
Output Power		4		12.2	16.1	dBm	TA = -40C, V_{DD} = +3.6V	into 50Ω matched load
			6.1	10	12.4		TA = +25C, VDD = +3.0V	
			2.7	5.3			TA = +125C, VDD = +2.1V	
Start-up time	t_{ON}	5		160		µs	STDBY to Tx	
Rise Time	tr	5		300		ns		
Max Data Rate		5		20		kbps	FSK (50% Duty Cycle)	
				100			ASK (50% Duty Cycle)	
Frequency Deviation (FSK)				55		kHz	315 Mhz Band	DEV[2..0]=111
				80			433 Mhz Band	
Transmit Efficiency $\eta=P_{OUT}/(V_{DD}xI_{DD})$		4		35		%	315 Mhz Band	CW
				31			433 Mhz Band	
				27			315 Mhz Band	50% duty cycle
				25			433 Mhz Band	
Power ON/OFF Ratio				-77		dB	ASK Mode	
Frequency Stability vs. V_{DD}	Δdf_{VDD}			4		kHz		
Frequency Stability vs. Temp	Δdf_{TA}			TBD		kHz	-40°C to +85°C	

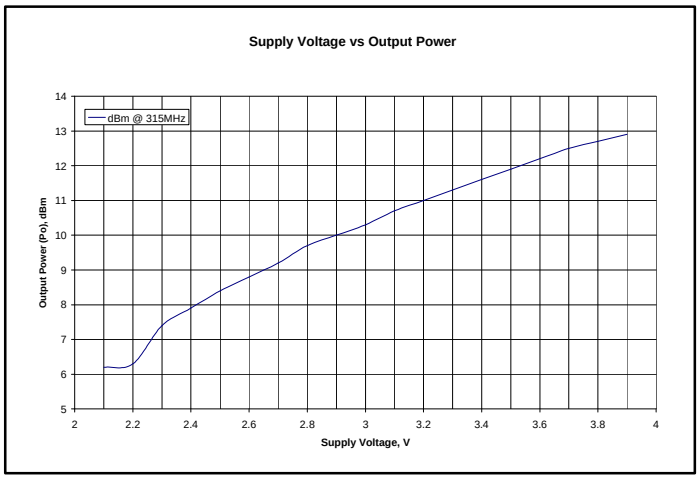
Notes:

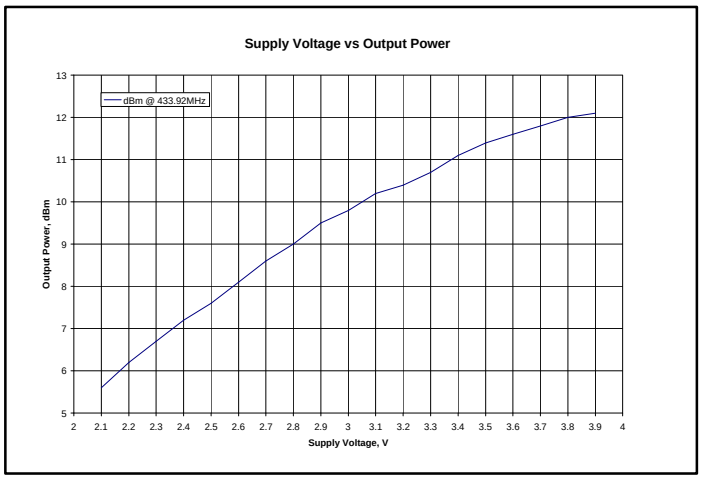
1. 10kHz, 50% duty cycle
2. Dependent on PCB parasitic trace capacitance and crystal parameters.
3. Dependent on crystal parameters.
4. Transmit Efficiency, RF Output Power, and Supply Current are heavily dependent on proper output matching and PCB layout.
5. No Envelope Shaping.

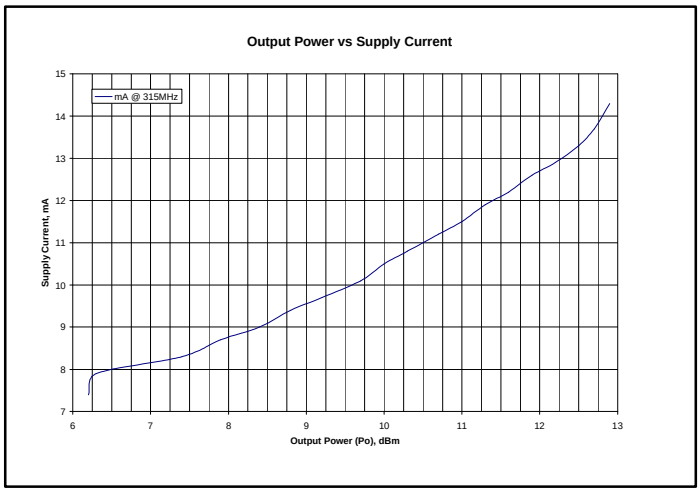
X. Typical Operating Characteristics

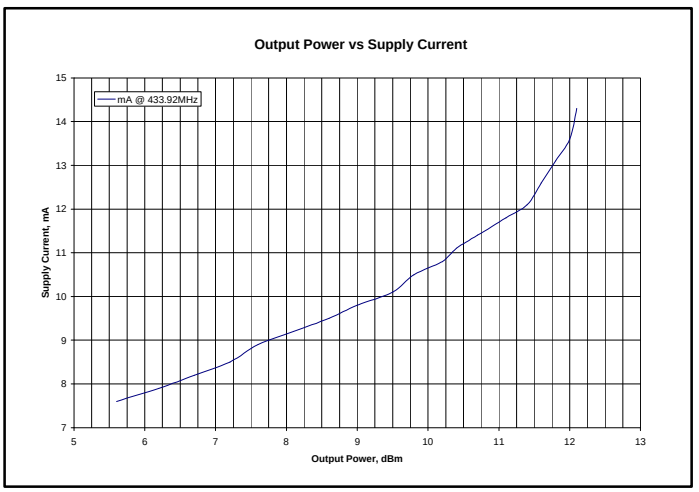


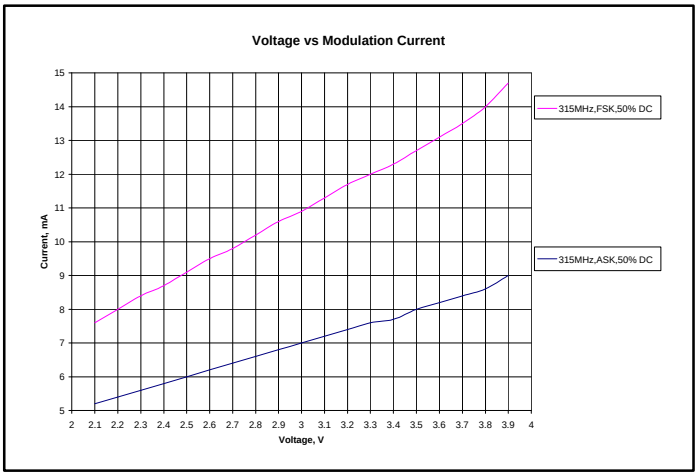


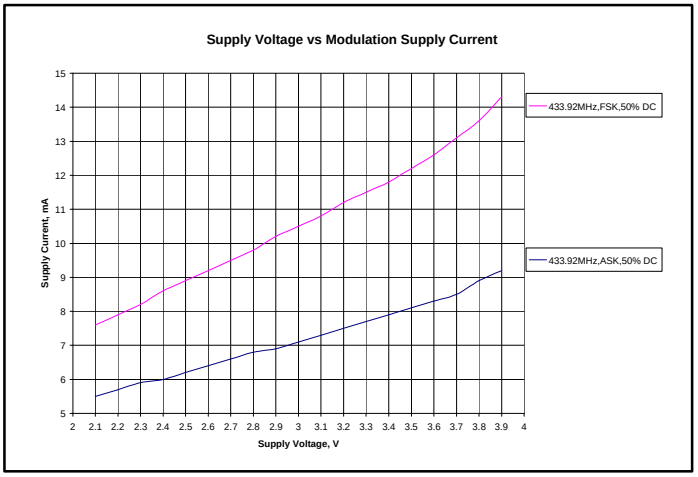


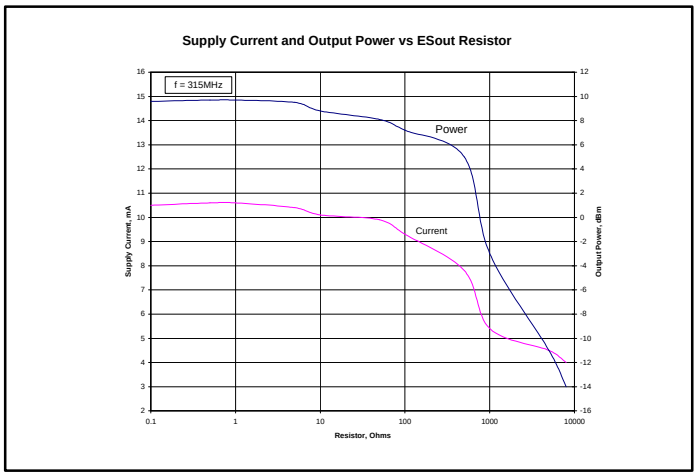


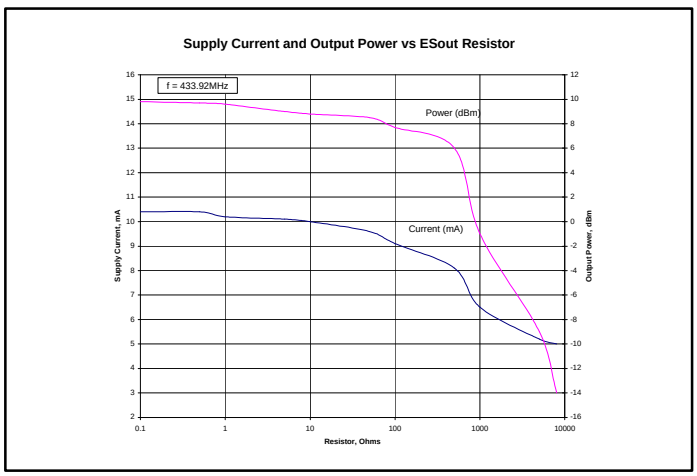





Voltage vs Modulation Current
Current, mA
Voltage, V
315MHz,FSK,50% DC
315MHz,ASK,50% DC


Supply Voltage vs Modulation Supply Current
Supply Current, mA
Supply Voltage, V
433.92MHz,FSK,50% DC
433.92MHz,ASK,50% DC


Supply Current and Output Power vs ESout Resistor
f = 315MHz
Power
Current
Supply Current, mA
Output Power, dBm
Resistor, Ohms


Supply Current and Output Power vs ESout Resistor
f = 433.92MHz
Power (dBm)
Current (mA)
Supply Current, mA
Output Power, dBm
Resistor, Ohms

XI. Theory of Operation

Introduction

The TXC100 is a crystal-referenced transmitter designed to operate in the 315/433 MHz frequency spectrum. The carrier and crystal reference relation is given by:

$$f_C = f_{XTAL} * 32$$

It is capable of supporting OOK/ ASK and FSK data transmissions at 100kbps and 20kbps, respectively. The output power is adjustable from -10dBm to +10dBm thru a resistor at the ES_{OUT} (pin 7). The FSK frequency deviation is programmable with up to eight different deviation values. The IC also provides a buffered clock output of the reference crystal for use by an external processor. The clock output is also programmable.

Frequency Synthesizer

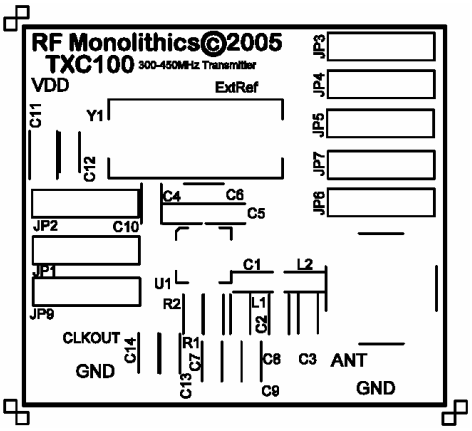
The frequency synthesizer is simply a Phase Locked Loop circuit with a loop bandwidth of 300 kHz. The PLL contains a phase detector, charge pump, VCO, integrated loop filter, ÷32 clock divider, and crystal oscillator drive circuit. The internal PLL is self contained and requires no external components for filtering or dividing. Only a reference crystal is needed.

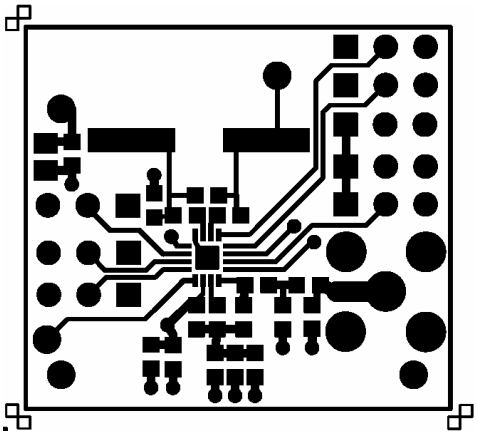
50Ω Output Matching

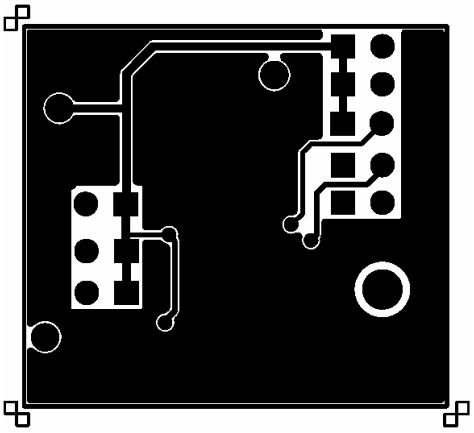
When properly matched, the TXC100 can output up to +12 dBm into a 50Ω load. The output is an open-drain configuration which requires a pull-up inductor for proper internal biasing. The pull-up inductance serves to provide biasing for the power amplifier and is a high frequency choke to reduce unwanted coupling back into the power supply. Maximum power transfer occurs when the output is closely matched to 250Ω. For best performance use wirewound inductors instead of chip inductors. Wirewound inductors provide lower insertion loss as opposed to chip inductors. See *Typical Application Circuit* (section IV) for topology and matching component values.

PCB Layout Considerations

PCB layout is critical to proper and consistent operation. Always use controlled impedance lines from the PA_{OUT} (pin 8). For a .062" thick FR4 board a 50Ω impedance line is approximately .110" wide. Component spacing is critical as well. Keep all output matching components as close together as possible to minimize stray inductance and capacitance that can detune the matching network. Keep ground planes at least a board thickness away from the signal output leading to the antenna or RF connector.





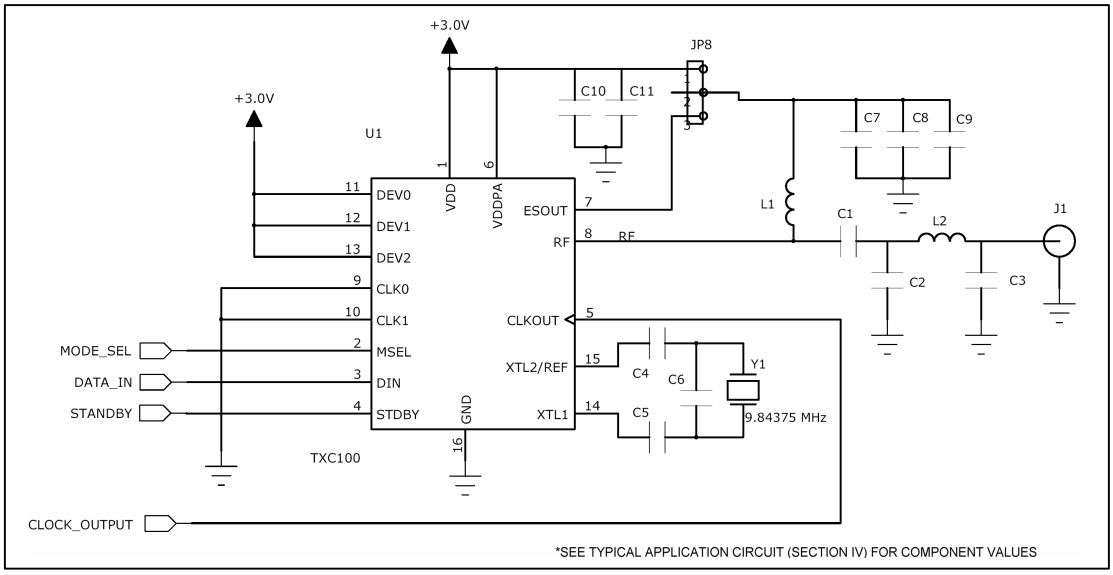


Antenna Layout Considerations

Most compact wireless designs have the need for a small, compact antenna. Typically, loop antennas are the ones of choice since they can be designed into tight spaces. Loop antenna design can become fairly lengthy and detailed discussion is beyond the scope of this datasheet. The object here is to provide a “rule of thumb” approach to achieve an appropriate starting point. Empirical data will provide the best path to take.

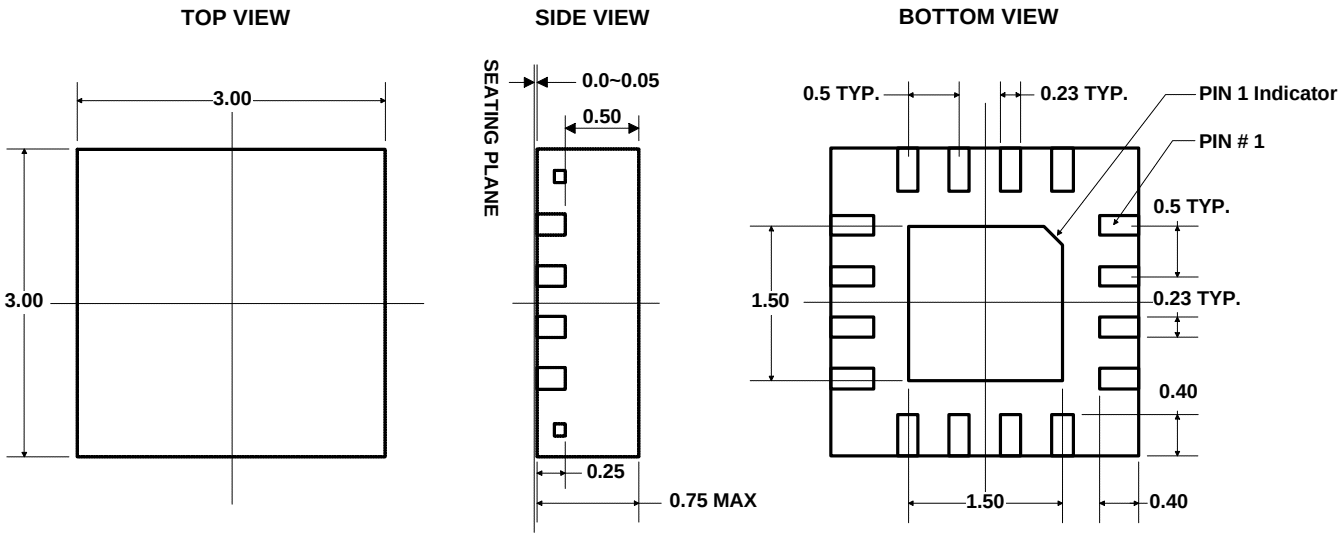
The circumference of the antenna should be less than λ/4 so that the antenna appears inductive. For this, a series matching capacitor is used to tune out the inductance of the antenna, since the antenna appears inductive. The capacitor may be located at the feed point of the antenna or at the “grounded” end. The capacitor may be a variable type or several fixed values may be attempted until an optimal match is reached. The use of a good network analyzer is essential for proper matching and maximum power transfer. For additional information on antenna design see the Application Notes section of our website: http://www.rfm.com/corp/apnotes.htm.

XII. Typical Test Circuit



Package Dimensions – 3x3mm 16-pin TQFN Package

(all values in mm)



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