DATA SHEET

TZA3043; TZA3043B
Gigabit Ethernet/Fibre Channel transimpedance amplifier

Product specification
Supersedes data of 1998 Jul 08
File under Integrated Circuits, IC19

2000 Mar 28

Philips Semiconductors

PHILIPS

FEATURES

- Wide dynamic range, typically 2.5 μA to 1.5 mA
- Low equivalent input noise, typically 5.7 pA/√Hz
- Differential transimpedance of 8.3 kΩ
- Wide bandwidth from DC to 950 MHz
- Differential outputs
- On-chip Automatic Gain Control (AGC)
- No external components required
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode
- Pin compatible with TZA3023 and SA5223
- Switched output polarity available (B-version).

APPLICATIONS

- Digital fibre optic receiver in medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

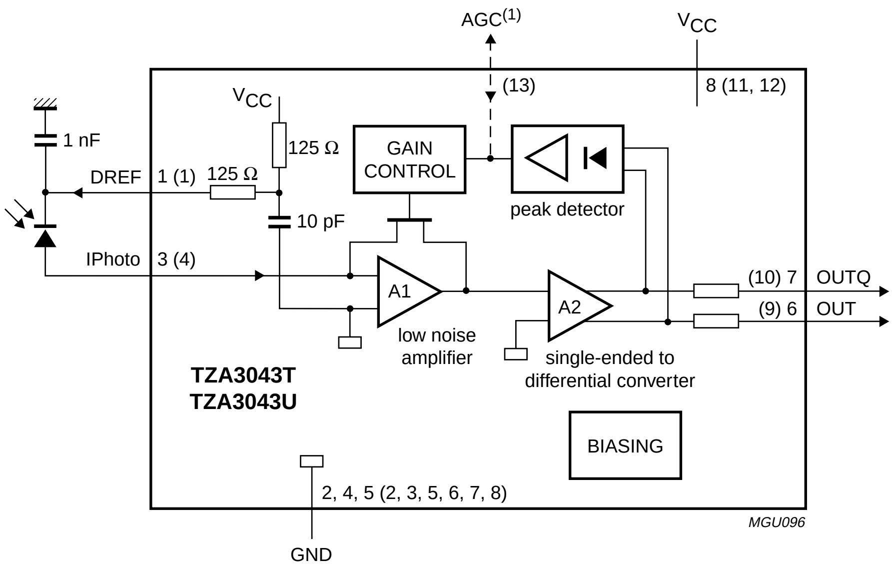
GENERAL DESCRIPTION

The TZA3043 is a high speed transimpedance amplifier with AGC designed to be used in Gigabit Ethernet/Fibre Channel optical links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3043T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3043U	–	bare die in waffle pack carriers; die dimensions 1.030 × 1.300 mm	–
TZA3043BT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3043BU	–	bare die in waffle pack carriers; die dimensions 1.030 × 1.300 mm	–

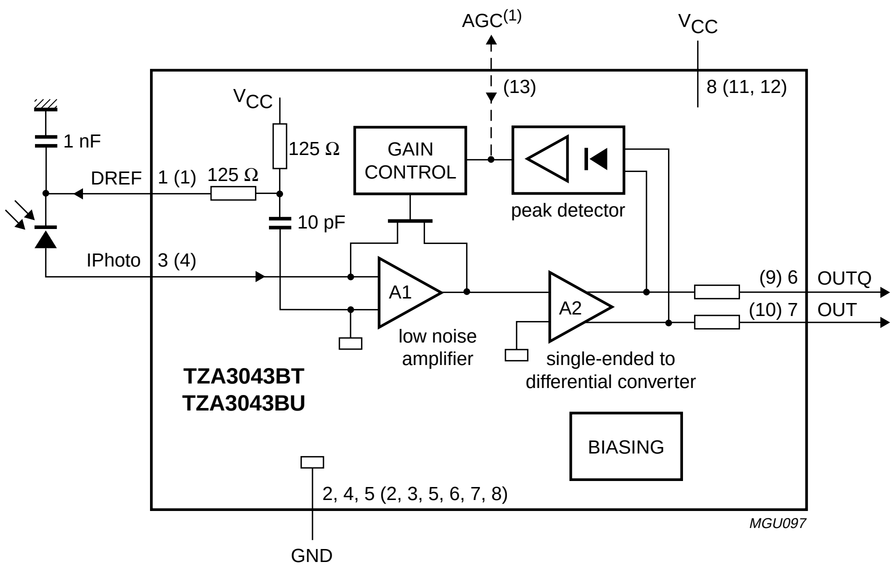
BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the bare die version.

(1) AGC analog I/O (pad 13) is only available on the TZA3043U.

Fig.1 Block diagram of TZA3043T and TZA3043U.



The numbers in brackets refer to the pad numbers of the bare die version.

(1) AGC analog I/O (pad 13) is only available on the TZA3043BU.

Fig.2 Block diagram of TZA3043BT and TZA3043BU.

PINNING

SYMBOL	PIN TZA3043T	PIN TZA3043BT	PAD TZA3043U	PAD TZA3043BU	TYPE	DESCRIPTION
DREF	1	1	1	1	analog output	bias voltage for PIN diode; cathode should be connected to this pin
GND	2	2	2, 3	2, 3	ground	ground
IPhoto	3	3	4	4	analog input	current input; anode of PIN diode should be connected to this pin; DC bias level of 822 mV is one diode voltage above ground
GND	4	4	5, 6	5, 6	ground	ground
GND	5	5	7, 8	7, 8	ground	ground
OUT	6	7	9	10	data output	data output; pin OUT goes HIGH when current flows into pin IPhoto
OUTQ	7	6	10	9	data output	compliment of pin OUT
V_{CC}	8	8	11, 12	11, 12	supply	supply voltage
AGC	–	–	13	13	input/ output	AGC analog I/O

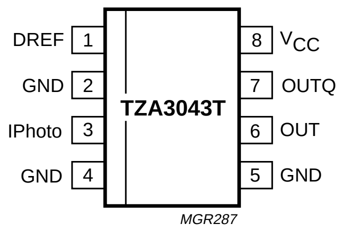


Fig.3 Pin configuration of TZA3043T.

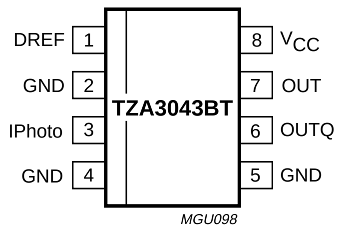


Fig.4 Pin configuration of TZA3043BT.

FUNCTIONAL DESCRIPTION

The TZA3043 is a transimpedance amplifier intended for use in fibre optic links for signal recovery in Fibre Channel or Gigabit Ethernet applications. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and transforms it into a differential output voltage. The most important characteristics of the TZA3043 are high receiver sensitivity and wide dynamic range. High receiver sensitivity is achieved by minimizing noise in the transimpedance amplifier.

Input circuit

The signal current generated by a PIN diode can vary between 2.5 μA to 1.5 mA (p-p).

An AGC loop is implemented to make it possible to handle such a wide dynamic range. The AGC loop increases the dynamic range of the receiver by reducing the feedback resistance of the preamplifier.

The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not needed for AGC.

AGC monitoring

The AGC voltage can be monitored at pad 13 on the bare die (TZA3043U/TZA3043BU). Pad 13 is not bonded in the packaged device (TZA3043T/TZA3043BT). This pad can be left unconnected during normal operation. It can also be used to force an external AGC voltage. If pad 13 (AGC) is connected to GND, the internal AGC loop is disabled and the receiver gain is at a maximum. The maximum input current is then approximately 75 μA.

Output circuit

A differential amplifier converts the output of the preamplifier to a differential voltage (see Fig.5).

The logic level symbol definitions for the differential outputs are shown in Fig.6.

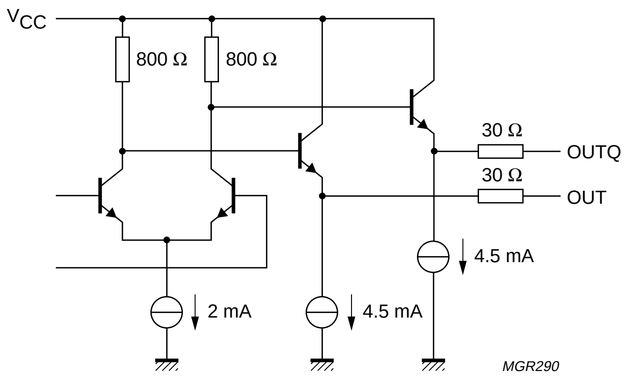


Fig.5 Differential data output circuit.

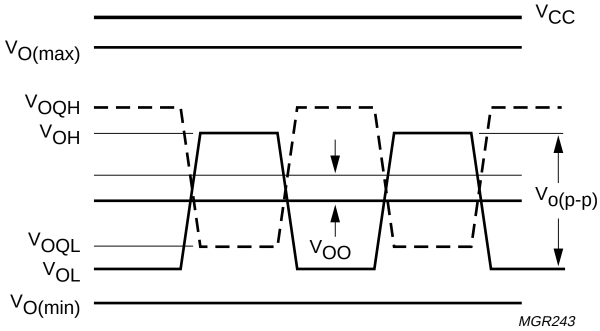


Fig.6 Logic level symbol definitions for data outputs OUT and OUTQ.

PIN diode bias voltage DREF

The transimpedance amplifier together with the PIN diode determines the performance of an optical receiver for a large extent. Especially how the PIN diode is connected to the input and the layout around the input pin influence the key parameters like sensitivity, the bandwidth and the Power Supply Rejection Ratio (PSRR) of a transimpedance amplifier. The total capacitance at the input pin is critical to obtain the highest sensitivity. It should be kept to a minimum by reducing the capacitance of the PIN diode and the parasitics around the input pin. The PIN diode should be placed very close to the IC to reduce the parasitics. Because the capacitance of the PIN diode depends on the reverse voltage across it, the reverse voltage should be chosen as high as possible.

The PIN diode can be connected to the input in two ways as shown in Figs 7 and 8. In Fig.7 the PIN diode is connected between pins DREF and IPhoto. Pin DREF provides an easy bias voltage for the PIN diode. The voltage at DREF is derived from V_{CC} by a low-pass filter. The low-pass filter consisting of the internal resistors R1, R2, C1 and the external capacitor C2 rejects the supply voltage noise. The external capacitor C2 should be equal or larger then 1 nF for a high PSRR.

The reverse voltage across the PIN diode is 4.18 V (5 – 0.82 V) for 5 V supply or 2.48 V (3.3 – 0.82 V) for 3.3 V supply.

It is preferable to connect the cathode of the PIN diode to a higher voltage then V_{CC} when such a voltage source is available on the board. In this case pin DREF can be left unconnected. When a negative supply voltage is available, the configuration in Fig.8 can be used. It should be noted that in this case the direction of the signal current is reversed compared to the Fig.7. Proper filtering of the bias voltage for the PIN diode is essential to achieve the highest sensitivity level.

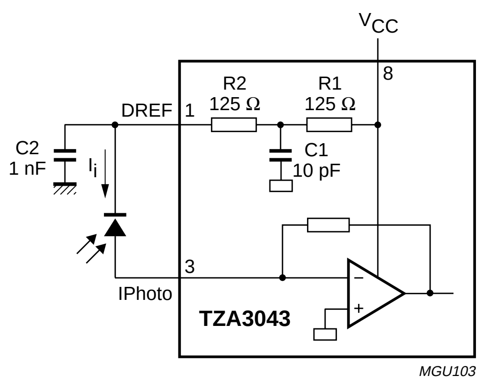


Fig.7 The PIN diode connected between the input and pin DREF.

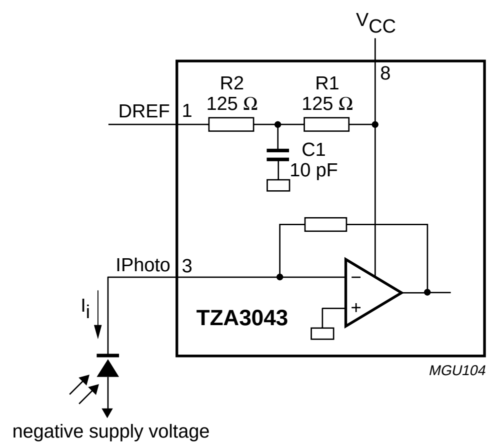


Fig.8 The PIN diode connected between the input and a negative supply voltage.

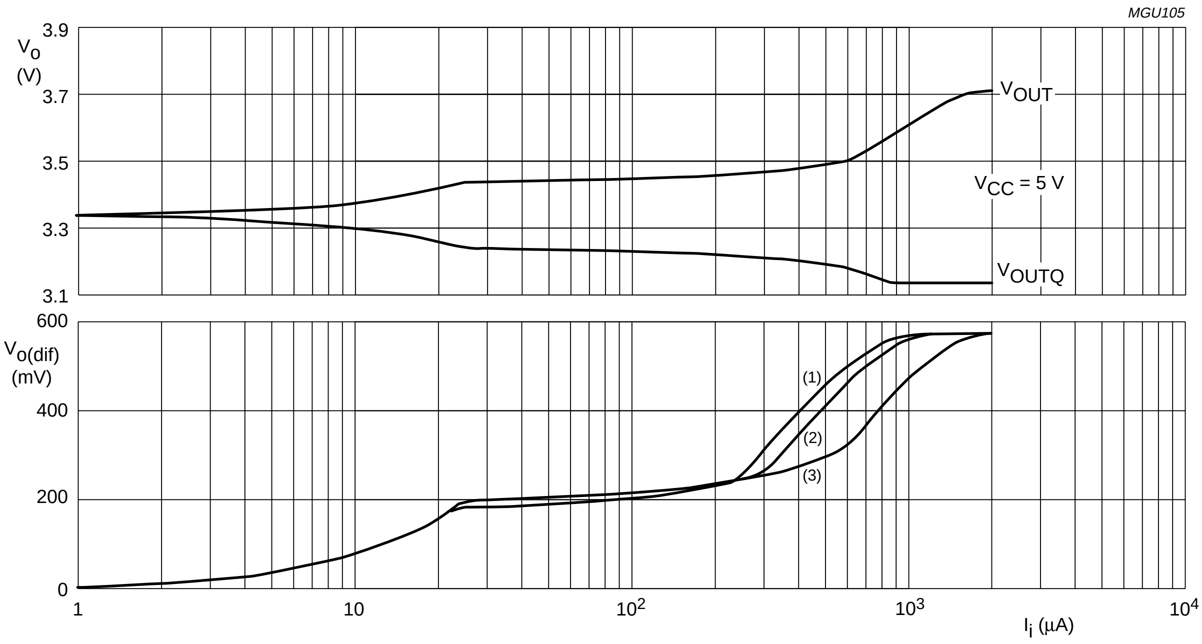
AGC

The TZA3043 transimpedance amplifier can handle input currents from 1 μA to 1.5 mA. This means a dynamic range of 63 dB. At low input currents, the transimpedance must be high to get enough output voltage, and the noise should be low enough to guaranty minimum bit error rate. At high input currents however, the transimpedance should be low to avoid pulse width distortion. This means that the gain of the amplifier has to vary depending on the input signal level to handle such a wide dynamic range. This is achieved in the TZA3043 by implementing an Automatic Gain Control (AGC) loop. The AGC loop consists of a peak detector, a hold capacitor and a gain control circuit.

The peak amplitude of the signal is detected by the peak detector and it is stored on the hold capacitor. The voltage over the hold capacitor is compared to a threshold level. The threshold level is set to 25 μA (p-p) input current. AGC becomes active only for input signals larger than the threshold level. It is disabled for smaller signals. The transimpedance is then at its maximum value (8.3 kΩ differential).

When AGC is active, the feedback resistor of the transimpedance amplifier is reduced to keep the output voltage constant. The transimpedance is regulated from 8.3 kΩ at low currents (I < 30 μA) to 1 kΩ at high currents (I < 500 μA). Above 500 μA the transimpedance is at its minimum and can not be reduced further but the front-end remains linear until input currents of 1.5 mA.

The upper part of Fig.9 shows the output voltages of the TZA3043 (OUT and OUTQ) as a function of the DC input current. In the lower part, the difference of both voltages is shown. It can be seen from the figure that the output changes linearly up to 25 μA input current where AGC becomes active. From this point on, AGC tries to keep the differential output voltage constant around 200 mV for medium range input currents (input currents <200 μA). The AGC can not regulate any more above 500 μA input current and the output voltage rises again with the input current.



$V_{o(dif)} = V_{OUT} - V_{OUTQ}$.

(1) V_{CC} = 3 V.

(2) V_{CC} = 3.3 V.

(3) V_{CC} = 5 V.

Fig.9 AGC characteristics.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6	V
V_n	DC voltage			
	pin/pad IPhoto	–0.5	+1	V
	pins/pads OUT and OUTQ	–0.5	V_{CC} + 0.5	V
	pad AGC (bare die only)	–0.5	V_{CC} + 0.5	V
	pin/pad DREF	–0.5	V_{CC} + 0.5	V
I_n	DC current			
	pin/pad IPhoto	–2.5	+2.5	mA
	pins/pads OUT and OUTQ	–15	+15	mA
	pad AGC (bare die only)	–0.2	+0.2	mA
	pin/pad DREF	–2.5	+2.5	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

HANDLING

Precautions should be taken to avoid damage through electrostatic discharge. This is particularly important during assembly and handling of the bare die. Additional safety can be obtained by bonding the V_{CC} and GND pads first, the remaining pads may then be bonded to their external connections in any order.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	160	K/W

CHARACTERISTICS

Typical values at T_{amb} = 25 °C and V_{CC} = 5 V; minimum and maximum values are valid over the entire ambient temperature range and supply range; all voltages are measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3	5	5.5	V
I_{CC}	supply current	AC coupled; R_L = 50 Ω	–	34	47	mA
P_{tot}	total power dissipation	V_{CC} = 5 V	–	170	259	mW
		V_{CC} = 3.3 V	–	112	169	mW
T_j	junction temperature		–40	–	+125	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
R_{tr}	small-signal transresistance of the receiver	measured differentially; AC coupled				
		R_L = ∞	13.2	16.6	20	kΩ
		R_L = 50 Ω	6.6	8.3	10	kΩ
$f_{-3dB(h)}$	high frequency –3 dB point	V_{CC} = 5 V; C_i = 0.7 pF	1000	1200	–	MHz
		V_{CC} = 3.3 V; C_i = 0.7 pF	850	1100	–	MHz
PSRR	power supply rejection ratio	measured differentially; note 1				
		f = 1 to 100 MHz	–	2	–	μA/V
		f = 1 GHz	–	66	–	μA/V
Bias voltage: pin DREF						
R_{DREF}	resistance between DREF and V_{CC}	tested at DC	210	250	290	Ω
Input: pin IPhoto						
$V_{bias(IPhoto)}$	input bias voltage on pin IPhoto		600	822	1000	mV
$I_{i(IPhoto)(p-p)}$	input current on pin IPhoto (peak-to-peak value)	V_{CC} = 5 V; note 2	–1500	+6	+1500	μA
		V_{CC} = 3.3 V; note 2	–1000	+6	+1000	μA
R_i	small-signal input resistance	f_i = 1 MHz; input current <2 μA (p-p)	–	28	–	Ω
$I_{n(tot)}$	total integrated RMS noise current over bandwidth	referenced to input; Δf = 920 MHz; note 3	–	200	–	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data outputs: pins OUT and OUTQ						
$V_{o(cm)}$	common mode output voltage	AC coupled; R_L = 50 Ω	V_{CC} – 2	V_{CC} – 1.7	V_{CC} – 1.4	V
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	AC coupled; R_L = 50 Ω; input current 100 μA (p-p)	75	200	330	mV
V_{OO}	differential output offset voltage		–100	–	+100	mV
R_o	output resistance	single-ended; DC tested	40	50	62	Ω
t_r, t_f	rise time, fall time	V_{CC} = 5 V; 20% to 80%; input current <20 μA (p-p)	–	285	430	ps
		V_{CC} = 3.3 V; 20% to 80%; input current <20 μA (p-p)	–	300	460	ps
Automatic gain control loop: pad AGC						
$I_{th(AGC)}$	AGC threshold current	referenced to the peak input current; tested at 10 MHz	–	25	–	μA
$t_{att(AGC)}$	AGC attack time		–	5	–	μs
$t_{decay(AGC)}$	AGC decay time		–	10	–	ms

Notes

1. PSRR is defined as the ratio of the equivalent current change at the input (ΔI_{IPhoto}) to a change in supply voltage:

$$PSRR = \frac{\Delta I_{IPhoto}}{\Delta V_{CC}}$$

For example, a +10 mV disturbance on V_{CC} at 10 MHz will typically add an extra 20 nA to the photodiode current. The external capacitor between pins DREF and GND has a large impact on the PSRR. The specification is valid with an external capacitor of 1 nF.

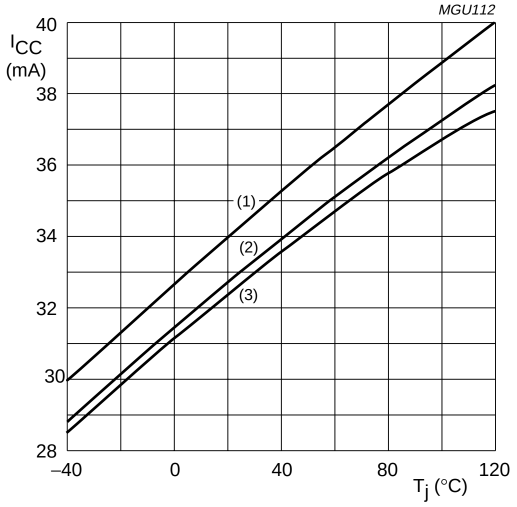
2. The pulse width distortion (PWD) is <5% over the whole input current range. The PWD is defined as:

$$PWD = \left(\frac{\text{pulse width}}{T} - 1\right) \times 100\%$$

where T is the clock period. The PWD is measured differentially with PRBS pattern of 10^{-23}.

3. All $I_{n(tot)}$ measurements were made with an input capacitance of C_i = 1 pF. This was comprised of 0.5 pF for the photodiode itself, with 0.3 pF allowed for the printed-circuit board layout and 0.2 pF intrinsic to the package. Noise performance is measured differentially.

TYPICAL PERFORMANCE CHARACTERISTICS



(1) V_{CC} = 5 V.
(2) V_{CC} = 3.3 V.
(3) V_{CC} = 3 V.

Fig.10 Supply current as a function of the junction temperature.

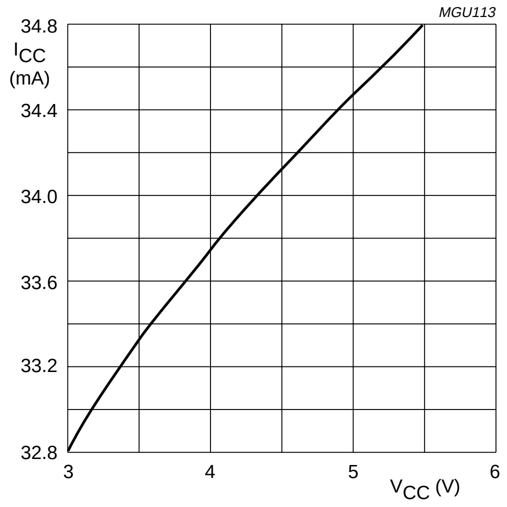


Fig.11 Supply current as a function of the supply voltage.

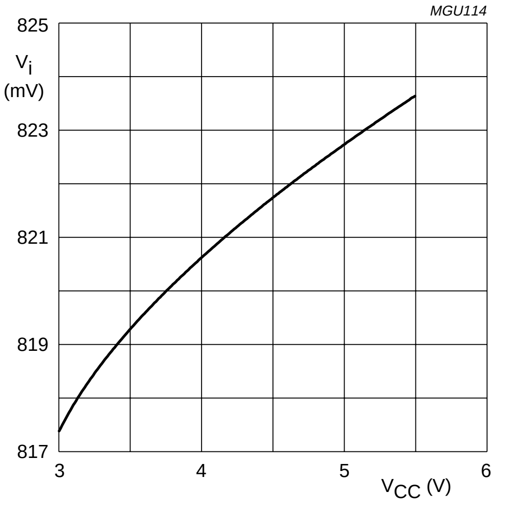
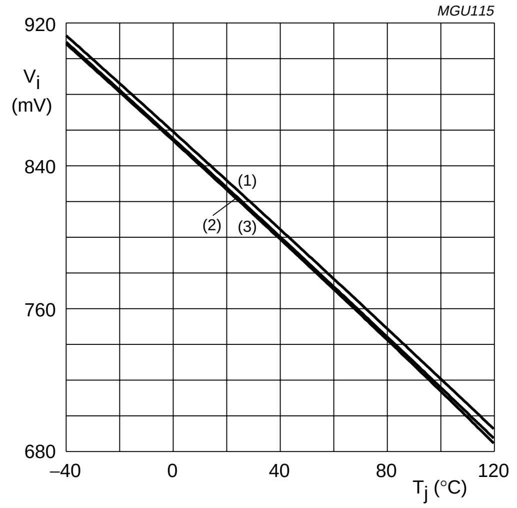
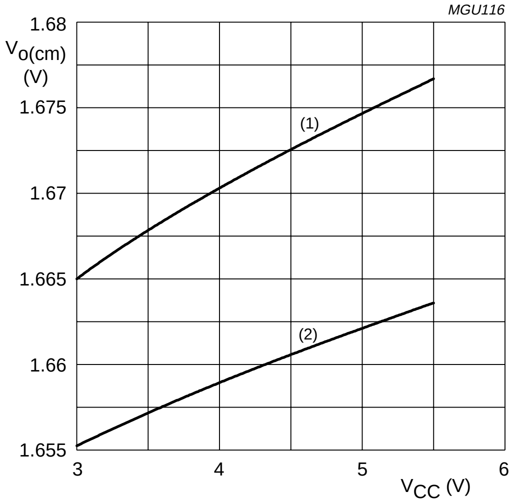


Fig.12 Input voltage as a function of the supply voltage.



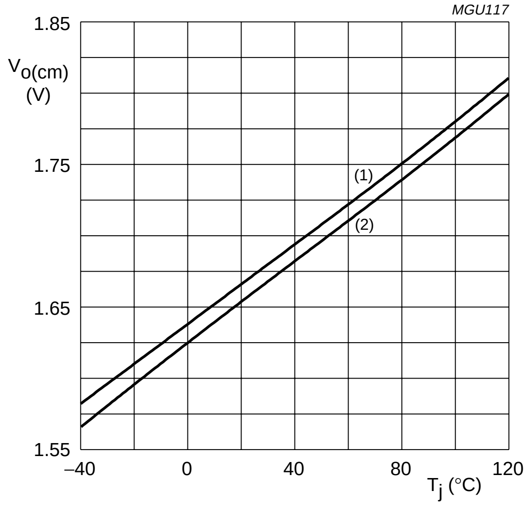
(1) V_{CC} = 5 V.
(2) V_{CC} = 3.3 V.
(3) V_{CC} = 3 V.

Fig.13 Input voltage as a function of the junction temperature.



(1) $V_{CC} - V_{OUT}$.
(2) $V_{CC} - V_{OUTQ}$.

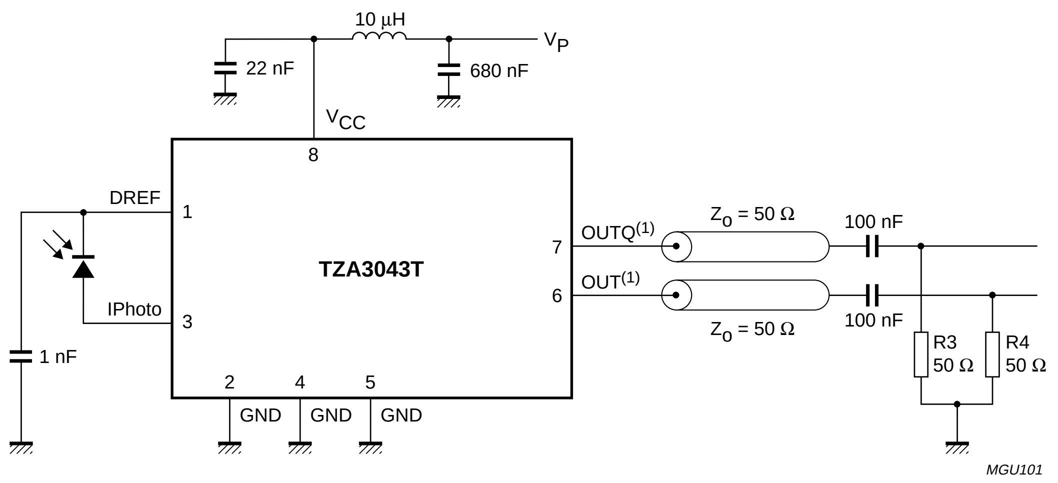
Fig.14 Common mode voltage at the output as a function of the supply voltage.



V_{CC} = 5 V.
(1) $V_{CC} - V_{OUT}$.
(2) $V_{CC} - V_{OUTQ}$.

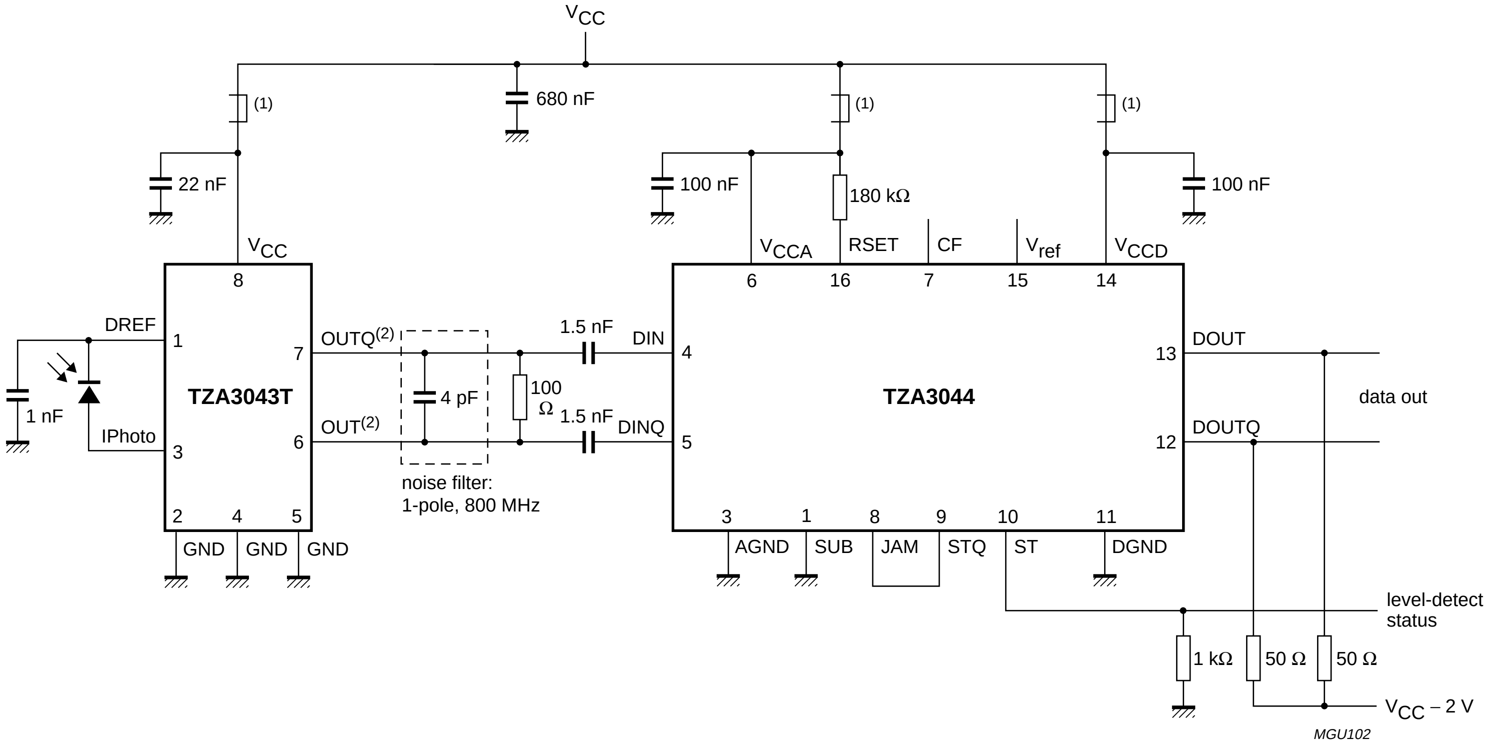
Fig.15 Common mode voltage at the output as a function of the junction temperature.

APPLICATION AND TEST INFORMATION



(1) For TZA3043BT pin 7 is OUT and pin 6 is OUTQ.

Fig.16 Application diagram.



(1) Ferrite bead e.g. Murata BLM10A700S.

(2) For TZA3043BT pin 7 is OUT and pin 6 is OUTQ.

Fig.17 Gigabit Ethernet/Fibre Channel receiver using the TZA3043T and TZA3044.

Test circuits

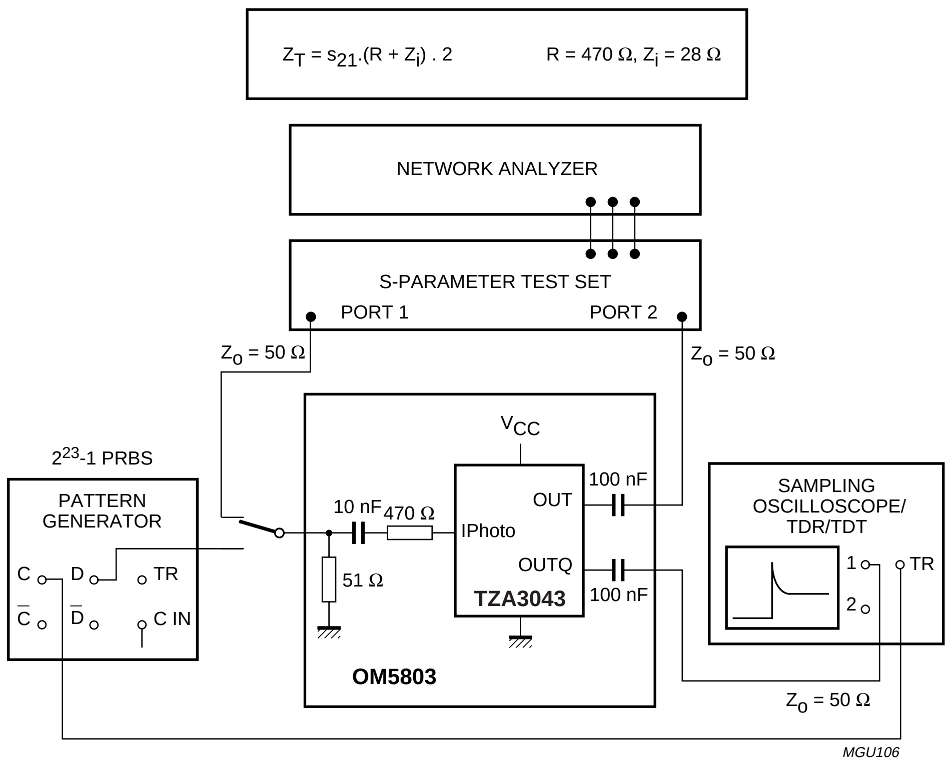


Fig.18 Electrical test circuit.

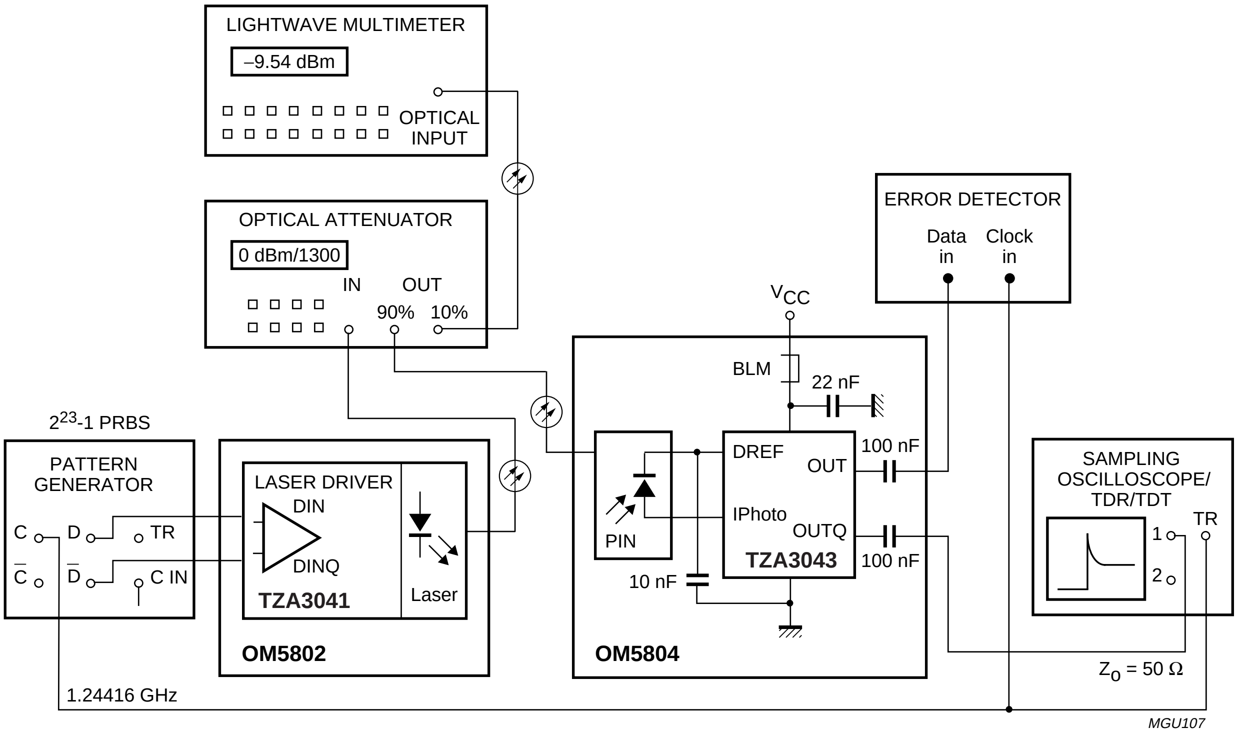


Fig.19 Optical test circuit.

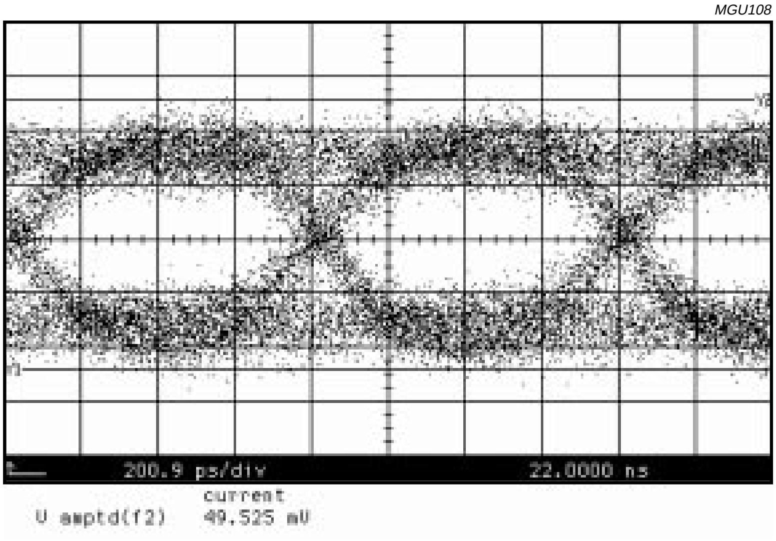


Fig.20 Differential output with –25 dBm optical input power [input current of 5.17 µA (p-p)].

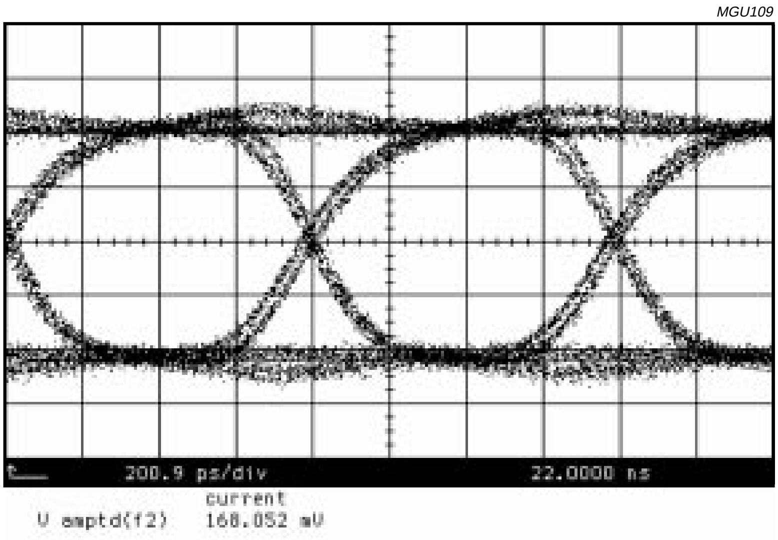


Fig.21 Differential output with –15 dBm optical input power [input current of 51.7 µA (p-p)].

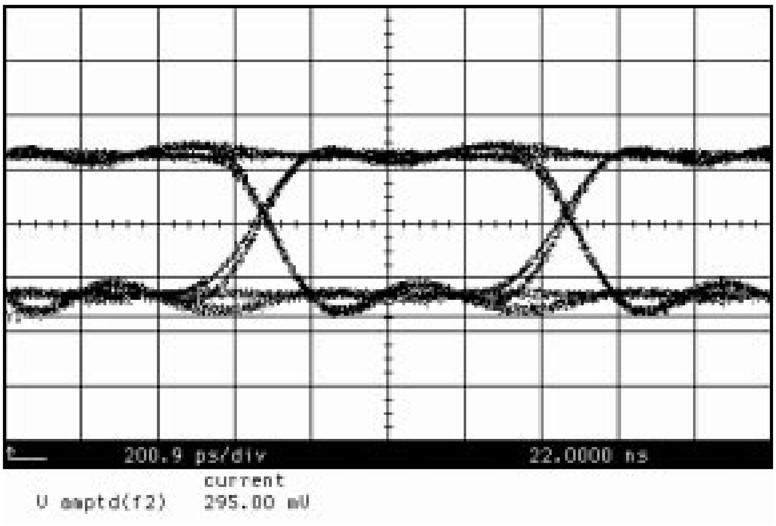


Fig.22 Differential output with –5 dBm optical input power [input current of 517 μA (p-p)].

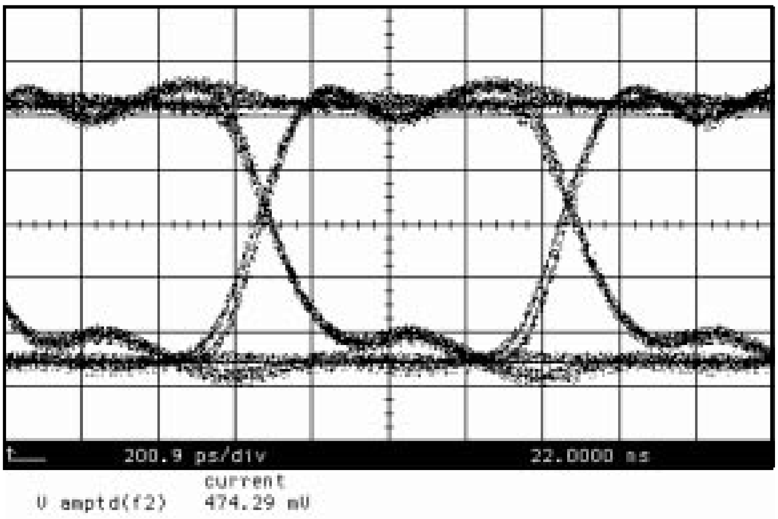


Fig.23 Differential output with –2 dBm optical input power [input current of 1030 μA (p-p)].

BONDING PAD LOCATIONS

SYMBOL	PAD TZA3043U	PAD TZA3043BU	COORDINATES[1]	
			x	y
DREF	1	1	95	881
GND	2	2	95	618
GND	3	3	95	473
IPhoto	4	4	95	285
GND	5	5	215	95
GND	6	6	360	95
GND	7	7	549	95
GND	8	8	691	95
OUT	9	10	785	501
OUTQ	10	9	785	641
V_{CC}	11	11	567	1055
V_{CC}	12	12	424	1055
AGC	13	13	259	1055

Note

1. All coordinates are referenced, in µm, to the bottom left-hand corner of the die.

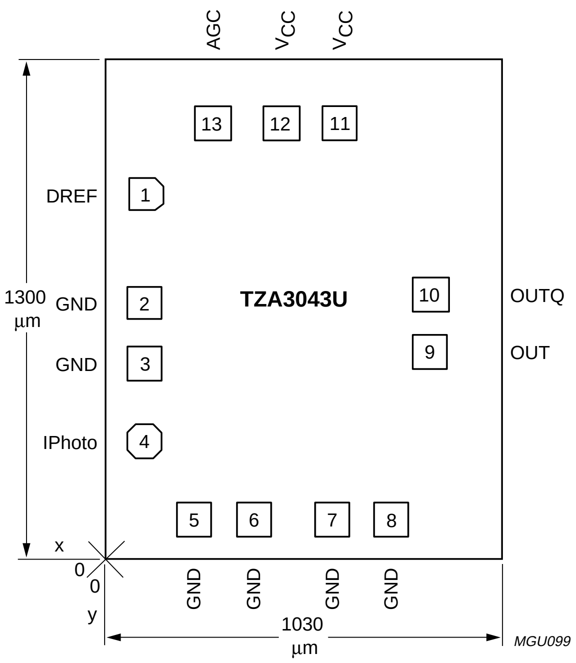


Fig.24 Bonding pad locations of the TZA3043U.

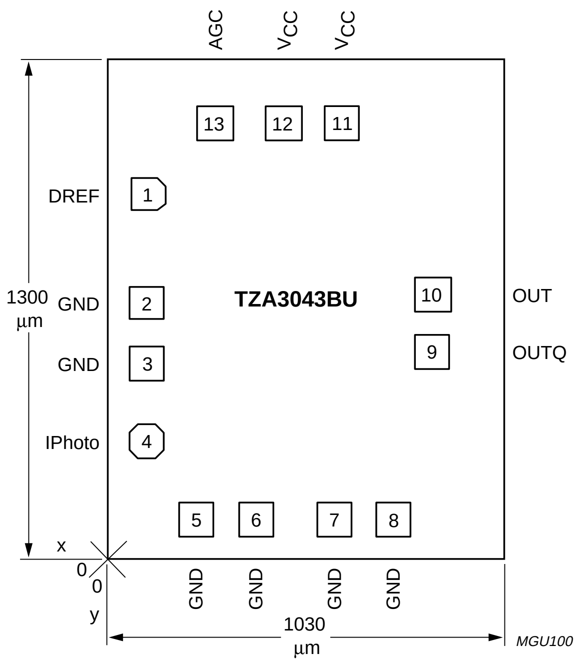


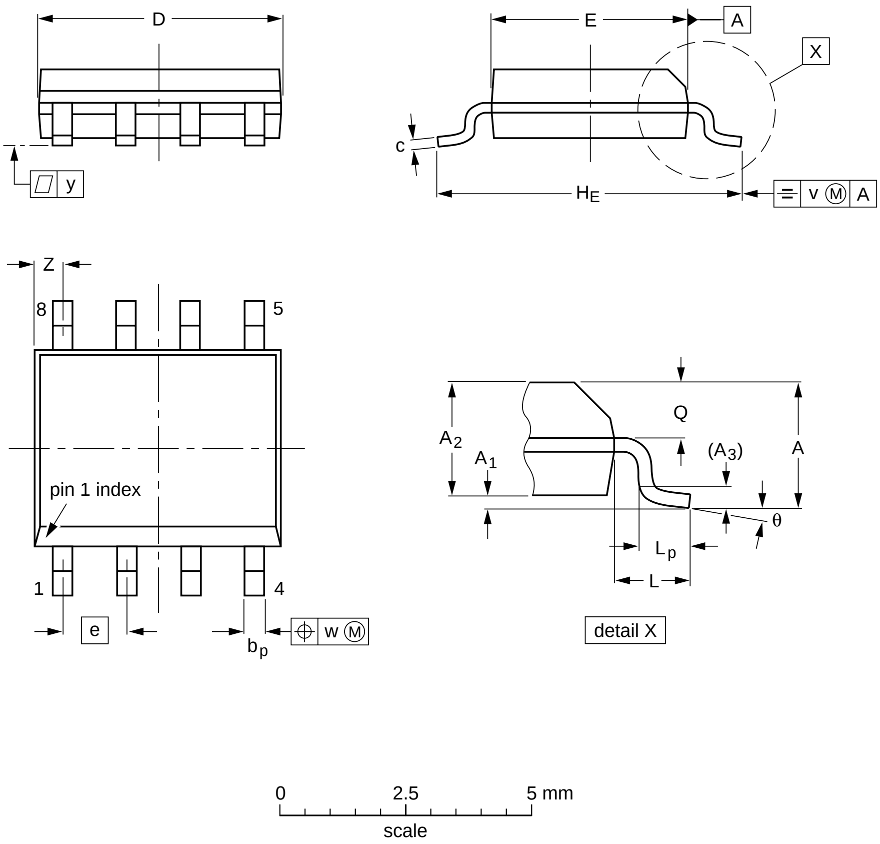
Fig.25 Bonding pad locations of the TZA3043BU.

Physical characteristics of the bare die

PARAMETER	VALUE
Glass passivation	2.1 µm PSG (PhosphoSilicate Glass) on top of 0.65 µm oxynitride
Bonding pad dimension	minimum dimension of exposed metallization is 90 × 90 µm (pad size = 100 × 100 µm)
Metallization	1.22 µm W/AlCu/TiW
Thickness	380 µm nominal
Size	1.03 × 1.30 mm (1.34 mm^2)
Backing	silicon; electrically connected to GND potential through substrate contacts
Attach temperature	<440 °C; recommended die attach is glue
Attach time	<15 s

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(2)]	e	H_E	L	L_p	Q	v	w	y	Z[(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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