Programmable Telephone Audio Processor

Description

The programmable telephone audio processor U3900BM is a linear integrated circuit for use in feature phones, answering machines, fax machines and cordless phones. It contains the speech circuit, tone-ringer interface with DC/DC converter, sidetone equivalent and ear-protection rectifiers. The circuit is line-powered and contains all components necessary for signal amplification and adaptation to the line. The U3900BM can also be supplied via an external power supply. An integrated voice switch with loudspeaker amplifier enables hands-free or loud-hearing operation. With an anti-feedback function, acoustical feedback during loudhearing can be reduced significantly. The generated supply voltage is suitable for a wide range of peripheral circuits.

Features

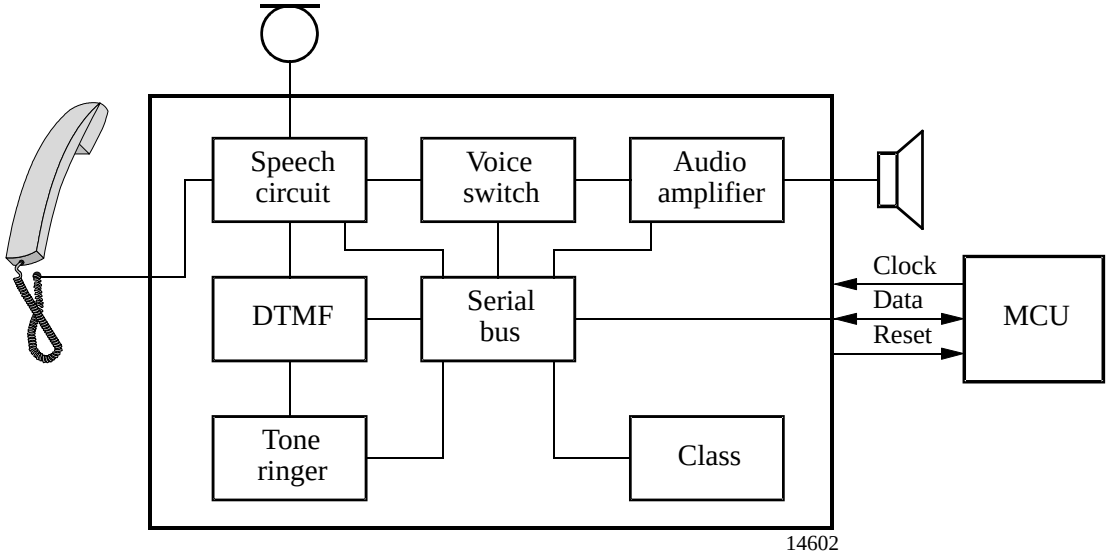
- Speech circuit with anti-clipping
- Tone ringer interface with DC/DC converter
- Speaker amplifier with anti-distortion
- Power-supply management, regulated, unregulated and a special supply for electret microphone
- Voice switch
- CLID + SCWID
- DTMF generator
- Switch matrix
- Line current information
- Fully programmable
- Watchdog

Benefits

- Savings of one piezoelectric transducer
- Complete system integration of analog signal processing on one chip
- Very few external components
- Highly integrated solution
- Extremely versatile due to full programmability

Applications

Feature phone, answering machine, fax machine, speaker phone, base station of cordless phone



Ordering Information

Extended Type Number	Package	Remarks
U3900BM-AFN	SSO44	
U3900BM-AFNG3	SSO44	Taped and reeled

Pin Description

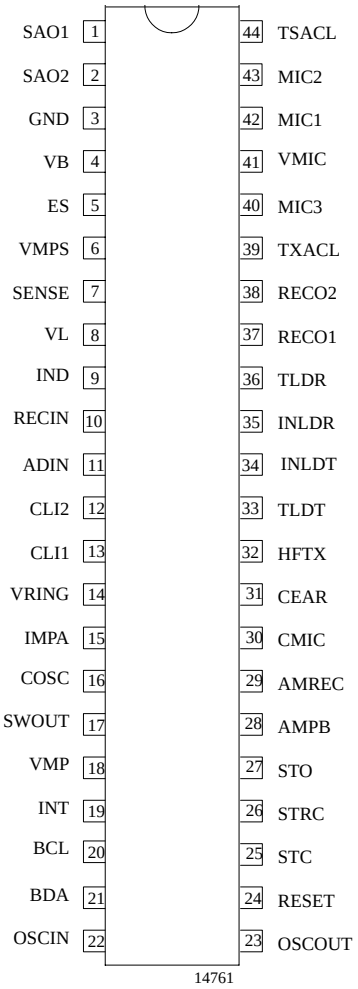


Figure 1. Pinning

Pin	Symbol	Function
1	SAO1	Positive output of speaker amplifier (single ended and push-pull operation)
2	SAO2	Negative output of speaker amplifier (push-pull only)
3	GND	Ground, reference point for DC- and AC signals
4	VB	Unstabilized supply voltage
5	ES	Input for external supply indication
6	VMPS	Unregulated supply voltage for the micro-controller (via series regulator to VMP)
7	SENSE	Input for sensing the available line current
8	VL	Positive supply-voltage input to the device in speech mode
9	IND	The internal equivalent inductance of the circuit is proportional to the value of the capacitor at this pin. A resistor connected to ground may be used to adjust the DC mask.
10	RECIN	Receive amplifier input
11	ADIN	Input of A/D converter
12	CLI2	CLID input 2
13	CLI1	CLID input 1
14	VRING	Input for ringer supply
15	IMPA	Input for adjusting the ringer input impedance
16	COSC	70-kHz oscillator for ringing power converter
17	SWOUT	Output for driving the external switching transistor
18	VMP	Regulated output voltage for supplying the microcontroller (typ. 3.3 V/ 6 mA in speech mode)
19	INT	Interrupt line for serial bus
20	BCL	Clock input for serial bus
21	BDA	Data line for serial bus
22	OSCIN	Input for 3.58-MHz oscillator
23	OSCOUT	Clock output for the microcontroller
24	RESET	Reset output for the microcontroller
25	STC	Input for sidetone network
26	STRC	Input for sidetone network
27	STO	Output for connecting the sidetone network
28	AMPB	Input for playback signal of answering machine
29	AMREC	Output for recording signal of answering machine
30	CMIC	Input for cordless telephone
31	CEAR	Output for cordless telephone
32	HFTX	Output for transmit-level detector in intercom mode
33	TLDT	Time constant of transmit-level detector
34	INLDT	Input of transmit-level detector
35	INLDR	Input of receive-level detector
36	TLDR	Time constant of receive-level detector
37	RECO1	Positive output of the receive amplifier, also used for sidetone network
38	RECO2	Negative output of the receive amplifier
39	TXACL	Time-constant adjustment for transmit anti-clipping
40	MIC3	Input of hands-free microphone
41	VMIC	Reference node for microphone amplifier, supply for electret microphone
42	MIC1	Inverting input of symmetrical microphone amplifier with high common-mode rejection ratio
43	MIC2	Non-inverting input of symmetrical micro-phone amplifier with high common-mode rejection ratio
44	TSACL	Time-constant for speaker amplifier anti-clipping

Table of Contents

1 Block Diagram

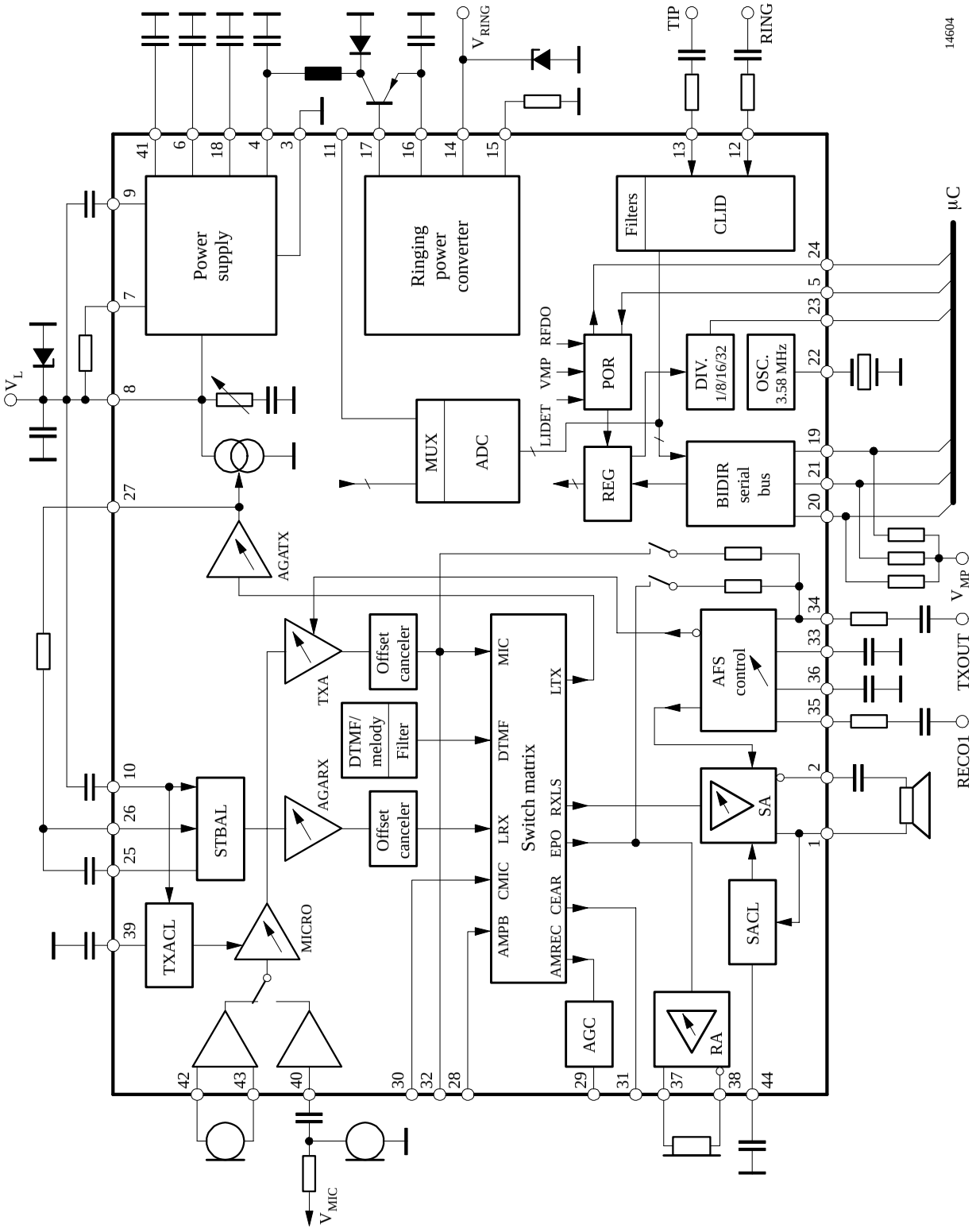


Figure 2. Block diagram

2 Class Function

The U3900BM includes a class function **C**alling **L**ine **ID**entification (CLID) for on-hook and **S**pontaneous **C**all **W**aiting **ID**entifier (SCWID) for off-hook status.

2.1 CLID

CLID is designed to demodulate CCITT V23 and BELL 202 (1200 bauds FSK asynchronous data) and is compatible with both formats without external intervention. It fulfils the CS B14-10W requirements.

The main feature of this part is to provide, for the user, information about the caller before answering the call. The information is a DATA message sent from the **C**entral **O**ffice (CO) to the CPE during the silent interval, and after the first ringing burst.

2.1.1 Description

On the receive side, the received signal coming from CLI1 and CLI2 first goes to an antialiasing filter after the differential op-amp.

The next section is a bandpass filter composed of an FSK filter composed of a fifth order high-pass followed by a third order low-pass filter. The low-pass and high-pass cut-off frequencies are about 300 Hz and 3400 Hz respectively.

2.1.2 Carrier Detect

The carrier detect provides an indication (to the microprocessor with an interrupt request) of the presence of a signal in the FSK band. It detects a sufficient amplitude signal at the output of the FSK bandpass filter.

Note that signals such as speech or DTMF tones also lie in the FSK frequency band and the carrier detect may be activated by these signals. The signals will be demodulated and presented as DATA. To avoid false DATA detection, a command bit is used to disable the demodulator when no FSK signal is expected.

Four bits are provided to improve carrier detection [CD_CD <3..0>]. With these bits it is possible to select a capture window (see the tables next page), and avoid a false detection.

With the use of SCD bit the carrier detect function is improved, because after a normal carrier detection (NCD), a part (10 bits) of the channel seizure is taken in count before alerting the microprocessor.

Note:
When the CPE is off hook (SCWID mode) the CO sends FSK data without channel seizure. The mark signal = 80 bits ±10 at 1200 bauds (1300 Hz continuously during 67 ms).

For this case a selected bandpass 1000 Hz to 1700 Hz could be very useful for the carrier detect ...

After the interrupt due to the carrier detect the microprocessor can change the bandpass frequencies according to the FSK band.

- The normal carrier detect guard time is 26.4 ms.
- The improved carrier detect guard time is 34.7 ms.
- The carrier lost guard time is 8.8 ms, in all the cases.

2.1.3 Demodulator

This part is enabled with the carrier detect signal.

The reference signal is at 1700 Hz, (the same frequency for BELL 202 and V23). All the incoming signals are compared to this value to make a digital square wave frequency varying in frequency and in phase as a function of the input frequencies.

2.1.4 Clock Recovery

The process starts at the first low-level bit received from the demodulator. After that the CLOCK is generated for the 10 serial bits (1 bit start, 8 bits data, 1 bit stop).When all the data are received DATA READY is generated. This signal loads the serial data in a parallel buffer.

DATA READY provides an indication (to the microprocessor with an interrupt request) of the presence data byte available.

2.1.5 Data Recovery and Buffer

The incoming serial data are stored and sent to the SSB each 10 bits (1 start bit, 8 data, 1 stop bit). When after a start bit 8 data bits and a stop bit are received, an interrupt is generated, the INT pin will become active, and data ready interrupt bit is set in the status register (bit 3). The received data is available in the CLID DATA register.

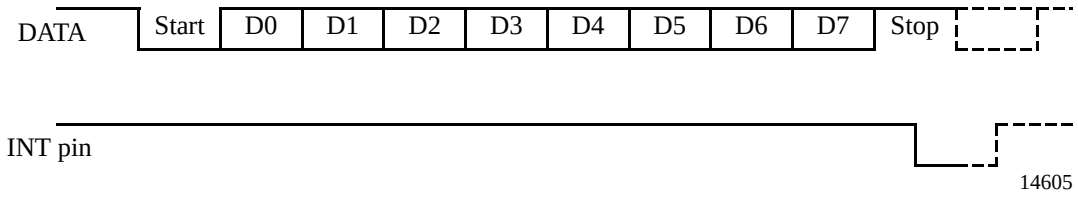


Figure 3. Interrupt treatment for SLID DATA register

2.1.6 CLID: Logical Part

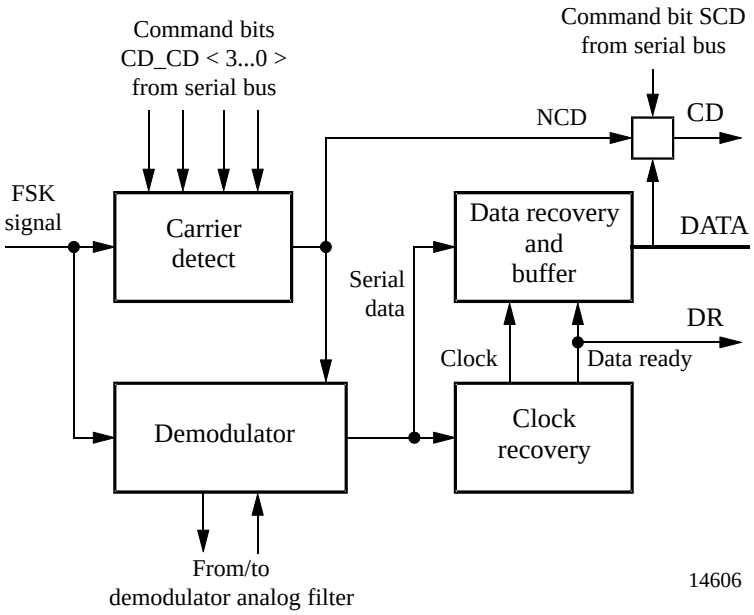


Figure 4. Block diagram for CLID logical part

2.1.7 Carrier Detect, Bandpass Frequencies

Low Frequencies

CD_CD<0>	CD_CD<1>	Value
0	0	290 Hz
1	0	515 Hz
0	1	770 Hz
1	1	1000 Hz

High Frequencies

CD_CD<2>	CD_CD<3>	Value
0	0	3400 Hz
1	0	3100 Hz
0	1	2665 Hz
1	1	1700 Hz

2.1.8 Special Carrier Detect

If SCD = 0 Detect guard time = 26.4 ms
If SCD = 1 Detect guard time = 34.7 ms (26.4 ms + 10 bits of the channel seizure)

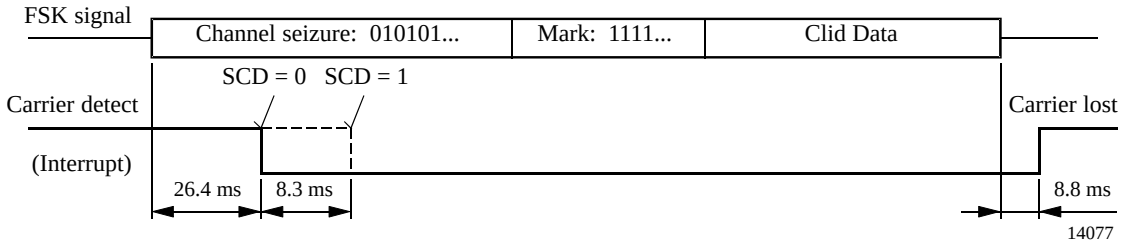


Figure 5. Timing diagram for carrier detect in CLID mode

2.2 SCWID

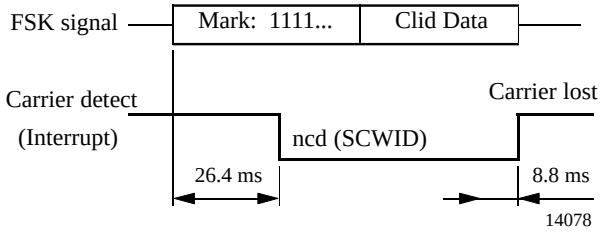


Figure 6. Timing diagram for carrier detect in SCWID mode

The **S**pontaneous **C**all **W**aiting **ID**entifier (SCWID) part is designed to meet:

- The Bellcore "**C**ustomer Premises Equipment **A**lerting **S**ignal (CAS)": TR-NWT-000030 & SR-TSV-002476 specifications.
- The British Telecom "Idle State Tone Alert Signal": SIN227 & SIN242 specifications.
- The European Telecommunication Standard: ETS300 778-1 & ETS300 778-2 specifications.

2.2.1 Overview

SCWID is a feature that allows a subscriber who is already engaged in a telephone call to receive caller ID information about an incoming call.

The European Telecommunication Standard specifies **D**ual-**T**one **A**lerting **S**ignal (DT-AS) for off-line data transmission (on-hook) and on-line data transmission (off-hook).

The British Telecom caller ID uses a Idle State Tone Alert Signal in on-hook mode.

Bellcore specifies a Dual-Tone Alert Signal called CPE Alerting Signal (CAS) for use in off-hook data transmission. Bellcore states that the CPE should be able to detect the CAS in the presence of near end speech. The CAS detector should also be immune to imitation from near and far end speech.

Note that the term "near end" refers to the end of the telephone connection receiving the caller ID service, "far end" refers to the other end of the connection, the **C**entral **O**ffice (CO).

There are two aspects of speech immunity: talk-off and talk-down.

Talk-off is the condition where signals are falsely detected because of imitation by speech or music. An imitation can be caused from the far end or the near end.

Talk-down is the condition where signals are missed because of interference from speech or music.

A CAS can be talked down only from the near end because the far end has already been muted by the CO.

2.2.2 Description

The SCWID part is a complete dual-tone receiver designed to detect the two frequencies 2750 Hz and 2130 Hz dedicated for this alerting function. An output interrupt is provided to the microprocessor when detecting the alert signal.

This device part provides all necessary filtering without any external component.

The on-chip filtering provides excellent signal-to-noise performance.

The dual-tone alert signal is divided into a high and a low bandpass switched capacitor filters:

- The high alert filter is a 2750 Hz bandpass design, with a notch placed at 2130 Hz for low frequency rejection.
- The low alert filter is a 2130 Hz bandpass design, with a notch placed at 2750 Hz for high frequency rejection.

The filter outputs are smoothed and then limited by high-gain comparators which have hysteresis to reduce sensitivity to unwanted low-level signals, jitter and noise. The outputs of the comparators are square-wave signals.

The two resulting rectangular waves are applied to the digital circuitry where a counting algorithm measures and averages their periods. This averaging prevents dual-tone SCWID simulation by extraneous signals such as voice.

The averaging algorithm has been optimized to provide excellent immunity to “talk-off” and tolerance to the presence of interfering frequencies (third tones) and noise.

When both digital circuitries simultaneously detect a valid tone (2130 Hz and 2750 Hz), the signal applied at the guard-time block goes high. Should the alert tone signal be lost, the input signal at the guard-time block will go low.

2.2.3 Guard Time, Overview

To prevent false detection due to talk-off effects and to detect real CAS signals even with drops, a guard-time system is necessary. A guard-time system improves the detection performance and verifies that the duration of a valid signal is sufficient before alerting the microprocessor with an interrupt. It rejects detection of insufficient duration (up guard time) and mask dropouts (down guard time).

There are nine bits for controlling the guard-time block:

- 2 bits, EGT0 and EGT1, for controlling the early guard time
- 2 bits, UGT0 and UGT1, for controlling the up guard time
- 2 bits, DGT0 and DGT1, for controlling the down guard time
- 1 bit, FFD, for controlling the width filter
- 1 bit, FDC, for controlling the drops count
- 1 bit, WP, for enabling the wetting pulse function

One bit is dedicated for enabling the SCWID part.

2.2.4 Up Guard Time, Description

The up guard time circuitry prevents false detection from speech or music (talk-off).

The input signal (both 2130 Hz and 2750 Hz) must be continuously high for a duration depending on the 2 programmable bits UGT0 and UGT1.

DGT0	DGT1	UGT Value
0	0	20 ms
1	0	25 ms
0	1	30 ms
1	1	35 ms

If a drop occurs at any time before the selected value, the detection system is cleared.

Nevertheless, there is the possibility to improve such a system using early guard time circuitry.

2.2.5 Early Guard Time, Description

The early guard time system, when enabled, helps the up guard time to detect a CAS signal even if there are drops in it. But there are conditions before validating such a polluted signal.

The input signal (both 2130 Hz and 2750 Hz) must be continuously high for duration depending on the 2 programmable bits EGT0 and EGT1.

EGT0	EGT1	EGT Value
0	0	Disabled
1	0	8.5 ms
0	1	10.3 ms
1	1	13.7 ms

After that, the input signal is filtered and a drop can occur without clearing the system if it is not too long . The maximum time value depends on the command filter bit FFD.

FFD	Filter Value (Maximum Drop Duration)
0	2 ms
1	4 ms

If there are too many drops, the system is cleared. The count of drops admitted depends on the command count bit FDC.

FDC	Count Value (Maximum Drop Count)
0	4
1	3

The early guard time with filter and count drops allow a good compromise to achieve talk-off and talk-down immunity.

2.2.6 Down Guard Time, Description

The down guard time circuitry prevents drops from speech or music (talk-down).
The input signal (both 2130 Hz and 2750 Hz) must be continuously low for a duration depending on the 2 programmable bits DGT0 and DGT1.
The early guard time is used like for up guard time, but the drop counter is not activated.

* Note:
The Idle State is an electrical condition into which the TE (when connected to the network) is placed such that it draws minimum current and does not activate the exchange.

DGT0	DGT1	DGT Value
0	0	15 ms
1	0	17 ms
0	1	18 ms
1	1	19 ms

2.2.7 Wetting Pulse Function

British Telecom states that the TE is required to apply a DC wetting pulse and an AC load 205 ms after the end of the alerting signal (the Idle State* Tone Alert Signal); the duration of the wetting pulse is 151 ms; the TE shall rise to a minimum of 25 mA and maintain that current for a total time of not less than 5 ms.

OCTEL3 provides a 15-ms counter (which starts at the end of the alerting signal delayed by the down guard time value) to help the microprocessor to fulfil this requirement.

The signals at the output of the guard time system are sent to the SSB-INTERRUPT treatment.

An interrupt occurs at each edge of the OUT SCWID detector.

When the wetting pulse is enabled (CDE8. mode UK = 1), an interrupt is sent to the microprocessor 15 ms after the falling edge of the WP detector.

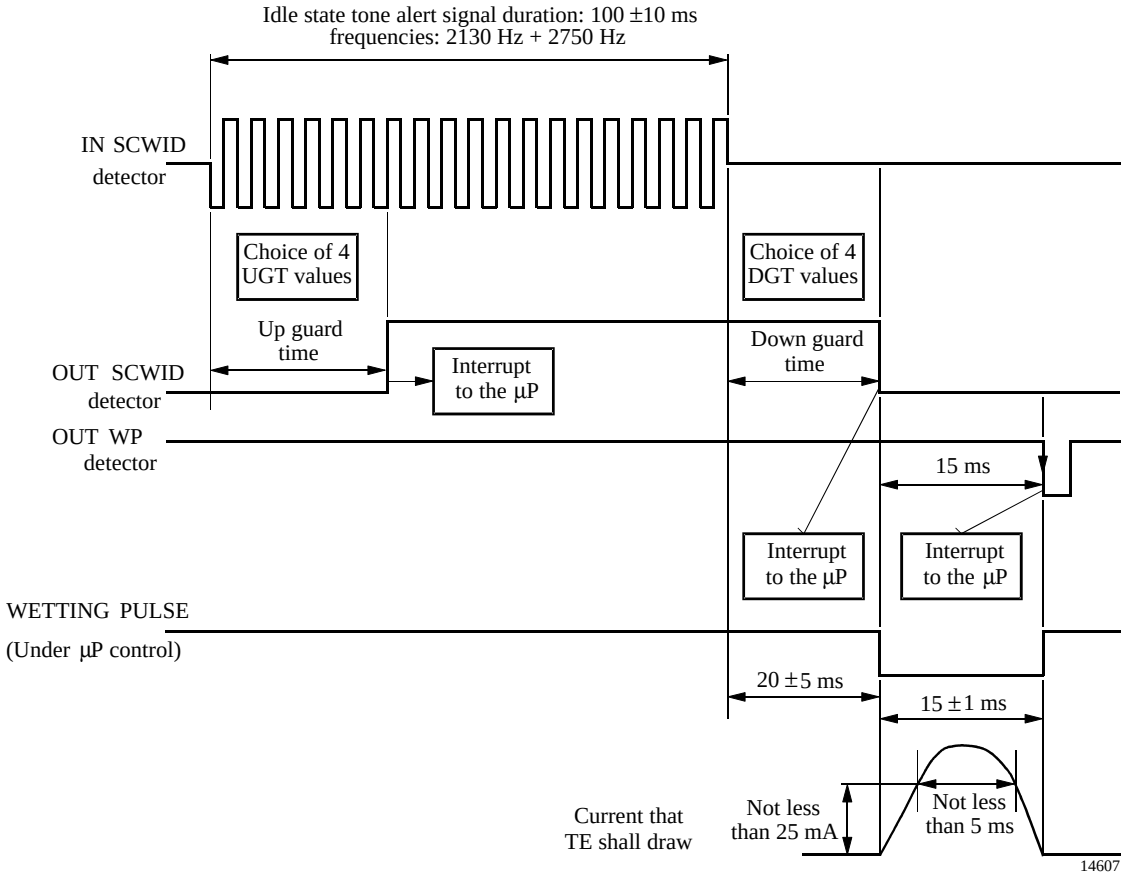


Figure 7. Alert detection timing diagram with wetting pulse

2.2.8 SCWID: Overview

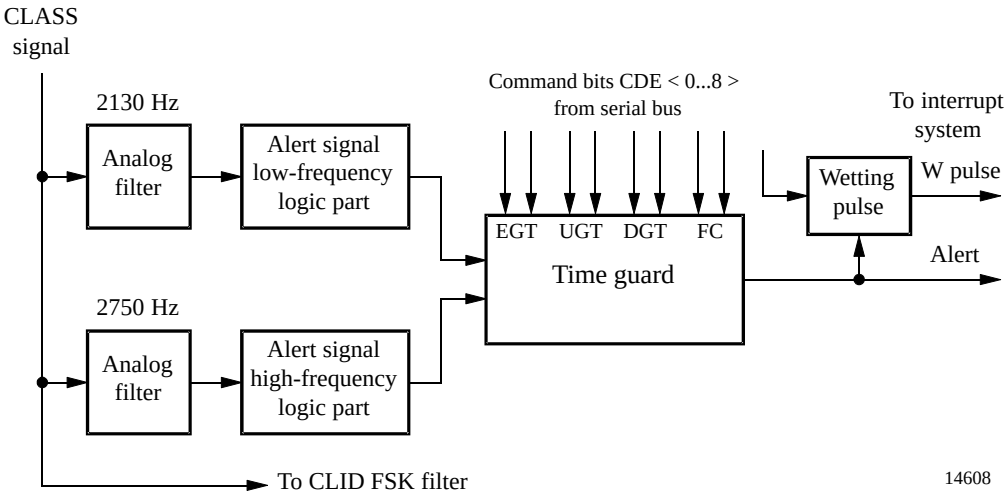


Figure 8. Alert detection

General information:
All the control bits provided for the SCWID function can be modified at any time with the microprocessor.

2.2.9 CAS Detect Process

Typical application:
The incoming signal from the CO is not polluted with speech or music. (The feature early guard time is not used)

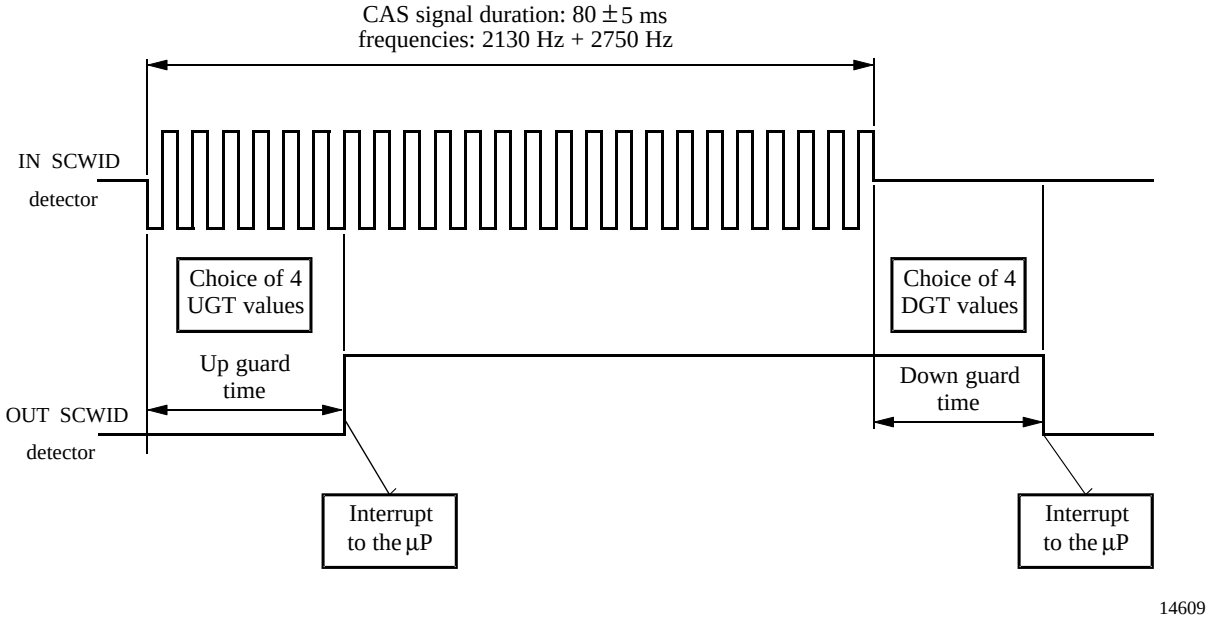


Figure 9. Timing diagram of standard alert detection

If any drop in the CAS signal occurs before the end of the UGT specified value, then the time counter restarts and the OUT SCWID detector remains low.

If any spike in the blank signal occurs before the end of the DGT specified value, then the time counter restarts and the OUT SCWID detector remains high.

CAS Detect Process (continued)

Improved process:
To prevent false detection from speech and music by the far and the near end (talk-off), and to detect the incoming CAS signal from the CO, polluted with speech or music by the near end (talk-down), a new feature is used: the early and up guard time.

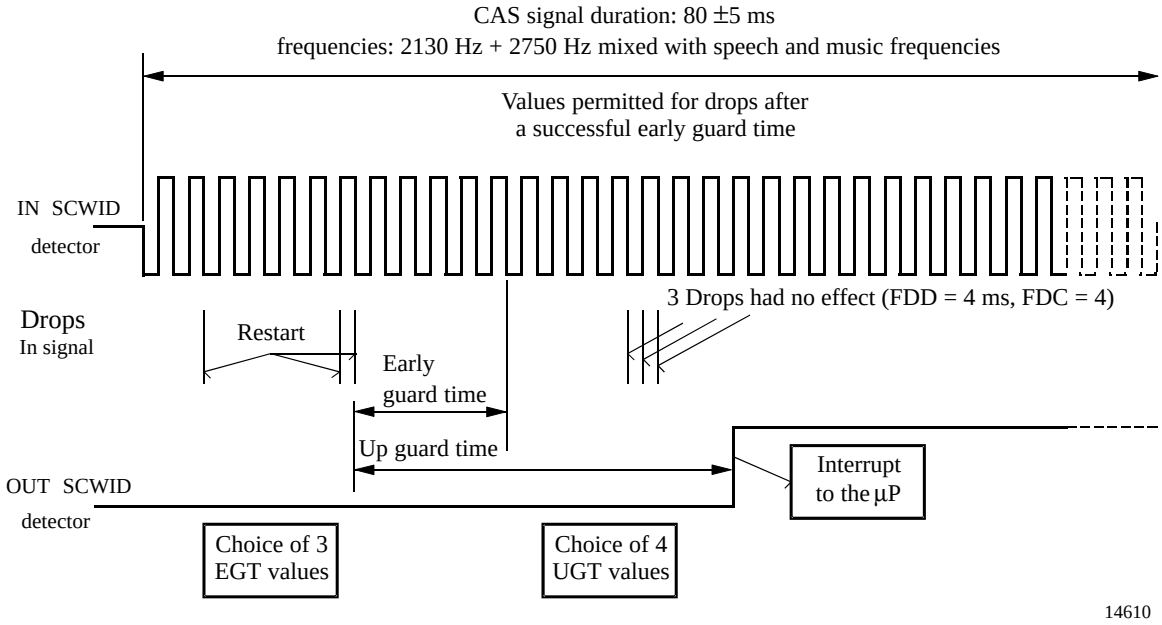


Figure 10. Timing diagram for early and up guard time

Note: In the case above, the EGT counter restarts 3 times. After a sucessful 10.3-ms EGT, 3 drops occured but without any effect because the duration and the number is less than the maximum permitted.

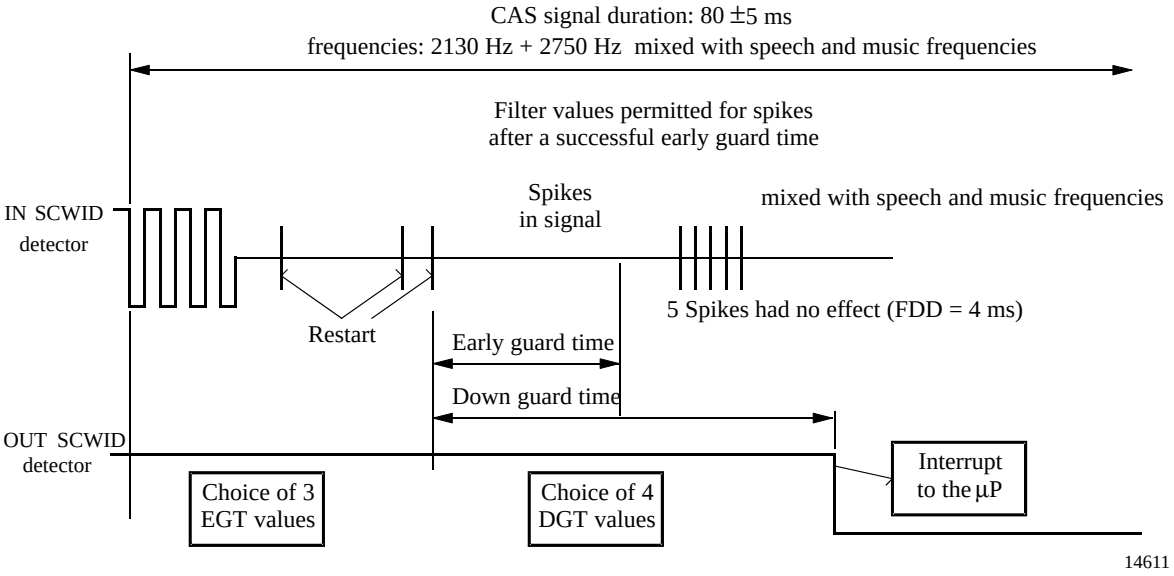


Figure 11. Timing diagram of early and down guard time

Note: In the case above, the EGT counter restarts 3 times. After a sucessful 13.7-ms EGT, 5 spikes occured but without any effect because the duration is less than the maximum permitted.

3 DC Line Interface and Supply-Voltage Generation

The DC line interface consists of an electronic inductance and a dual-port output stage which charges the capacitors at VMPS and VB. The value of the equivalent inductance is given by:

$L = 2 \times R_{SENSE} \times C_{IND} \times (R_{DC} \times R_{30}) / (R_{DC} + R_{30})$

The U3900BM contains two identical series regulators which provide a supply voltage VMP of 3.3 V suitable for a microprocessor. In speech mode, both regulators are active because VMPS and VB are charged simultaneously by the DC-line interface. The output current is 6 mA. The capacitor at VMPS is used to provide the microcomputer with sufficient power during long line interruptions. Thus, long flash pulses can be bridged or an LCD display can be turned on for more than 2 seconds after going on-hook. When the system is in ringing mode, VB is charged by the on–chip ringing power converter. In this mode, only one regulator is used to supply VMP with maximum 3 mA.

3.1 Supply Structure of the Chip

As main benefit of the U3900BM is the easy implementation of various applications due to the flexible system structure of the chip.

Possible applications:

- Group listening phone
- Hands-free phone
- Phones which feature ringing with the built-in speaker amplifier
- Answering machine with external supply

The special supply topology for the various functional blocks is illustrated in figure 11.

There are four major supply states:

1. Speech condition
2. Power down (pulse dialing)
3. Ringing
4. External supply

1. In speech condition, the system is supplied by the line current. If the LIDET-block detects a line voltage above approximately 2 V, the internal signal VLON is activated. This is detected via serial bus, all necessary the blocks have to be switched on via the serial bus.

For line voltages below 2 V, the switches remain in quiescent state as shown in the diagram.

2. When the chip is in power-down mode (Bit LOMAKE), e.g., during pulse dialing, all internal blocks are disabled via the serial bus, except the oscillator. In this condition, the voltage regulators and their internal bandgap are the only active blocks.
3. During ringing, the supply for the system is fed into VB via the **R**inging **P**ower **C**onverter (RPC). Normally, the speaker amplifier in single-ended mode is used for ringing. The frequency for the melody is generated by the DTMF/Melody generator.
4. In an answering machine, the chip is powered by an external supply via Pin VB. The answering machine connections could be directly put to U3900BM. The answering machine is connected to the Pin AMREC. For the output AMREC, an AGC function is selectable via the serial bus. The output of the answering machine will be connected to the Pin AMPB, which is directly connected to the switching matrix, and thus enables the signal to be switched to every desired output.

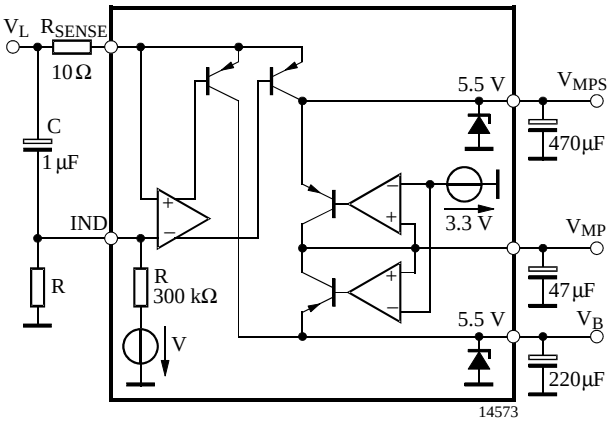


Figure 12. Supply generator

4 Ringing Power Converter (RPC)

The RPC transforms the input power at VRING (high voltage/ low current) into an equivalent output power at VB (low voltage/ high current) which is capable of driving the low-ohmic loudspeaker. The input impedance at VRING is adjustable from 3 kΩ to 12 kΩ by RIMPA (ZRING = RIMPA / 100) and the efficiency of the step-down converter is approximately 65%.

4.1 Ringing Frequency Detector (RFD)

The U3900BM provides an output signal for the microcontroller. This output signal is always double the value of the input signal (ringing frequency). It is generated by a current comparator with hysteresis. The levels for the on-threshold are programmable in 16 steps and the off-level is fixed. Every change of the comparator output generates a high level at the interrupt output INT. The information can then be read out by means of a serial bus with either a normal or a fast read mode. The block RFD is always enabled.

RINGTH[0:3]	VRING
min. 0	7 V
max. 15	22 V
step	1 V

5 Clock Output Divider Adjustment

The Pin OSCOUT is a clock output which is derived from the crystal oscillator of the ceramic resonator. It can be used to drive a microcontroller or another remote component and thereby reduces the number of crystals required. The oscillator frequency can be divided by 1, 8, 16, 32. During power-on reset, the divider will be reset to 1 until it is changed by setting the serial bus.

CLK[0:1]	Divider	Frequency
0	1	3.58 MHz
1	8	447 kHz
2	16	224 kHz
3	32	112 kHz

6 Serial Bus Interface

The circuit is controlled by an external microcontroller through the serial bus. The serial bus is a bi-directional system consisting of a one-directional clock line (BCL) which is always driven by the microcontroller, and a bi-directional data-signal line. It is driven by the microcontroller as well as from the U3900BM (see figure 12). The serial bus requires external pull-up resistors as only open-collector transistors (Pin BDA) are integrated.

WRITE: The data is a 12-bit word:

A0 – A3: address of the destination register (0 to 15)

D0 – D7: content of the register

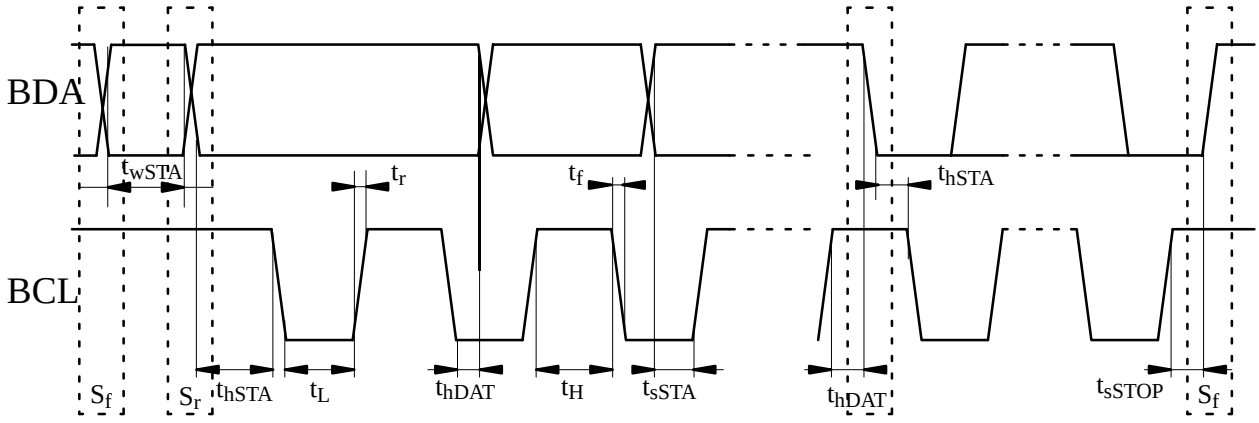
The data line must be stable when the clock is high. Data must be shifted serially.

After 12 clock periods, the write indication is sent. Then, the transfer to the destination register is (internally) generated by a strobe signal transition of the data line when the clock is high (see figure 13).

READ:
There is a normal and a fast-read cycle.
In the normal read cycle, the microcontroller sends a 4-bit address followed by the read indicator, then an 8-bit word is read out. The U3900BM drives the data line (see figure 14).

The fast read cycle is indicated by a strobe signal. With the following two clocks the U3900BM reads out the status bits RFDO and LIDET which indicate that a ringing signal or a line signal is present (see figure 15).

6.1 Bus Timing



S_f = Strobe falling, S_R = Strobe rising

Figure 13. Bus timing

7 DTMF Dialing

The DTMF generator sends a multi-frequency signal through the matrix to the line. The signal is the result of the sum of two frequencies and is internally filtered. The frequencies are chosen from a low and a high frequency group.

The circuit conforms to the CEPT recommendation concerning DTMF option (rec. T/CF 46–03).

Two different levels for the low level group and two different preemphasis (2.5 dB and 3.5 dB) can be chosen by means of the serial bus.

7.1 Melody – Confidence Tone Generation

Melody/confidence tone frequencies are given in the table below.

The frequencies are provided at the DTMF input of the switch matrix. A sinus wave, a square wave or a pulsed wave can be selected by the serial bus. Square signal means output is half of frequency cycle high and half low, so duty cycle of 50% square wave or 50% for pulsed signal.

	DTMFM[0:2]	
0	000	DTMF generator OFF
1	001	Confidence tone melody on (sinus)
2	010	Ringer melody (pulse)
3	011	Ringer melody (square signal)
4	100	DTMF(high level)
5	101	DTMF(low level)
6	110	
7	111	

	DTMFF[0:1] in DTMF Mode	Frequency	Error / %
0	00	697	–0.007
1	01	770	–0.156
2	10	852	0.032
3	11	941	0.316

	DTMFF[2:3] in DTMF Mode	Frequency	Error / %
0	00	1209	–0.110
1	01	1336	0.123
2	10	1477	–0.020
3	11	1633	–0.182

DTMFF4 in DTMF mode

Preemphasis Selection	
0	2.5 dB
1	3.5 dB

	DTMFF [0:4]	f Hz	Tone-Name	Error/%	DTMF		Key
0	00000	440.0	a^1	–0.008	697	1209	1
1	00001	466.2	b^1	–0.016	770	1209	4
2	00010	493.9	h^1	–0.003	852	1209	7
3	00011	523.2	c^2	0.014	941	1209	*
4	00100	554.4	des^2	0.018	697	1336	2
5	00101	587.3	d^2	–0.023	770	1336	5
6	00110	622.3	es^2	–0.129	852	1336	8
7	00111	659.3	e^2	0.106	941	1336	0
8	01000	698.5	f^2	–0.216	697	1477	3
9	01001	740.0	ges^2	–0.222	770	1477	6
10	01010	784.0	g^2	0.126	852	1477	9
11	01011	830.0	as^2	–0.169	941	1477	#
12	01100	880.0	a^2	0.288	697	1633	A
13	01101	932.3	b^2	–0.014	770	1633	B
14	01110	987.8	h^2	–0.004	852	1633	C
15	01111	1046.5	c^3	–0.335	941	1633	D
16	10000	1108.7	des^3	–0.355	697	1209	1
17	10001	1174.7	d^3	–0.023	770	1209	4
18	10010	1244.5	es^3	–0.129	852	1209	7
19	10011	1318.5	e^3	0.106	941	1209	*
20	10100	1396.9	f^3	–0.214	697	1336	2
21	10101	1480.0	ges^3	–0.222	770	1336	5
22	10110	1568.0	g^3	0.126	852	1336	8
23	10111	1661.2	as^3	–0.241	941	1336	0
24	11000	1760.0	a^3	–0.302	697	1477	3
25	11001	1864.6	b^3	–0.014	770	1477	6
26	11010	1975.5	h^3	0.665	852	1477	9
27	11011	2093.0	c^4	0.367	941	1477	#
28	11100	2217.5	des^4	0.387	697	1633	A
29	11101	2349.3	d^4	0.771	770	1633	B
30	11110	2663.3		—	852	1633	C
31	11111	2983.0		—	941	1633	D

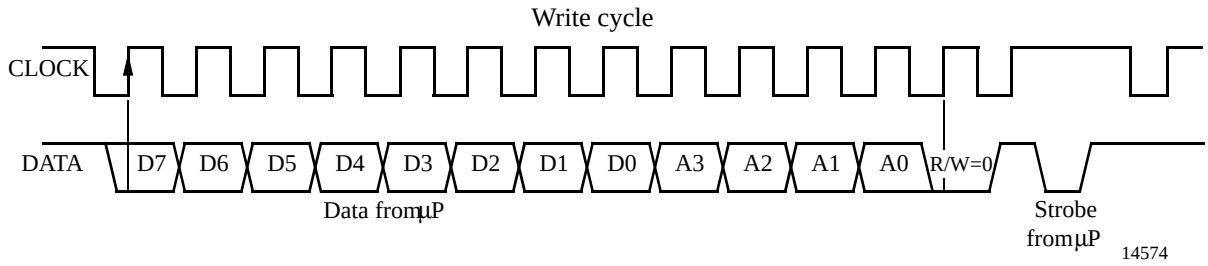


Figure 14. Write cycle

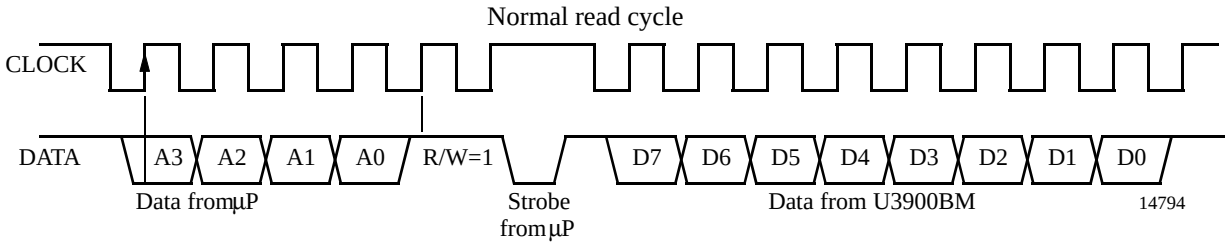


Figure 15. Normal read cycle

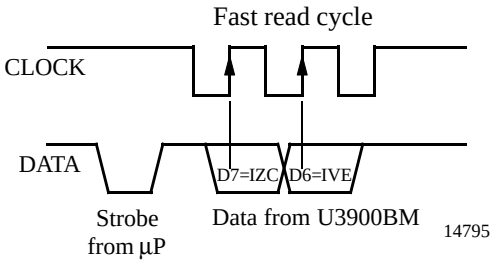


Figure 16. Fast read cycle

Table 1. Names and functions of the serial bus registers

Register	Group	No	Name	Description	Status	
R0	Enables	R0B0	ENRING	Enable ringer		1
		R0B1	ERX	Enable receive part	0	
		R0B2	ETX	Enable transmit part	0	
		R0B3	ENVM	Enable VM generator		1
		R0B4	ENMIC	Enable microphone	0	
		R0B5	ENSTBAL	Enable sidetone balancing	0	
		R0B6	MUTE	Muting earpiece amplifier	0	
		R0B7	ENRLT	Enable POR low threshold		1
R1	Enables	R1B0	ENSACL	Enable anti-clipping for speaker amplifier	0	
		R1B1	ENSA	Enable speaker amplifier and AFS	0	
		R1B2	ENSAO	Enable output stage speaker amplifier	0	
		R1B3	ENAM	Enable answering machine connections	0	
		R1B4	ENCT	Enable cordless telephone connections	0	
		R1B5	ANAMAGC	Enable answering machine AGC	0	
		R1B6	ENCLID	Enable CLID	0	
		R1B7	ENSCWID	Enable SCWID	0	
R2	Matrix	R2B0	I1O1	Switch on MIC / LTX	0	
		R2B1	I1O2	Switch on MIC / RXLS	0	
		R2B2	I1O3	Switch on MIC / EPO	0	
		R2B3	I1O4	Switch on MIC / CEAR	0	
		R2B4	I1O5	Switch on MIC / AMREC	0	
		R2B5	I2O1	Switch on DTMF / LTX	0	
		R2B6	I2O2	Switch on DTMF / RXLS	0	
		R2B7	I2O3	Switch on DTMF / EPO	0	
R3	Matrix	R3B0	I2O4	Switch on DTMF / CEAR	0	
		R3B1	I2O5	Switch on DTMF / AMREC	0	
		R3B2	I3O1	Switch on LRX / LTX	0	
		R3B3	I3O2	Switch on LRX / RXLS	0	
		R3B4	I3O3	Switch on LRX / EPO	0	
		R3B5	I3O4	Switch on LRX / CEAR	0	
		R3B6	I3O5	Switch on LRX / AMREC	0	
		R3B7	I4O1	Switch on CMIC / LTX	0	
R4	Matrix	R4B0	I4O2	Switch on CMIC / RXLS	0	
		R4B1	I4O3	Switch on CMIC / EPO	0	
		R4B2	I4O4	Switch on CMIC / CEAR	0	
		R4B3	I4O5	Switch on CMIC / AMREC	0	
		R4B4	I5O1	Switch on AMPB / LTX	0	
		R4B5	I5O2	Switch on AMPB / RXLS	0	
		R4B6	I5O3	Switch on AMPB / EPO	0	
		R4B7	I5O4	Switch on AMPB / CEAR	0	
R5	Matrix	R5B0	I5O5	Switch on AMPB / AMREC	0	
	AGATX	R5B1	AGATX0	Gain transmit AGA LSB	0	
	MICLIM	R5B2	AGATX1	Gain transmit AGA	0	
		R5B3	AGATX2	Gain transmit AGA MSB	0	
		R5B4	MICHF	Select RF-microphone input	0	
		R5B5	DBM5	Max. transmit level for anti-clipping	0	
		R5B6	MIC0	Gain microphone amplifier LSB	0	
		R5B7	MIC1	Gain microphone amplifier MSB	0	

Register	Group	No	Name	Description	Status	
R6	Sidetone	R6B0	FOFFC	Speed up offset canceller	0	
		R6B1	DTAMAGC	Decay time answering machiune AGC	0	
		R6B2	SL0	Slope adjustment for sidetone LSB	0	
		R6B3	SL1	Slope adjustment for sidetone MSB	0	
		R6B4	LF0	Low-frequency adjustment for sidetone LSB	0	
		R6B5	LF1	Low-frequency adjustment for sidetone	0	
		R6B6	LF2	Low-frequency adjustment for sidetone	0	
		R6B7	LF3	Low-frequency adjustment for sidetone MSB	0	
R7	Sidetone AGARX	R7B0	P0	Pole adjustment for sidetone LSB	0	
		R7B1	P1	Pole adjustment for sidetone	0	
		R7B2	P2	Pole adjustment for sidetone	0	
		R7B3	P3	Pole adjustment for sidetone	0	
		R7B4	P4	Pole adjustment for sidetone MSB	0	
		R7B5	AGARX0	Gain receive AGC LSB	0	
		R7B6	AGARX1	Gain receive AGC	0	
		R7B7	AGARX2	Gain receive AGC MSB	0	
R8	EARA PS	R8B0	EA0	Gain earpiece amplifier LSB	0	
		R8B1	EA1	Gain earpiece amplifier	0	
		R8B2	EA2	Gain earpiece amplifier	0	
		R8B3	EA3	Gain earpiece amplifier	0	
		R8B4	EA4	Gain earpiece amplifier MSB	0	
		R8B5	IMPSEL	Line-impedance selection (1 = 1 kΩ)	0	
		R8B6	LOMAKE	Short circuit during pulse dialing	0	
		R8B7	SD	Shut down	0	
R9	AFS	R9B0	AFS0	AFS gain adjustment LSB	0	
		R9B1	AFS1	AFS gain adjustment	0	
		R9B2	AFS2	AFS gain adjustment	0	
		R9B3	AFS3	AFS gain adjustment	0	
		R9B4	AFS4	AFS gain adjustment	0	
		R9B5	AFS5	AFS gain adjustment MSB	0	
		R9B6	AFSM	AFS mode	0	
		R9B7	ALT	Antilarsen threshold	0	
R10	SA	R10B0	SA0	Gain speaker amplifier LSB	0	
		R10B1	SA1	Gain speaker amplifier	0	
		R10B2	SA2	Gain speaker amplifier	0	
		R10B3	SA3	Gain speaker amplifier	0	
		R10B4	SA4	Gain speaker amplifier MSB	0	
		R10B5	SE	Speaker amplifier single-ended mode	0	
		R10B6	LSCUR0	Speaker amplifier charge-current adjustment LSB	0	
		R10B7	LSCUR1	Speaker amplifier charge-current adjustment MSB	0	
R11	ADC	R11B0	ADC0	Input selection ADC	0	
		R11B1	ADC1	Input selection ADC	0	
		R11B2	ADC2	Input selection ADC	0	
		R11B3	ADC3	Input selection ADC	0	
		R11B4	NWT	Network tuning	0	
		R11B5	SOC	Start of ADC conversion	0	
		R11B6	ADCR	Selection of ADC range	0	
		R11B7	MSKIT	Mask for interrupt bits	0	

Register	Group	No	Name	Description	Status	
R12	DTMF	R12B0	DTMFF0	DTMF frequency selection	0	
		R12B1	DTMFF1	DTMF frequency selection	0	
		R12B2	DTMFF2	DTMF frequency selection	0	
		R12B3	DTMFF3	DTMF frequency selection	0	
		R12B4	DTMFF4	DTMF frequency selection	0	
		R12B5	DTMFM0	Generator mode selection	0	
		R12B6	DTMFM1	Generator mode selection	0	
		R12B7	DTMFM2	Generator mode selection	0	
R13	CLK	R13B0	CLK0	Selection clock frequency for µC	0	
	RTH	R13B1	CLK1	Selection clock frequency for µC	0	
	TM	R13B2	RTH0	Ringer threshold adjustment LSB	0	
		R13B3	RTH1	Ringer threshold adjustment	0	
		R13B4	RTH2	Ringer threshold adjustment	0	
		R13B5	RTH3	Ringer threshold adjustment MSB	0	
		R13B6	TME0	Test mode enable (low active)	0	
		R13B7	TME1	Test mode enable (high active)	0	
R14	TM	R14B0	TME2	Test mode enable (high active)	0	
	CLID	R14B1	TME3	Test mode enable (low active)	0	
		R14B2			0	
		R14B3			0	
		R14B4	ENRXCL	Selection of internal CLID input signals	0	
		R14B5	GSCWID	Gain adjustment of SCWID behind sidetone	0	
		R14B6	WP	Wetting pulse	0	
		R14B7			0	
R15	CLID	R15B0	UGT0	SCWID up guard time	0	
		R15B1	UGT1/SCD	SCWID up guard time/ CLIB special carier detect	0	
		R15B2	DGT0/CDLF0	SCWID down guard time/ CLID LF carrier detect	0	
		R15B3	DGT1/CDLF1	SCWID down guard time/ CLID LF carrier detect	0	
		R15B4	EGT0/CDHF0	SCWID early guard time/ CLID HF carrier detect	0	
		R15B5	EGT1/CDHF1	SCWID early guard time/ CLID HF carrier detect	0	
		R15B6	FDD	Filter drop duration	0	
		R15B7	FDC	Filter drops count	0	

8 Power-on Reset

To avoid undefined states of the system when it is powered on, an internal reset clears the internal registers.

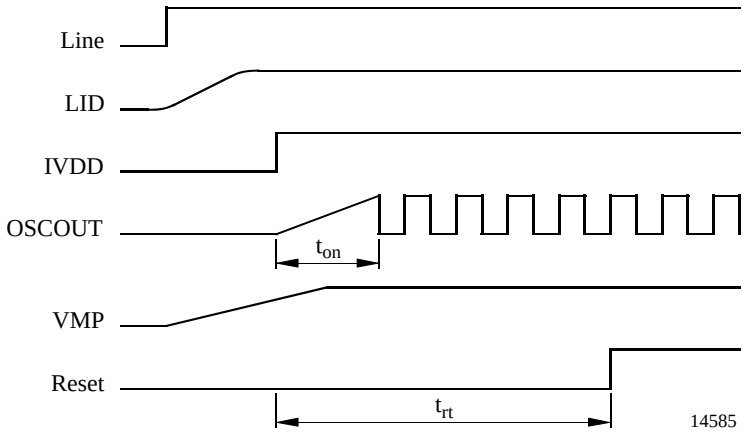
The system (U3900BM + microcontroller) is woken up by any of the following conditions:

VMP > 2.75 V and VB > 2.45 V and
line voltage (VL)
or ringer (VRING)
or external supply (ES)

The power-down of the circuit is caused by a shut-down sent by the serial bus (SD = 1), low-voltage reset or by the watchdog function (see figures 16, 17 and 18).

9 Watchdog Function

To avoid the system operating the microcontroller in a wrong condition, the cicuit provides a watchdog function. The watchdog has to be retriggered every second by triggering the serial bus (sending information to the IC or other remoted components at the serial bus). If there has been no bus transmission for more than one second the watchdog iniates a reset.



$t_{rt} - t_{on}$ = 4.5 ms
t_{on} = start–up oscillator

Figure 17. Power-on reset (line)

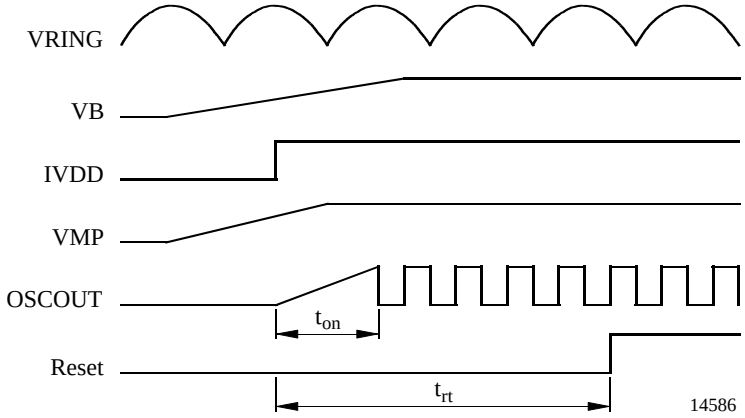


Figure 18. Power-on reset (ringing)

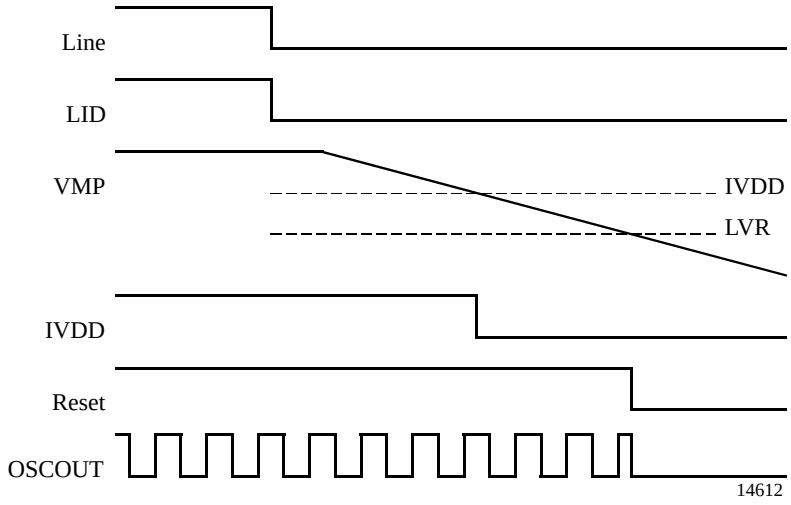


Figure 19. Power-on reset if low voltage reset enabled

10 Acoustic Feedback Suppression

Acoustical feedback from the loudspeaker to the microphone may cause instability of the system. The U3900BM has a very efficient feedback-suppression circuit which uses a modified voice switch topology. Figure 20 shows the basic system configuration.

Two attenuators (TXA and SAI) reduce the critical loop gain via the serial bus either in the transmit or in the receive path. The sliding control in block AFS control (figure 19) determines whether the TX or the RX signal has to be attenuated. The overall loop gain remains constant under all operating conditions.

Selection of the active channel is made by a comparison of the logarithmically compressed TX- and RX- envelope curve. Figure 19 shows the AFS control.

The system configuration for group listening, which is implemented in the U3900BM, is illustrated in figure 21. TXA and SAI represent the two attenuators, whereas the logarithmic envelope detectors are shown in a simplified way (operational amplifiers with two diodes).

Receive and transmit signals are first processed by logarithmic rectifiers in order to produce the envelopes of the speech at TLDT and RLDT. After amplification a decision is made by the differential pair as to which direction should be transmitted.

The attenuation of the controlled amplifiers TXA and SAI is determined by the emitter current IAFS which is bus programmable.

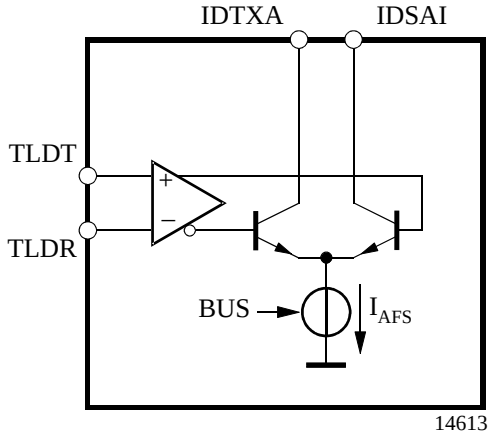


Figure 20. AFS control

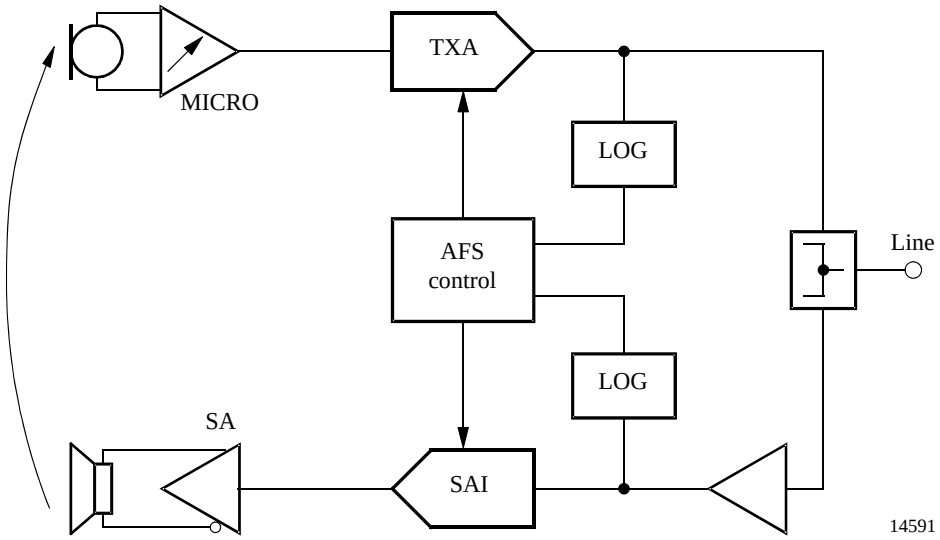


Figure 21. Basic system configurations

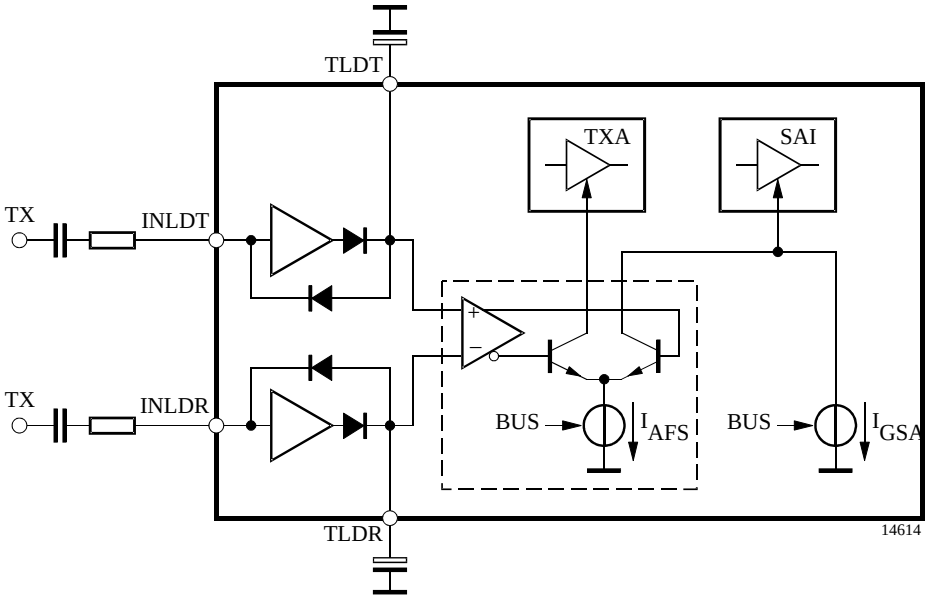


Figure 22. System configuration for group listening

11 Analog-to-Digital Converter (ADC)

The circuit is a 7-bit successive approximation analog-to-digital converter in switched capacitor technique. An internal bandgap circuit generates a 1.25-V reference voltage which is the equivalent of 1 MSB. 1 LSB = 19.5 mV. The possible input voltage at ADIN is 0 to 2.48 V.

The ADC needs an SOC (**S**tart **O**f **C**onversion) signal. In the ‘High’ phase of the SOC signal, the ADC is reset. 50 µs after the beginning of the ‘Low’ phase of the SOC signal the ADC generates an EOC (**E**nd **O**f **C**onversion) signal which indicates that the conversion is finished. The rising edge of EOC generates an interrupt at the INT output. The result can be read out by the serial bus.

Voltages higher than 2.48 V have to be divided. The signal which is connected to the ADC is determined by 5 bits ADC0, ADC1, ADC2, ADC3 and NWT. TLDR/TLDT measuring is possible relative to a preceding reference measurement. The current range of IL can be doubled by ADCR. If ADCR is ‘High’, S has the value 0.5, otherwise S = 1.

The source impedance at ADIN must be lower than 250 kΩ.

Accuracy: 1 LSB ± 3%

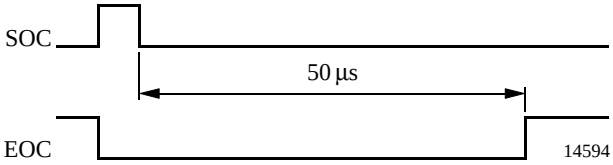


Figure 23. Timing of ADC

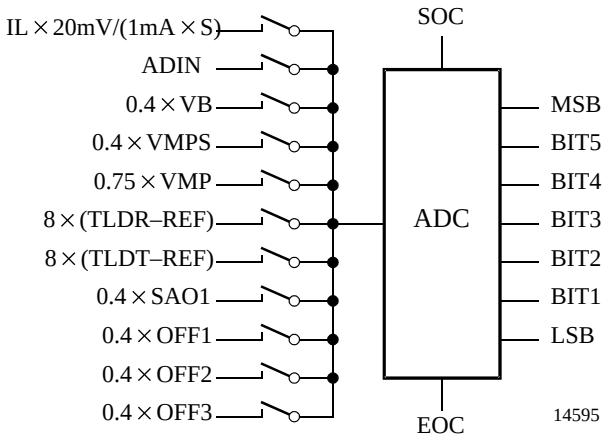


Figure 24. ADC input selection

Table 2. Input selection AD converter

	ADC[0:3]		Value
0	0000	OFF	
1	0001	IL	I1 = S × 127 mA × D / 127
2	0010	ADIN external	V2 = 2.5 V × D / 127 (max. 2.5 V)
3	0011	VB	V3 = (2.5 V / 0.4) × D / 127
4	0100	VMPS	V4 = (2.5 V / 0.4) × D / 127
5	0101	VMP	V5 = (2.5 V / 0.75) × D / 127
6	0110	TLDR	V6 = 1/8 × (Vp – Ref) × D / 127
7	0111	TLDT	V7 = 1/8 × (Vp – Ref) × D / 127
8	1000	Free	
9	1001	SAO1	V4 = (2.5 V / 0.4) × D / 127
10	1010	Offcan1	TEMIC internal use
11	1011	Offcan2	TEMIC internal use
12	1100	Offcan3	TEMIC internal use
13	1101	Free	
14	1110	Free	
15	1111	Free	

D = measured digital word (0 < = D < = 127)
S = programmable gain 0.5 or 1
Vp = peak value of the measured signal

12 Switch Matrix

The switch matrix has 5 inputs and 5 outputs. Every pair of input and output can be connected. The inputs and outputs used must be enabled. If 2 or more inputs are switched to an output, the sum of the inputs is available at the output. The inputs MIC and LRX have offset cancellers with a 3-dB corner frequency of 270 Hz. AMPB and CMIC have a 60-kΩ input impedance. The TXO output has a digitally-programmable gain stage with a gain of 2, 3 to 9 dB depending on AGATX0 (LSB), AGATX1, AGATX2 (MSB) and a first-order low-pass filter with 0.5 dB damping at 3300 Hz and 3 dB damping at 9450 Hz. The outputs RXLS, EPO and CEAR have a gain of 0 dB. If a switch is open, the path has a damping of more than 60 dB.

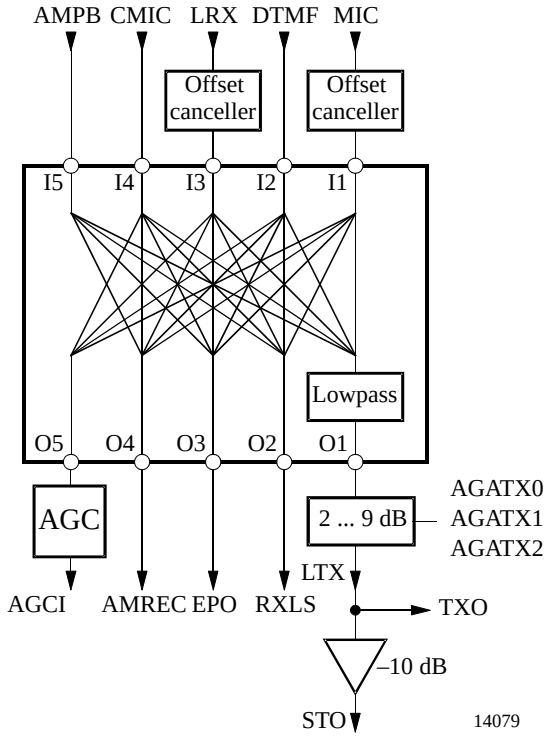


Figure 25. Diagram of switch matrix

Table 3. Table of bits and corresponding switches

Register	Group	No.	Name	Description
R2	Matrix	R2B0	I1O1	Switch on MIC / LTX
		R2B1	I1O2	Switch on MIC / RXLS
		R2B2	I1O3	Switch on MIC / EPO
		R2B3	I1O4	Switch on MIC / CEAR
		R2B4	I1O5	Switch on MIC / AMREC
		R2B5	I2O1	Switch on DTMF / LTX
		R2B6	I2O2	Switch on DTMF / RXLS
		R2B7	I2O3	Switch on DTMF / EPO
R3	Matrix	R3B0	I2O4	Switch on DTMF / CEAR
		R3B1	I2O5	Switch on DTMF / AMREC
		R3B2	I3O1	Switch on LRX / LTX
		R3B3	I3O2	Switch on LRX / RXLS
		R3B4	I3O3	Switch on LRX / EPO
		R3B5	I3O4	Switch on LRX / CEAR
		R3B6	I3O5	Switch on LRX / AMREC
		R3B7	I4O1	Switch on CMIC / LTX
R4	Matrix	R4B0	I4O2	Switch on CMIC / RXLS
		R4B1	I4O3	Switch on CMIC / EPO
		R4B2	I4O4	Switch on CMIC / CEAR
		R4B3	I4O5	Switch on CMIC / AMREC
		R4B4	I5O1	Switch on AMPB / LTX
		R4B5	I5O2	Switch on AMPB / RXLS
		R4B6	I5O3	Switch on AMPB / EPO
		R4B7	I5O4	Switch on AMPB / CEAR
R5	Matrix	R5B0	I5O5	Switch on AMPB / AMREC

13 Sidetone System

The **S**idetone **B**alancing (STB) has the task to reduce the crosstalk from LTX (microphone) to LRX (earpiece) in the frequency range of 0.3 to 3.4 kHz. The LTX signal is converted into a current in the MOD block. This current is transformed into a voltage signal (LINE) by the line impedance ZL. The LINE signal is fed into the summing amplifier DIFF1 via capacitor CK and attenuator AMP1.

On the other side the LTX buffered by STOAMP drives an external low-pass filter (RST, CST). The external low-pass filter and the internal STB have the transfer function drawn in the STB box. The amplified STB-output signal drives the negative input of the summing block. If both signals at the DIFF1 block are equal in level and phase, we have a good suppression of the LTX signal. In this condition the frequency and phase response of the STB block will represent the frequency curve on line.

In real live the line impedance ZL varies strongly for different users. To reach a good suppression with one application for all different line impendances, the STB function is programmable.

The 3 programmable parameters are

1. LF (gain at low frequency).
   LF has 15 programming steps. LF(0) gives –2 dB gain, LF(15) gives 5.5 dB gain.

LF	0	1	2	3	4	5	6	7
Step gain	–2	–1.3	–0.6	0.1	0.6	1.0	1.3	1.6

LF	8	9	10	11	12	13	14	15
Step gain	1.9	2.2	2.5	3.0	3.6	4.2	4.8	5.5

$STO\_DIFF(LF) = (-10\,dB - 2\,dB + 0.5\,dB \times LF + 9\,dB) \times LTX$

2. P (the pole position of the lowpass).
   The P adjustment has 31 Steps. P(0) means the lowpass determined by the external application (RST, CST). The internally processed low-pass frequency is fixed by this equation.

$$f(P) = \frac{1}{2 \times \pi \times CST \times RST} \times 1.122^{P}$$

3. SL
   (sidetone slope; the pole frequency of the highpass)
   The SL have 3 steps. SL(0) is a lower frequency of the highpass. SL(3) is a higher frequency of the highpass. With SL we can influence the suppression at high frequencies.

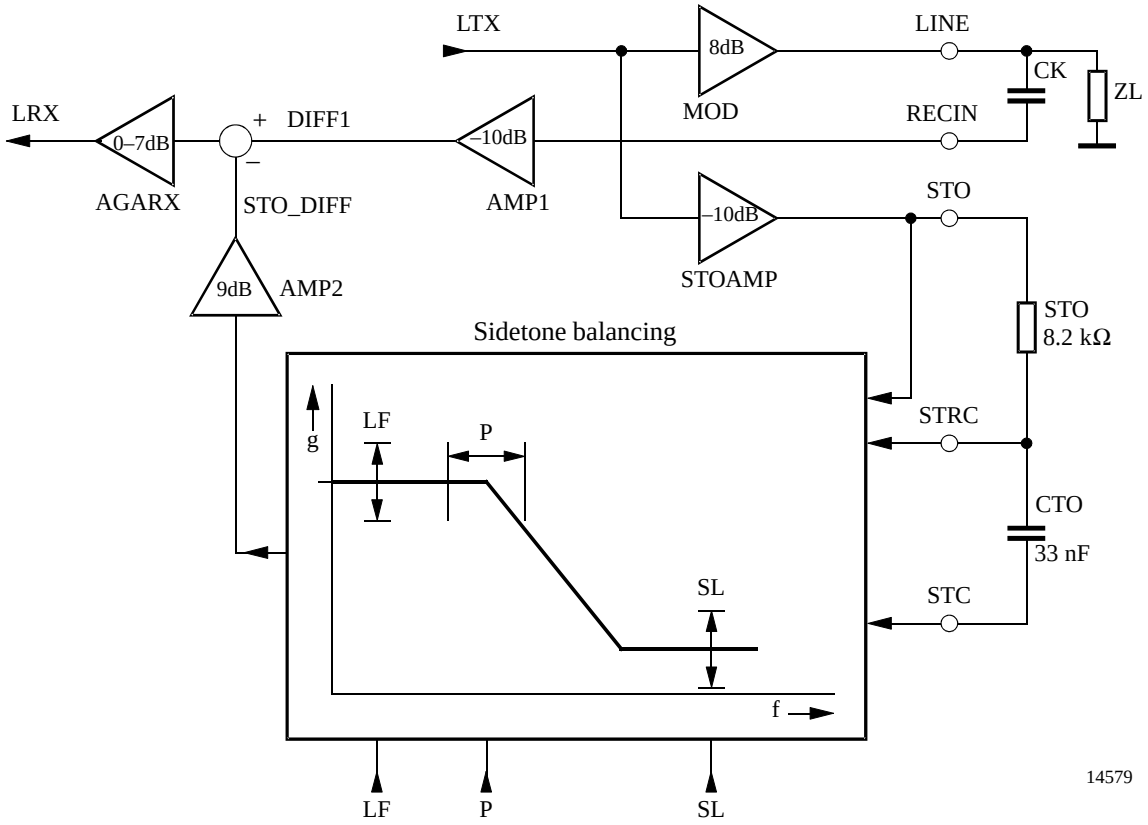


Figure 26. Programmable sidetone supression circuit

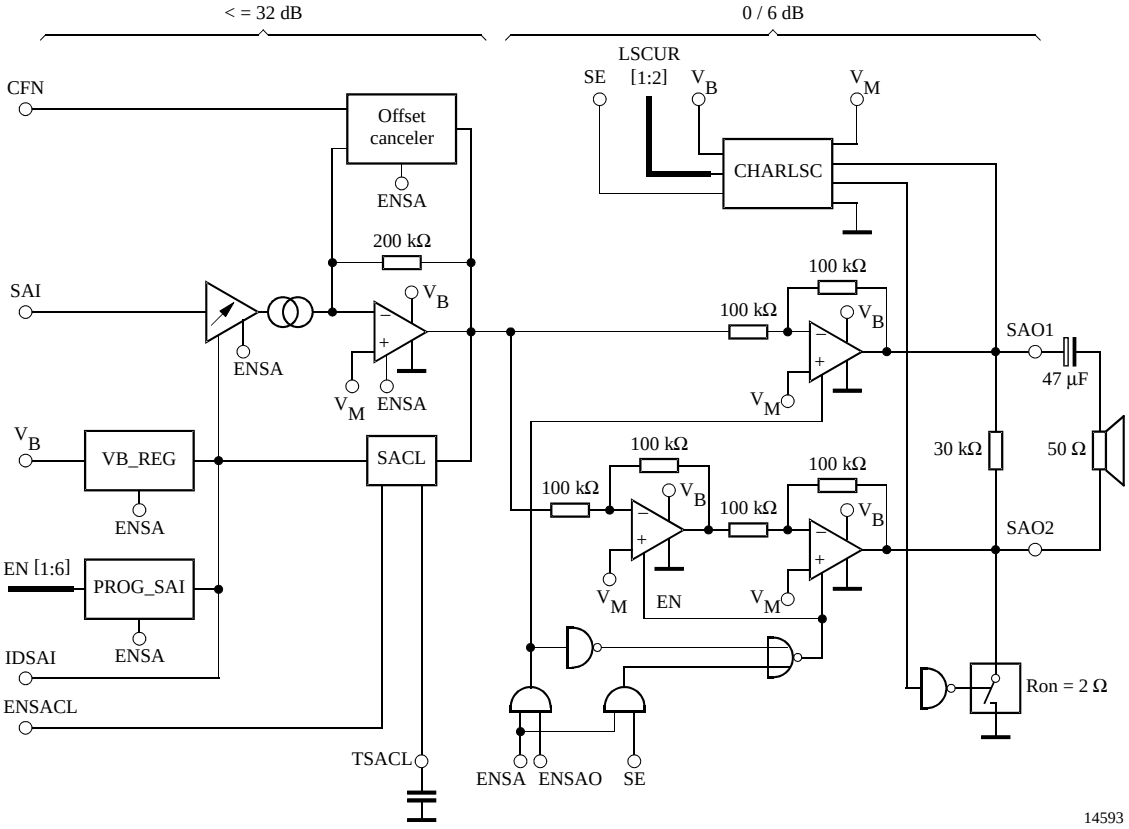


Figure 27. Speaker amplifier

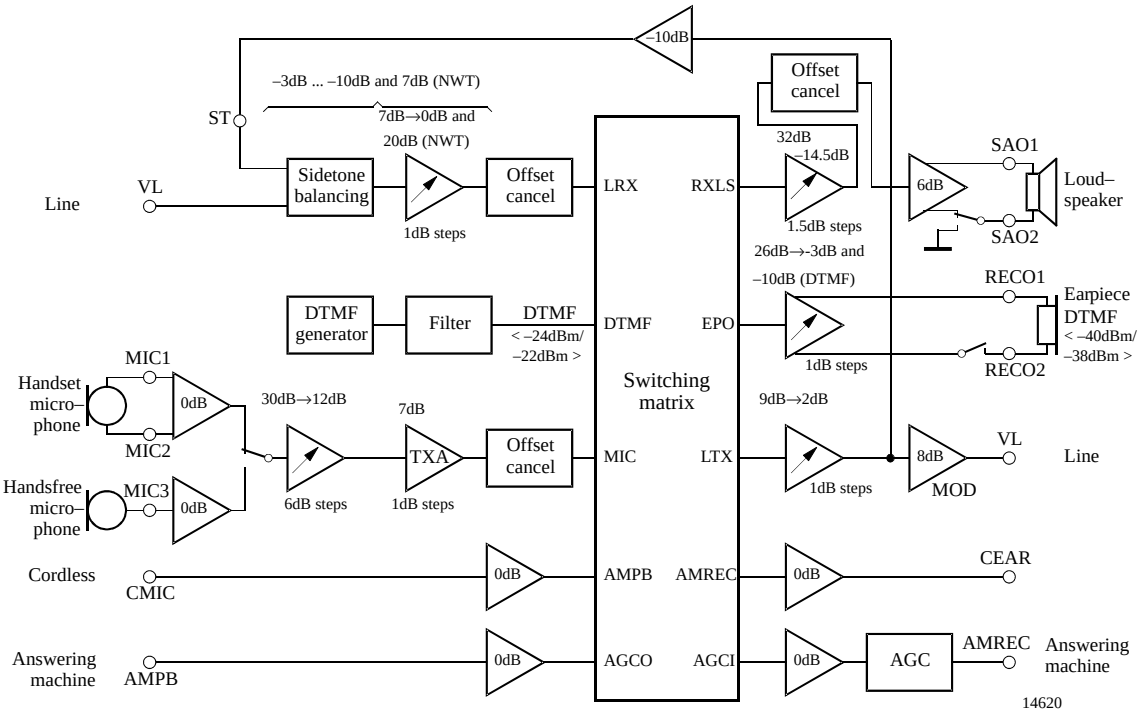


Figure 28. Audio frequency signal management U3900BM

14 Technical Data

14.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Line current	I_L	140	mA
DC line voltage	V_L	12	V
Maximum input current	I_{RING}	15	mA
Junction temperature	T_j	125	°C
Ambient temperature	T_{amb}	–25 to +75	°C
Storage temperature	T_{stg}	–55 to +150	°C
Total power dissipation, T_{amb} = 60°C	P_{tot}	0.9	W

14.2 Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO44	R_{thJA}	70	K/W

14.3 Electrical Characteristics

f = 1 kHz, 0 dBm = 775 mV_{rms}, IVMIC = 0.3 mA, IMP = 3 mA, R_{DC} = 1.3 MΩ, T_{amb} = 25°C, Z_{ear} = 68 nF + 100 Ω, Z_M = 68 nF, f = 3.58 MHz, all bits in reset condition, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
DC characteristics							
DC voltage drop-over circuit	I_L = 2 mA I_L = 14 mA I_L = 60 mA I_L = 100 mA	V_L	 4.6 8.8	2.4 5.0 7.5 9.4	 5.4 10.0	V	
Transmission amplifier, I_L = 14 mA, V_{MIC} = 2 mV_{RMS}, MICG[0:1] = 2, AGATX[0:2] = 7 ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, (G_T = 48 dB)							
Transmit amplification	MICG[0:1] = 2 AGATX[0:2] = 7	G_T	46	47	48	dB	
Frequency response (see note 1)	$I_L \geq$ 14 mA, f = 3.4 kHz	ΔG_T	–1		0	dB	
Gain change with current	I_L = 14 to 100 mA	ΔG_T			±0.5	dB	
Gain deviation	T_{amb} = –10 to +60°C	ΔG_T			±0.5	dB	
CMRR of microphone amplifier		CMRR	60	80		dB	
Input resistance of MIC amplifier		R_i		50		kΩ	
Input resistance of MIC3 amplifier	MICHF = 1	R_i	75	150	300	kΩ	
Gain difference between MIC1, MIC2 to MIC3	MICHF = 1	ΔG_T			±0.4	dB	
Distortion at line	$I_L \geq$ 14 mA V_L = 700 mV_{rms}	d_t			2	%	

Note 1) Frequency response is due to internal filters

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Maximum output voltage	$I_L \geq 19$ mA, d < 5% V_{MIC} = 10 mV CTXA = 1 µF DBM5 = 0	V_{Lmax}	1.3	2.5	3.7	dBm	
	DBM5 = 1, V_{MIC} = 14 mV	V_{Lmax}	3.8	5.0	6.2	dBm	
	V_{MIC} = 20 mV MICG[0:1] = 3	$V_{MICOmax}$		–5.2		dBm	
Noise at line psophometrically weighted	$I_L \geq 14$ mA MICG[0:1] = 2 AGATX[0:2] = 7	no		– 80	– 72	dBmp	
Anti-clipping: attack time release time	CTXA = 1 µF each 3 dB overdrive	 t_a t_r		 0.5 16		 ms ms	
Gain at low operating current	I_L = 8 mA I_{MP} = 1 mA R_{DC} = 680 kΩ V_{MIC} = 0.5 mV I_{VMIC} = 300 µA	G_T	46.5		49.5	dB	
Distortion at low operating current	I_L = 8 mA I_{MP} = 1 mA R_{DC} = 680 kΩ V_{MIC} = 5 mV I_{VMIC} = 300 µA	d_t			5	%	
Receiving amplifier **I_L = 14 mA, V_{GEN} = 300 mV,** **ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, SL[0:1] = 0, LF[0:3] = 1, P[0:4] = 31,** **AGARX[0:2] = 0**							
Adjustment range of receiving gain	Single ended, $I_L \geq 14$ mA, Mute = 1, EA[0:4] = 2 – 31 AGARX[0:2] = 0 – 7	G_R	–25		11	dB	
Receiving amplification	Differential AGARX[0:2] = 0 EA[0:4] = 21 EA[0:4] = 31	 G_R	 –1 10	 0 11	 1 12	 dB dB	
Frequency response	$I_L \geq 14$ mA, f = 3.4 kHz	ΔG_{RF}	–1		0	dB	
Gain change with current	I_L = 14 to 100 mA	ΔG_R			±0.5	dB	
Gain deviation	T_{amb} = –10 to +60°C	ΔG_R			±0.5	dB	
Ear protection differential	$I_L \geq 14$ mA, V_{GEN} = 11 V_{rms}	EP			3	V_{rms}	
MUTE suppression	I_L = 14 mA	ΔG_R	60			dB	
Output voltage d < 2% differential	I_L = 14 mA Z_{ear} = 68 nF + 100 Ω EA[0:4] = 11		tbd.			V_{rms}	
Maximum output current d < 2%	Z_{ear} = 100 Ω EA[0:4] = 31		10			mAp	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Receiving noise psophometrically weighted	I_L = 14 mA Z_{ear} = 68 nF + 100 Ω EA[0:4] = 21			– 80	– 77	dBmp	
Sidetone suppression	Z = 600 Ω		20			dB	
Output resistance	Each output against GND	Ro			10	Ω	
Gain at low operating current (receive only)	I_L = 5 mA, I_{MP} = 1 mA I_M = 300 µA V_{GEN} = 200 mV R_{DC} = 680 kΩ, EA[0:4] = 21, ENMIC = ETX = I101 = 0	G_R	–2	0	2	dB	
AC impedance	IMPH = 0 IMPH = 1	Z_{imp} Z_{imp}	570 950	600 1000	640 1050	Ω Ω	
Distortion at low operating current	I_L = 8 mA, I_{MP} = 1 mA V_{GEN} = 400 mV R_{DC} = 680 kΩ EA[0:4] = 21	dR			5	%	
Adjustment step: ear-piece amplifier	AGARX[0:4] = 1		0.8	1	1.2	dB	
Adjustment step: AGARX	EA[0:4] = 1		0.8	1	1.2	dB	
Gain for DTMF signal	AMPB → RECO1/2 EA[0:4] = 1			 –16		 dB	
DTMF, I_L = 14 mA, ETX = I201 = 1, AGATX[0:2] = 7, DTMFM[0:2] = 4, DTMFF[0:2] = 0							
Max. level at line	Sum level, 600 Ω, DTMFM[0:2] = 5		–5.1	–3.6	–2.1	dBm	
DTMF level at line (low gain)	Sum level, 600 Ω, DTMFM[0:2] = 4		–7.6	–6.1	–4.6	dBm	
Preemphasis	600 Ω, DTMFF4 = 0 DTMFF4 = 1		2 3	2.5 3.5	3 4	dBm dBm	
Speaker amplifier, differential mode **AMPB → SAO1/2** **ENSACL = ENSA = ENSAO = ENAM = I5O2 = 1, SA[0:4] = 0**							
Minimum line current for operation	No AC signal	I_{Lmin}			8	mA	
Gain from AMPB to SAO	V_{AMPB} = 3 mV, I_L = 15 mA, SA[0:4] = 31 SA[0:4] = 0	G_{SA}	37	38 –8.5	39	dB	
Adjustment step speaker amplifier	ΔSA[0:4] = –1		1.3	1.5	1.7	dB	
Output power single ended	Load resistance: R_L = 50 Ω, d < 5% V_{AMPB} = 20 mV, SE = 1 I_L = 15 mA I_L = 20 mA	 P_{SA} P_{SA}	 3	 7 20		 mW mW	
Max. output power differential	Load resistance: R_L = 50 Ω, d < 5% V_{AMPB} = 20 mV, SE = 0 V_B = 5 V	P_{SA}		200		mW	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Output noise (input AMPB open) psophometrically weighted	I_L > 15 mA	n_{SA}			240	μV_{psoph}	
Gain deviation	I_L = 15 mA T_{amb} = –10 to +60°C	ΔG_{SA}			±1	dB	
Mute suppression	I_L = 15 mA, V_L = 0 dBm, V_{AMPB} = 4 mV, I5O2 = 0	VSAO	60			dB	
Gain change with current	I_L = 15 to 100 mA	ΔG_{SA}			±1	dB	
Gain change with frequency	I_L = 15 mA f = 3.4 kHz	ΔG_{SA}	–1		0	dB	
Attack time of anti-clipping	20 dB over drive	t_r		5		ms	
Release time of anti-clipping		t_f		80		ms	
Charge current Pin SAO2	ENSAO = 0, SE = 1 LSCUR[0:1] = 3	I_{CHA}	–1.45	–1.2	–0.95	mA	
Discharge current Pin SAO2	ENSAO = 0, SE = 0 LSCUR[0:1] = 3	I_{DIS}	0.95	1.2	1.45	mA	
Adjustment step of charge current	ENSAO = 0, SE = 1 ΔLSCUR[0:1] = 1		–480	–400	–320	µA	
Adjustment step of discharge current	ENSAO = 0, SE = 0 ΔLSCUR[0:1] = 1		320	400	480	µA	
Microphone amplifier, V_B = 5 V, V_{MIC} = 2 mV, V_{MIC3} = 2 mV, ENMIC = ENCT = I1O4 = 1, MICHF = 0							
Gain MIC Amp.: MIC1/2 → CEAR	MICG[0:1] = 0		18.4	19	19.6	dB	
	MICG[0:1] = 1		24.4	25	25.6	dB	
	MICG[0:1] = 2		30.4	31	31.6	dB	
	MICG[0:1] = 3		36.4	37	37.6	dB	
MIC3 → CEAR	MICHF = 1, MICG[0:1] = 3		36.4	37	37.6	dB	
Input suppression: MIC3 → MIC1/2	MICG[0:1] = 3, MICHF = 0		60			dB	
MIC1/2 → MIC3	MICHF = 1		60			dB	
Settling time offset-cancellers, 5 τ	FOFFC = 0			9	12	ms	
Settling time offset-cancellers in speed-up mode, 5 τ	FOFFC = 1			1.8	2.4	ms	
AGC for answering machine, AMPB → AMREC, ENAM = I5O5 = 1							
Nominal gain	V_{AMPB} = 5 mV		–1	0	1	dB	
Max. output level	V_{AMPB} = 50 mV, d< 5%		160	200	240	mVp	
Attack time	20 dB overdrive			2		ms	
Release time				100		ms	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Switching matrix, VL = 0, VB = 5 V, ENCT =ENAM = I4O4 = I5O4 = 1, V_{AMPB} = V_{CMIC} = 1 V_{rms}							
Input impedance AMPB, CMIC			50	60	70	kΩ	
Gain CMIC → CEAR, AMREC → CEAR			–0.4	0	0.4	dB	
Max. input level AMPB, CMIC					600	mV	
Max. output level CEAR					VB– 600 mV	V_{PP}	
Offset	I4O4: 1 → 0	ΔV_{AMREC}			±30	mV	
Mute switching matrix	I4O4 = 0		60			dB	
Power-on reset VL = 0, V_{MP} = 3.3 V, V_B = 5 V, U3900BM in power-down mode							
Power-on reset by V_{MP} threshold, VL or V_{RING} or ES high	V_B = 4 V, ES = 4 V, rise VMP	VMPon	2.65	2.75	2.85	V	
Power-on reset by V_B threshold, V_L or V_{RING} or ES high	V_{MP} = 3 V, ES = 3 V, rise V_B	VBon	2.85	2.95	3.05	V	
Low voltage interrupt V_L = 0, V_{MP} = 3.3 V, V_B = 0 V							
VMP decreasing	Decrease VMP until INT returns to high	VLVI	2.5	2.6	2.7	V	
Power-off reset V_L = 0, V_{MP} = 3.3 V, V_B = 0 V							
Low voltage reset	Decrease VMP until RESET returns to low	VLVR	2.35	2.45	2.55	V	
Difference voltage between low voltage interrupt and reset	VLVI – VLVR		100	150		mV	
Logical part V_{MP} = 3.3 V, V_B = 5 V							
Output impedance at OSCOUT			0.5		1.0	kΩ	
Pins BCL, BDA (input mode) Input leakage current	Low level High level $0 < V_i < V_{MP}$		 $0.8 \times V_{MP}$ –1		$0.2 \times V_{MP}$ 1	V V µA	
Pins INT, BDA (output mode)	Output low (resistance to GND)		220	310	400	Ω	
AFS acoustic feedback suppression, I_L = 14 mA, V_{GEN} = 300 mV, ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, SL[0:1] = 0, LF[0:3] = 1, P[0:4] = 31, AGARX[0:2] = 0							
Adjustment range of attenuation	$I_L \geq 15$ mA		0		50	dB	
Attenuation of transmit gain	$I_L \geq 15$ mA, I_{INLDT} = 0 µA I_{INLDR} = 10 µA	ΔG_T	48	50	52	dB	
Attenuation of speaker amplifier	$I_L \geq 15$ mA, I_{INLDT} = 10 µA I_{INLDR} = 0 µA	G_{SA}	48	50	52	dB	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Supply voltages, V_{MIC} = 25 mV, T_{amb} = – 10 to + 60°C							
V_{MP}	I_L = 14 mA, R_{DC} = 680 kΩ I_{MP} = 3 mA	V_{MP}	3.1	3.3	3.5	V	
V_{MPS}	I_L = 100 mA, R_{DC} = inf., I_{MP} = 0 mA	V_{MPS}			5.7	V	
V_{MIC}	I_L 14 mA, R_{DC} = 1.3 MΩ I_M = 700 A	V_{MIC}	1.5		4	V	
V_B	I_B = +20 mA, I_L = 0 mA VL = 100 mA	V_B		5.5	6.3	V	
Ringing power converter, I_{MP} = 1 mA, I_M = 0 R_{IMPA} = 500 kΩ							
Maximum output power	V_{RING} = 20.6 V, DTMFM[0:2] = 3 I2O2 = ENSA = ENSAO = SE = 1	P_{SA}		20		mW	
Threshold	V_{RING}: high to low			6.5	7	V	
	low to high RINGTH [0:3] = 0		6.3	7	7.7	V	
	low to high RINGTH [0:3] = 15		20	22	24	V	
Adjustment steps threshold	ΔRINGTH = 1		0.8	1	1.2	V	
Input impedance	V_{RING} = 30 V		4	5	6	kΩ	
Z-diode voltage	I_{RING} = 25 mA	$V_{RINGmax}$	30.8			V	
Serial bus BCL, BDA, AS, VMP = 3.3 V, RBDA = RBCL = RINT = 12 kΩ							
Input voltage HIGH LOW	BDA, BCL, INT	V_{iBUS}	 3.0 0		 V_{DD} 1.5	 V V	
Output voltage Acknowledge LOW	BDA I_{BDA} = 3 mA	V_O			 0.4	 V	
Clock frequency	BCL	f_{BCL}			100	kHz	
Rise time BDA, BCL		t_r			1	µs	
Fall time BDA, BCL		t_f			300	ns	
Period of BCL HIGH LOW	 HIGH LOW	 t_H t_L	 4.0 4.7			 µs µs	
Setup time							
Start condition Data Stop condition Time space [1]		t_{sSTA} t_{sDAT} t_{sSTOP} t_{wSTA}	4.7 250 4.7 4.7			µs ns µs µs	
Hold time							
Start condition DATA		t_{hSTA} t_{hDAT}	4.0 0			µs µs	

[1] This is a space of time where the bus must be free from data transmission and before a new transmission can be started

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Alert tone detection							
Low tone frequency		f_l		2130		Hz	
High tone frequency		f_h		2750		Hz	
Frequency deviation accept	Range within which tones are accepted		±0.75			%	
Frequency deviation reject	Range within which tones are rejected		±3.5			%	
Accept signal level per tone			37.78		0.22	dBm	
Reject signal level per tone					–43.78	dBm	
Positive and Negative twist accept			7			dBm	
Noise tolerance	Band-limited random noise 300 to 3400 Hz. Present only when tone is present.	SNR TONE	tbd	20	tbd	dB	
Speech tolerance	Speech level is in ASL (**A**ctive **S**peech **L**evel). Over the CAS signal level range –16 dBm to –30 dBm per performance objectives stated in SR-TSV-002476 appendices A&B.		tbd	tbd	tbd	dB	
Tone alert guard time and wetting pulse signal							
Early guard time – 1 – 2 – 3 – 4	Disabled	egt	– 8.3 10.1 13.4	– 8.5 10.3 13.7	– 8.7 10.5 14.0	ms	
Up guard time – 1 – 2 – 3 – 4		ugt	19.5 24.5 29.5 34.5	20 25 30 35	20.5 25.5 30.5 35.5	ms	
Down guard time – 1 – 2 – 3 – 4		dgt	17.5 19.5 21.5 24.5	18 20 22 25	18.5 20.5 22.5 25.5	ms	
Wetting pulse signal delay	Delay after the Alert Signal falling edge	wpd	14.8	15	15.2	ms	

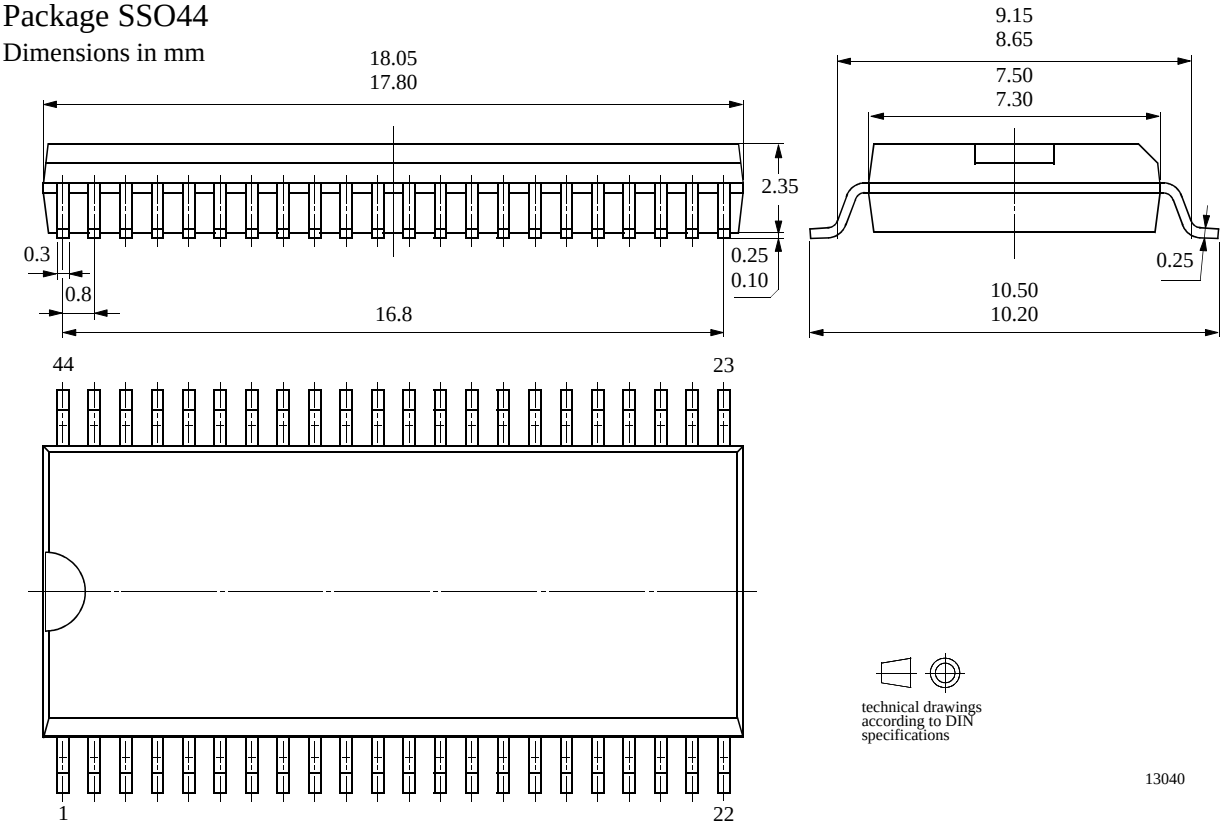
Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
FSK detection							
Input signal power level 1)	On-HOOK mode	Pifon	–38		–1.5	dBm	
Reject signal level (threshold) 2)	On-HOOK mode	Prjon	–44			dBm	
Input signal level 3)	Off-HOOK mode	Pifoff	–38		–1.5	dBm	
Reject signal level (threshold) 2)	Off-HOOK mode	Prjoff	–44			dBm	
Transmission rate (CCITT V23 & BELL 202)		T_r	1188	1200	1212	baud	
Space frequency (CCITT V23)		SfV	2079	2100	2121		
Mark frequency (CCITT V23)		MfV	1287	1300	1313		
Space frequency (BELL 202)		SfB	1178	2200	2222		
Mark frequency (BELL 202)		MfB	1188	1200	1212		
Signal-to-noise ratio	200 – 340 baud	S/N fsk	20			dBm	

1) Referenced to a 600 Ω termination at the CPE Tip and Ring interface. Input signal at Pins CLI1 and CLI2.
2) Signal lower than –43.8 dBm is rejected.
3) Referenced to a 600 Ω termination at the CPE Tip and Ring interface. With a maximum gain in the RX chain. Input signal at Pin VL.

15 Package Information

Package SSO44
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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