UCB1510

AC97 digital modem codec

Rev. 01 — 4 February 2000 **Preliminary specification**

1. Description

The UCB1510 is a single chip, integrated mixed signal telecom codec that can directly be connected to a DAA and supports high speed modem protocols. The general purpose I/O pins provide programmable inputs and/or outputs to the system.

The UCB1510 has a serial AClink interface intended to communicate to the system controller. Both the codec input data and codec output data and the control register data are multiplexed on this interface.

2. Features

- Sigma delta telecom codec with programmable sample rate, including digitally controlled input voltage level, mute, loop back and clip detection functions. The telecom codec can be directly connected to a Data Access Arrangement (DAA) and includes a built in sidetone suppression circuit
- AClink (rev 2.1) interface with secondary codec support
- 3.3 V supply voltage and built in power saving modes make the UCB1510 optimal for portable and battery powered applications
- 5 V tolerant interface for motherboard/PC add on
- Maximum operating current 25 mA
- 8 general purpose IO pins for line interface control
- Interrupt detection driven wake up sequence for ring detect
- Low cost 12.288 MHz crystal

3. Applications

- Standalone modems
- Integrated modems
- Audio/Modem Riser (AMR) Cards
- Mobile Daughter Cards (MDC)

PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
UCB1510DB	SSOP28	plastic shrink small outline package, 28 leads, body width 5.3mm	SOT341-1

5. Block diagram

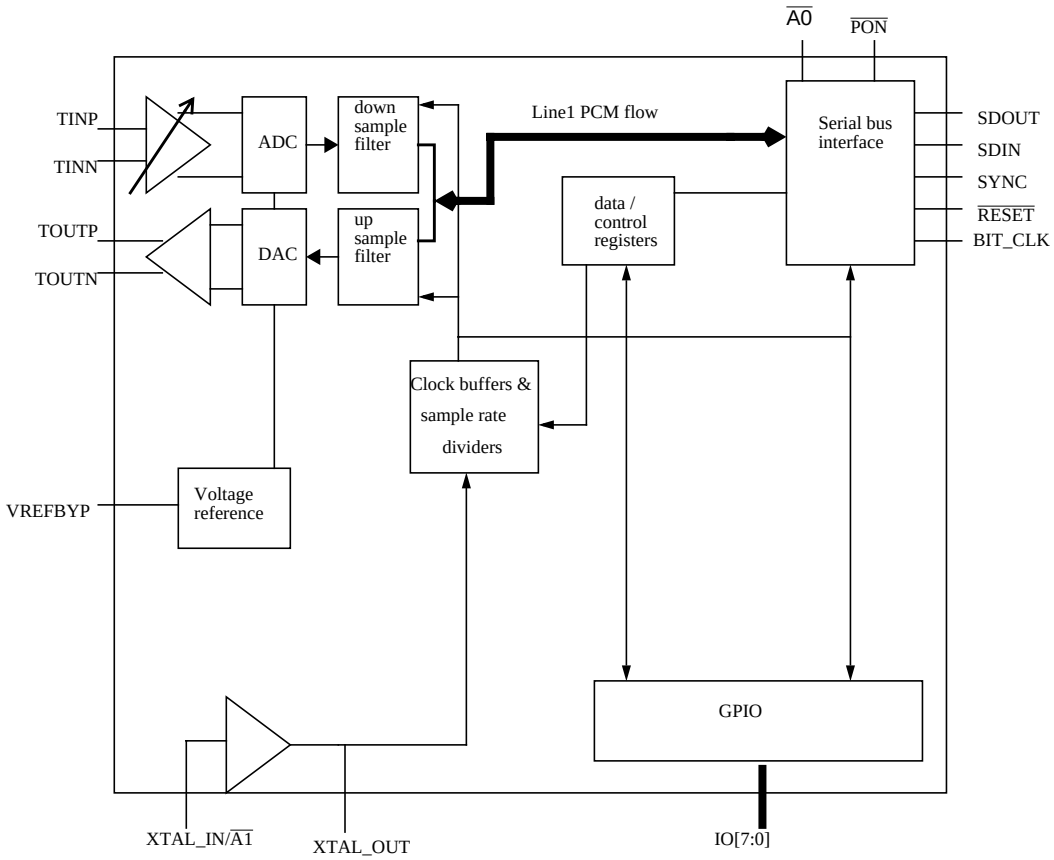


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

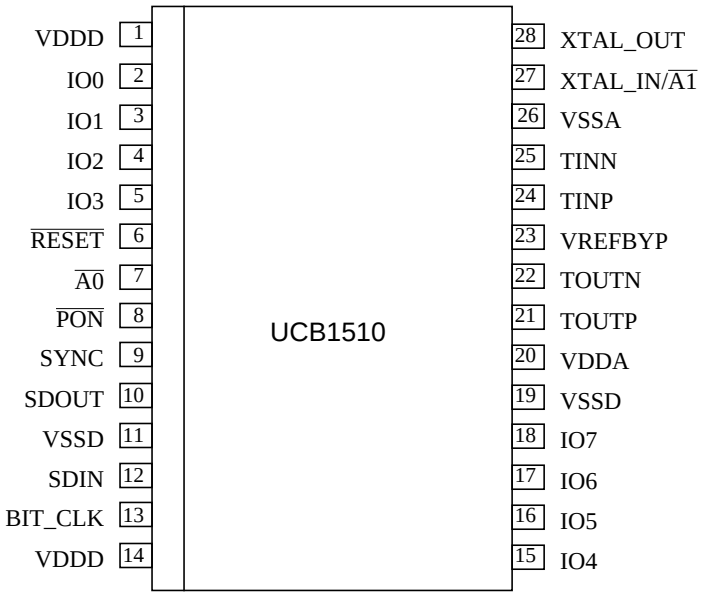


Fig 2. Pin configuration

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Reset state [1]	Type [2]	Description
V_{DDD}	1	-	S	digital supply
IO0	2	input	I/O_C	general purpose I/O pins
IO1	3	input	I/O_C	general purpose I/O pins
IO2	4	input	I/O_C	general purpose I/O pins
IO3	5	input	I/O_C	general purpose I/O pins
$\overline{RESET}$	6	-	I_C	asynchronous reset input
$\overline{A0}$	7	-	I_C	address select (for secondary codec) - inverted polarity
$\overline{PON}$	8	-	I_C	asynchronous cold reset
SYNC	9	-	I/O_C	AClink synchronization input
SDOUT	10	-	I_C	AClink data input
V_{SSD}	11	-	S	digital ground
SDIN	12	0 [4]	O_C	AClink data output
BIT_CLK	13	- [3]	I/O_C	AClink serial interface clock
V_{DDD}	14	-	S	digital supply
IO4	15	input	I/O_C	general purpose I/O pins

Table 2: Pin description *...continued*

Symbol	Pin	Reset state [1]	Type [2]	Description
IO5	16	input	I/O_C	general purpose I/O pins
IO6	17	input	I/O_C	general purpose I/O pins
IO7	18	input	I/O_C	general purpose I/O pins
V_{SSD}	19	-	S	digital ground
V_{DDA}	20	-	S	analog supply
TOUTP	21	hi Z	O_A	positive telecom codec output
TOUTN	22	hi Z	O_A	negative telecom codec output
VREFBYP	23	hi Z	I/O_A	external reference voltage bypass
TINP	24	-	I_A	positive telecom codec input
TINN	25	-	I_A	negative telecom codec input
V_{SSA}	26	-	S	analog ground
XTAL_IN/$\overline{A1}$	27	- [3]	I_A/I_C	Xtal oscillator/master clock input or inverted secondary address
XTAL_OUT	28	- [3]	O_A	Xtal oscillator output

[1] After cold or warm reset, the AClink interface is active with MLNK bit reset.

[2] I/O_C = CMOS bidirectional; I_D = digital input; S = supply; O_A = analog output; I_C = CMOS input; I_A = analog input; I/O_A = analog bidirectional; O_C = CMOS output.

[3] BIT_CLK is an input for AClink secondary codec, an output for primary codec. When BIT_CLK is an output, the XTAL oscillator is active.

[4] SDIN is driving a 0 until a valid SYNC framing signal is received after cold reset.

7. Functional description

The functional description of the devices id described in Section 8 through Section 15.

8. Telecom codec

The telecom codec contains an input channel, built up from a 64 times oversampling sigma delta analog to digital converter (ADC) with digital decimation filters, programmable gain and attenuation and built-in sidetone suppression circuit.

The output path consists of a digital up sample filter, a 64 time oversampling 4 bit digital to analog converter (DAC) circuit with integrated filter followed by a differential output driver, capable of directly driving a 600 Ω isolation transformer. The output path includes a mute function. The telecom codec also incorporates loop back modes, in which codec output path and the input path are connected in series. The loop back tap and entry points are identified as circled letters in Figure 3, loop back modes are described in the AClink register definition.

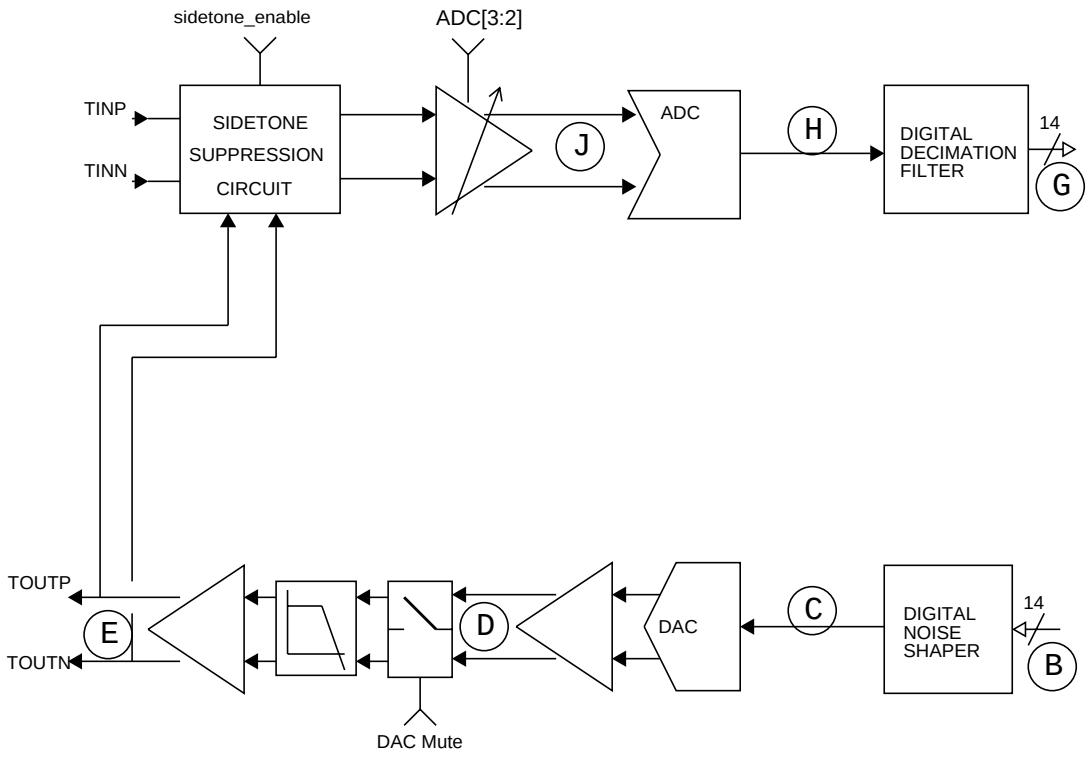


Fig 3. Telecom codec block diagram

The telecom sample rate (f_{st}) is derived from the AC master clock and is programmable using the sample rate registers. Not all AC97 specified sample rates are supported, refer to Table 3 “Sampling frequencies” for details.

PCM data is transferred in the slot 5 of the AClink.

Table 3: Sampling frequencies

Sampling frequency (Hz)	Register 0x40 value	Support	AC '97 requirements
7200	0x1C20	no	recommended
8000	0x1F40	yes	required
8228.57 (57600/7)	0x2024	no	recommended
8400	0x20D0	no	recommended
9000	0x2328	no	recommended
9600	0x2580	yes	required
10285.71 (72000/7)	0x282D	no	recommended
12000	0x2EE0	yes	recommended
13714.29 (96000/7)	0x3592	yes	required
16000	0x3E80	yes	required
19200	0x4B00	yes	recommended
24000	0x5DC0	yes	recommended
48000	0xBB80	no	recommended

Any programmed vlaue above 24 kHz will lead to a 24 kHz sampling rate.

Changing the sampling rate while the codec is active may lead to unpredictable results in the ADC and DAC chains and should be avoided.

The output section of the telecom codec is designed to interface with a 600 Ω line through an isolation transformer. The built in mute function is activated by the **DAC Mute** bit in register 0x46. The output driver remains active in the mute mode, however no output signal is produced.

8.1 Digital filters

These filters are tailored for high speed modem performance.

A voice band filter can be activated to reduce the noise in the lower frequencies.

Table 4: Filter characteristics

Parameter	Condition	Value
Group delay		25 samples
Pass band ripple		±0.1 dB
Out of band rejection	>0.55 fs	-50 dB
Pass band	(no voice band filter)	0.0016 to 0.45 fs
Transition band		0.45 to 0.55 fs
Voice band filter rejection band	0-0.0018 fs	30 dB
Voice band filter cutoff frequency		0.05 fs

8.2 Analog interface

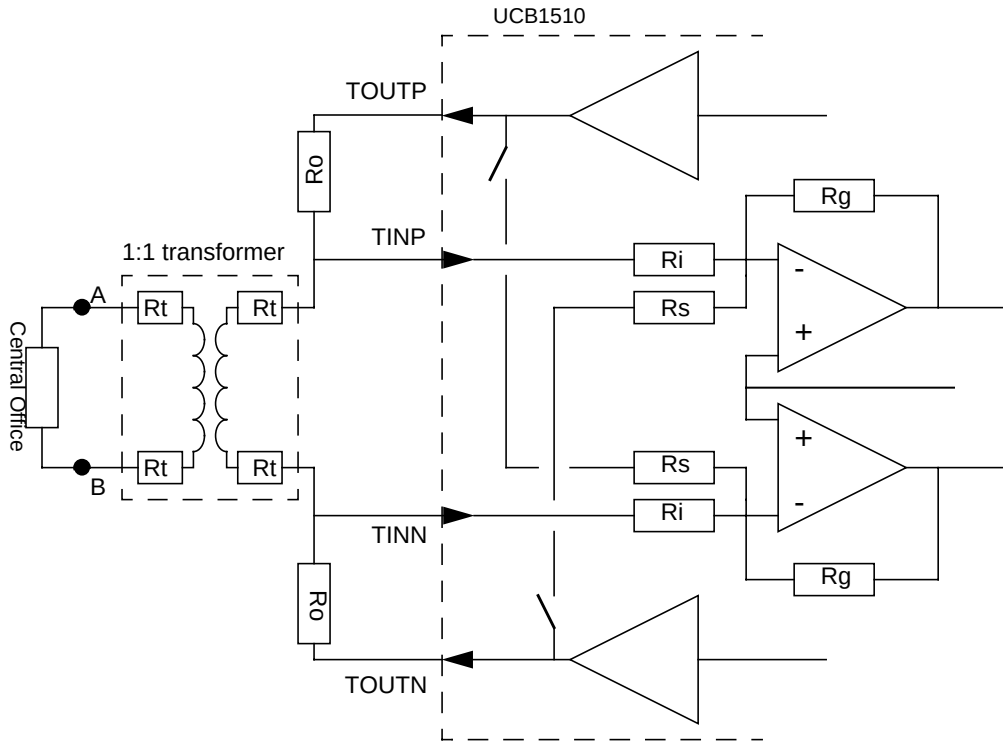


Fig 4. Typical telecom codec sidetone suppression circuit (without protection circuits).

An important built-in feature of the telecom codec is the sidetone suppression circuit. The sidetone suppression circuit is activated when **sidetone_enable** of register 0x5A is set.The sidetone suppression circuit subtracts part of the telecom output signal from the telecom input signal. As a result the available dynamic range of the input path can be more effectively utilized. If the sidetone suppression circuit is disabled, the telecom input dynamic range can be largely occupied by the telecom output signal.

The built-in side tone suppression circuit, shown in Figure 4, has a fixed subtraction ratio, set be the resistors R_s and R_i, which equals $^{600}/_{456}$. This ratio is calculated from the following relations.

The impedance seen by the telephone line equals:

$Z_{line} = 2 \times \left(R_t + R_t + \frac{R_o \times R_i}{R_o + R_i} \right)$, differential, in which R_t represents winding resistance of the transformer, divided by 2. Assuming $R_i >> R_o$, then

$R_{line} = R_t + R_t + R_o = 600/2 = 300\Omega$ single ended.

A typical transformer has 156 Ω winding impedance, thus R_o should be 144 Ω. The ratio of the telecom input and output voltage is, therefore:

$$V_{i(tel)} = V_{o(tel)} \times \frac{156 + 300}{156 + 300 + 144} = V_{o(tel)} \times \frac{456}{600}$$

Proper sidetone suppression thus requires R_s/R_i to be V_i/V_o.

9. On-chip reference circuit

The UCB1510 contains an on chip reference voltage source, which generates the bias currents and the virtual analog ground. Alternatively the UCB1510 can be driven from an external reference voltage source.

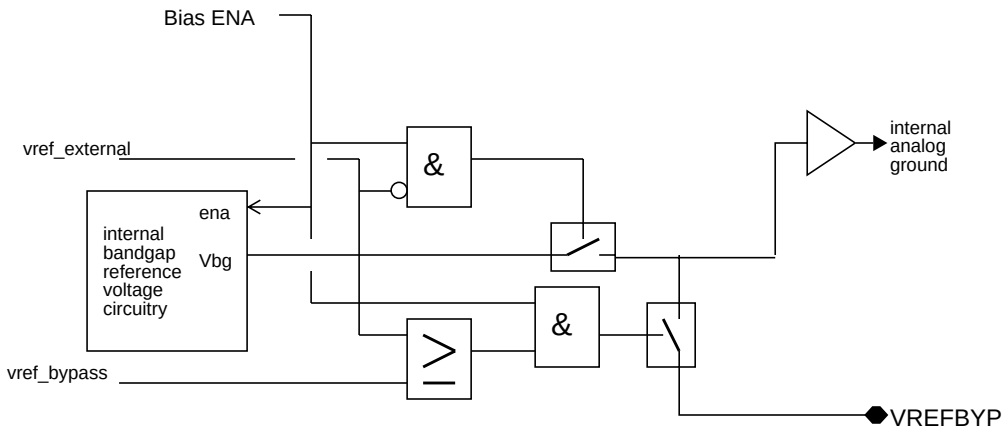


Fig 5. Block diagram of the reference circuit.

Two bits in the control register 0x5A determine the mode of operation of this reference voltage circuit. **vref_bypass** connects the internal reference voltage to the VREFBYP pin, while **vref_external** disables the internal reference voltage and switches the UCB1510 into the external voltage reference mode.

If the internal reference voltage is connected to the VREFBYP pin, an external capacitor could be connected to filter this reference voltage. When choosing a capacitor, the internal impedance (around 50 kΩ) should be taken into account.

If **vref_external** is set, an external voltage reference connected to the VREFBYP pin is used as the voltage reference by UCB1510.

10. Power supply strategy

Since all the control logic of the UCB1510 is powered by the V_{DDD}, power should always be present on this pin for interrupts to be possible. V_{DDA} needs not be present all the time although it is recommended to use the control bits to turn OFF the analog sections.

11. Register definition

11.1 Supported registers

Table 5: Supported registers

Register	Name
0x00 to 0x3A	All audio registers are ignored
0x3C	Extended Modem ID
0x3E	Extended Modem Status and Control
0x40	Line1 DAC/ADC Rate
0x42 and 0x44	Reserved for future use
0x46	Line1 DAC/ADC Level
0x48 and 0x4A	Reserved for future use
0x4C	GPIO Pin Configuration
0x4E	GPIO Pin Polarity
0x50	GPIO Pin Sticky
0x52	GPIO Pin Wake-up Mask
0x54	GPIO Pin Status
0x56	Miscellaneous Modem AFE Status and Control
0x58	Ignored
0x5A	Codec control
0x5C	Mode control
0x5E	Test control
0x5E to 0x7A	Ignored
0x7C	Vendor ID1
0x7E	Vendor ID2

11.2 Register detail

Shaded areas indicate read only data.

11.2.1 Extended Modem ID

Table 6: Extended Modem ID Register

Register address: 0x3C; default: N/A

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	ID1	ID0						
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol				0	0	0	0	LIN1

Table 7: Description of Extended Modem ID bits

Bit	Symbol	Function/Value
D15:14	ID[1:0]	{A1,A0} where A0 is the inverse polarity of the $\overline{A0}$ pin. A1 is the inverse polarity of **XTAL_IN** pin if A0 is HIGH ($\overline{A0}$ pin is LOW), otherwise A1 is 0.
D0	LIN1	Line 1 support indicator = 1 (i.e., Line 1 is supported).

[1] Writing this register will cause a register reset: all modem registers will then take their default values.

11.2.2 Extended Modem Status and Control

Table 8: Extended Modem Status and Control Register

Register address: 0x3E; default: 0xFFxx

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO

Table 9: Description of Extended Modem status and Control bits

Bit	Symbol	Function/Value
D15	PRH	Reserved, should be 1
D14	PRG	Reserved, should be 1
D13	PRF	Reserved, should be 1
D12	PRE	Reserved, should be 1
D11	PRD	1 -> Line1 DAC OFF
D10	PRC	1 -> Line1 ADC OFF
D9	PRB	1 -> Line1 V_{REF} OFF
D8	PRA	1 -> GPIO OFF
D7	HDAC	0 (not supported)
D6	HADC	0 (not supported)
D5	DAC2	0 (not supported)
D4	ADC2	0 (not supported)
D3	DAC1	1 indicates Line1 DAC ready (means that the Line1 DAC and the V_{REF} are enabled and ready)
D2	ADC1	1 indicates Line1 ADC ready (means that the Line1 ADC and the V_{REF} are enabled and ready)
D1	MREF	1 indicates Line1 V_{REF} up to nominal level.
D0	GPIO	1 indicates GPIO ready.

11.2.3 Line 1 Sample Rate

Table 10: Line 1 Sample Rate Register

Register address: 0x40; default: 0x1F40

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

Refer to Table 3 “Sampling frequencies” for supported sample rates.

11.2.4 Line 1 DAC/ADC Level

Table 11: Line 1 DAC/ADC Level Register

Register address: 0x46; default: 0x8080

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	DAC mute							
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	ADC mute				ADC3	ADC2	ADC1	ADC0

Table 12: Description of Line1 DAC/ADC Level bits

Bit	Symbol	Function/Value
D15	DAC mute	DAC section is active, but no signal will be sent.
D7	ADC mute	ADC section is active, but no signal will be sent.
D3-D2	ADC[3:2]	ADC Gain (0 -> 0 dB, 1 -> 6 dB, 2 -> 12 dB, 3 -> 18 dB)
D1-D0	ADC[1:0]	These bits are ignored.

11.2.5 GPIO Pin Configuration

Table 13: GPIO Pin Configuration Register

Register address: 0x4C; default: 0x00FF

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

The GPIO Pin Configuration register specifies whether a GPIO pin is configured for input (1) or for output (0).

11.2.6 GPIO Pin Polarity

Table 14: GPIO Pin Polarity Register

Register address: 0x4E; default: 0xFFFF

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0

The GPIO Pin Polarity register defines GPIO Input Polarity (0 = Low, 1 = High) when a GPIO pin is configured as an input.

11.2.7 GPIO Pin Sticky

Table 15: GPIO Pin Sticky Register

Register address: 0x50; default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0

The GPIO Pin Sticky register defines GPIO Input Type (0 = Non-Sticky, 1 = Sticky) when a GPIO pin is configured as input. Sticky is defined as Edge sensitive, Non-Sticky as Level-sensitive.

GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of the GPIO Pin Status register 0x54, and by reset.

Remark: Changing GPIO control registers while a GPIO is sticky may cause unwanted interrupts and should be done carefully.

11.2.8 GPIO Wake-up Mask

Table 16: GPIO Wake-up Mask Register

Register address: 0x52; default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0

The GPIO Pin Wake-up Mask register provides a mask for determining if an input GPIO change will generate a wake-up or GPIO_INT (0 = No, 1 = Yes).

When the AC-link is powered down, a wake-up event will trigger the assertion of SDIN. When the AC-link is powered up, a wake-up event will appear as GPIO_INT = 1 on bit 0 of input slot 12.

11.2.9 GPIO Pin Status

Table 17: GPIO Pin Status Register

Register address: 0x54; default: N/A

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0

The GPIO Status register reflects the state of all GPIO pins (inputs and outputs) on slot 12.

When the GPIO is an output pin, the value set on slot #12 is transmitted directly to the pin. When the GPIO pin is a non-sticky input, the status of the pin is accessible in read mode. When the GPIO is a sticky Input, a transition, either from high to low (polarity = 0) or from low-to-high (polarity = 1), will assert the corresponding GI bit to 1. The GI bit will remain asserted until it is cleared by a write of 0.

11.2.10 Miscellaneous Modem AFE Status and Control

Table 18: Miscellaneous Modem AFE Status and Control Register

Register address: 0x56; default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol			MLNK			reserved, should be 0x0		
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol		reserved, should be 0x0				L1B2	L1B1	L1B0

Table 19: Description of Miscellaneous Modem AFE Status and Control bits

Bit	Symbol	Function/Value
D13	MLNK	1 -> AClink goes to sleep.
D[2:0]	L1B[2:0]	Line1 loop back modes (refer to Table 20).

Table 20: Loop back modes

See Figure 3.

Mode	Description
0	Disabled
1	ADC loop back (incoming analog signal is amplified, digitized, down-sampled, LOOPED, up-sampled, converted to analog, amplified/filtered) (G) to (B) loop.
2	Local analog loop back (digital signal is up-sampled, converted to analog, amplified/filtered, LOOPED, amplified, digitized, down-sampled, sent back) (E) to (J) loop.
3	DAC loop back (digital signal is up-sampled, converted to analog, LOOPED digitized, down-sampled, sent back) (E) to (J) loop. Same as mode 2.
4	Remote analog loop back (incoming analog signal is amplified, LOOPED, amplified/filtered, sent back) (J) to (D) loop.
7	Digital loop back: signal is captured from the AC-link and sent back as is. Slot request for slot#5 is controlled according to the programmed sampling rate.

11.2.11 Vendor Specific Codec Control

Table 21: codec_control Register

Register address: 0x5A; default: 0x0400

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol				AC		ME	VE	VB
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	0	0	0	SE	0	0	0	VF

Table 22: codec_control bits

Bit	Symbol	Function/Value
D12	AC	adc_clip, in read mode, this bit indicates clipping in the line1 ADC. This indicator is sticky and should be cleared by writing it with a 0.
D10	ME	reserved, should be 1
D9	VE	vref_external, overwrites VB
D8	VB	vref_bypass
D[7:5], D[3:1]	0	Bits marked '0' are reserved for future use and should be programmed with 0.
D4	SE	sidetone_enable
D0	VF	voice_filter:1->enable voice band digital filter.

11.2.12 Vendor Specific Mode Control

Table 23: mode_control Register

Register address: 0x5C; default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol						reserved: 0x0		
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol		0	0	0			0	BITSTREAM

[1] Bits marked 0 are reserved for future use and should be programmed with 0.

Table 24: mode_control bits

Bit	Symbol	Function/Value
D0	BITSTREAM	line1 ADC bitstream data is sent directly to IO4. The associated clock is sent to IO6.

11.2.13 Vendor specific Test Control

Table 25: Test_control Register

Register address: 0x5E; default: N/A

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol								

This register cannot be reset. It has no effect until the IC is put in vendor test mode (see Table 29 "Mode selection with AC pins").

11.2.14 Vendor ID1

Table 26: Vendor ID1 Register

Register address: 0x7C; default: 0x5053

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	0	1	0	1	0	0	0	0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	0	1	0	1	0	0	1	1

11.2.15 Vendor ID2

Table 27: Vendor ID2 Register

Register address: 0x7E; default: 0x4301

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	0	1	0	0	0	0	1	1
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	0	0	0	0	0	0	0	1

11.3 Register reset modes

11.3.1 Warm reset

When a warm reset is activated, MLNK is set to 0 but the other registers retain their values. If the codec is primary, the BIT_CLK is started and stabilized after 200 ms.

11.3.2 Cold reset

When a cold reset is activated, MLNK is set to 0 and all registers are programmed to their default values. If the codec is primary, the BIT_CLK is started and stabilized after 200 ms.

11.3.3 Register reset

A register reset causes all registers to return to their default values. Initiated by a write to register 0x3C.

12. AC97 interface

12.1 Control register data transfer

The AClink frames is made of 13 slots. Slot0 is a 16-bit long tag slot, the remaining 12 slots are 20-bit long data transfer.

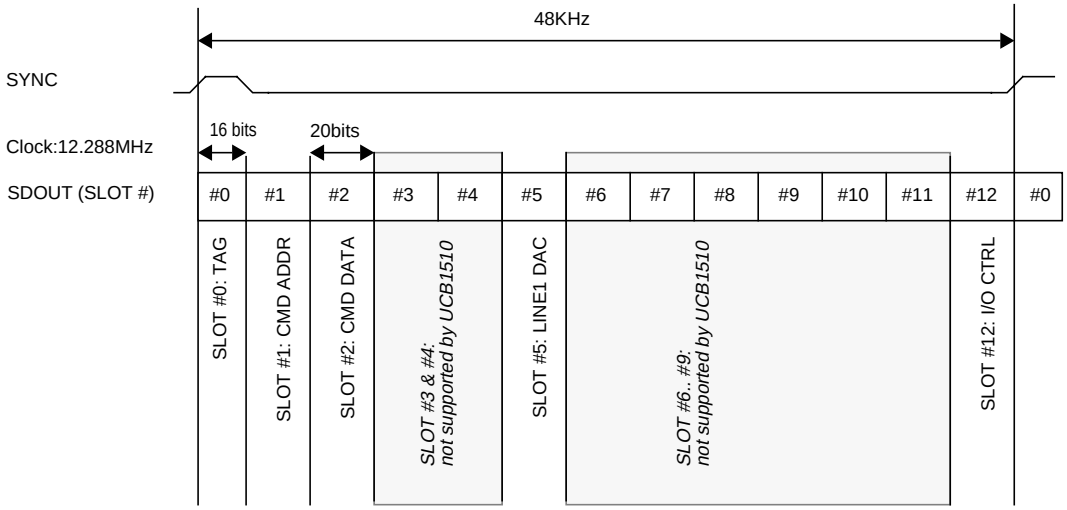


Fig 6. AClink frame slot definition

Register update is done at the end of slot 2. The new register value is effective thereafter.

Slot #0 and slot #3 to #12 are shared by all codecs (primary and secondary). Multiple codecs using the same slot cannot be used at the same time. Slot #1 and slot #2 are used for register transfer and are codec specific. Addressing is defined in the Tag slot #0: The UCB1510 will send a 1 as Tag slot bit 15 whenever the AClink is active (MLNK is 0).

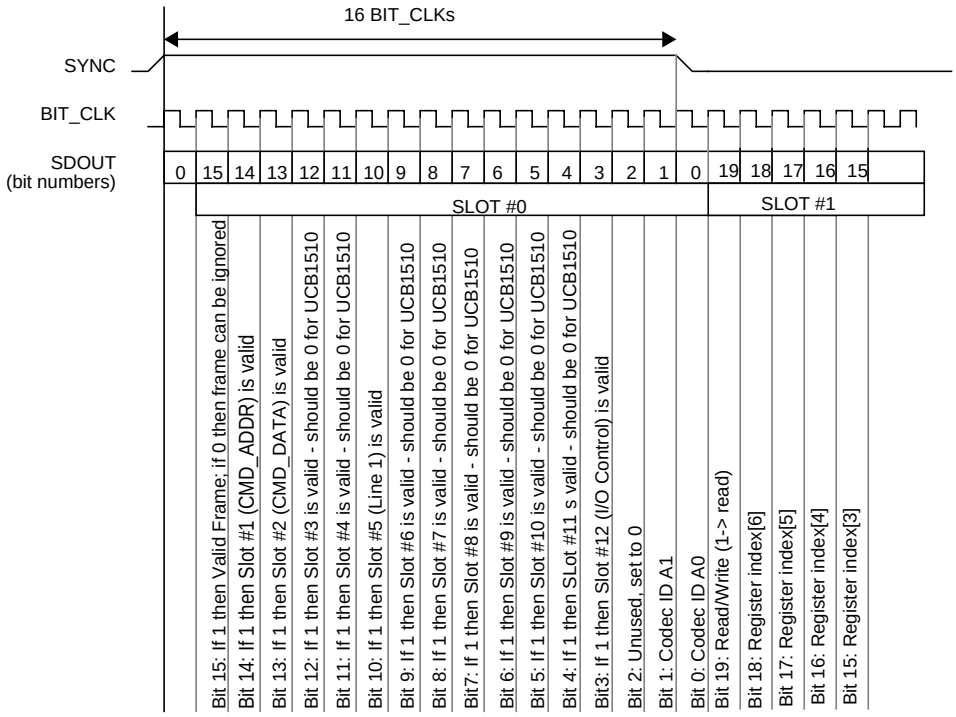


Fig 7. Tag slot bit definition (controller to codec)

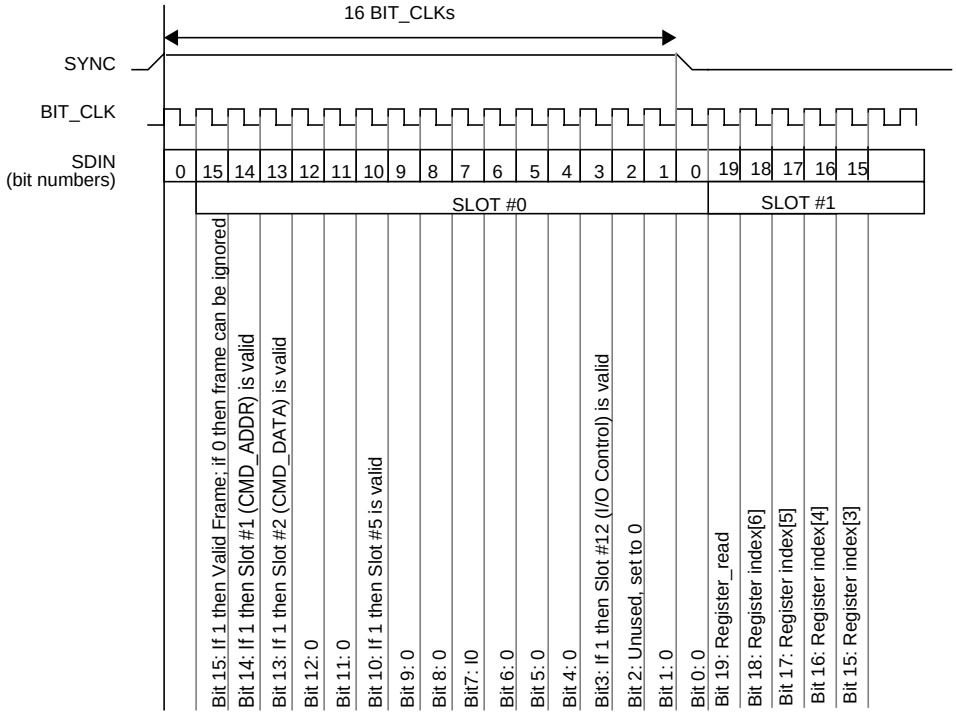


Fig 8. Tag slot bit definition (codec to controller)

12.2 Codec addressing

Table 28: Codec addressing examples

CMD ADDR slot #0 bit 14	CMD DATA slot #0 bit 13	Codec ID (A1, A0) slot #0 bits 1 and 0	Read/Write slot #1 bit 19	Transfer	Description
0	0	00	x	idle	No register data is transferred, slots 1 and 2 are not valid
1	x	00	1	primary read	Read for primary codec register
1	1	00	0	primary write	Write to a primary codec register
x	x	01	1	secondary read	Read from the 01 secondary codec register
x	x	11	0	secondary write	Write to a 11 secondary codec register

12.2.1 Primary codec addressing

For addressing a primary codec, bits 1 and 0 of the Tag slot (codec ID A1 and A0) should be 0. The bits 13 and 14 are used for register data transfer. When the controller is not sending/receiving control data, it should be addressing the primary codec. When writing to a register, the bits 14 and 13 (ADDR and DATA valid) should be set to 1. When reading from a register, only the bit 14 is required to be 1.

12.2.2 Secondary codec addressing

When the Codec ID (A1,A0) is not 00, the controller is addressing a secondary codec in a read or write sequence. The direction is defined in the slot 1 read/write bit (bit 19).

12.3 PCM sample transfer

Since the AClink frame frequency is defined to be 48kHz, exchanging samples with the controller at a different sampling rate requires the support of on demand sample transfer (slot request). The UCB1510 will send samples to the controller and assert the slot 5 valid bit in the slot#0 (bit10)of the AClink frame. When it needs a new sample from the controller, it will put a 0 on the slot5req bit in the slot#1 (bit9) of the AClink frame. When the slot5req bit is 1, it indicates to the controller that no new sample is needed. When the DAC is not active, the slot5req bit is kept at 0.

12.4 Interrupt request from UCB1510

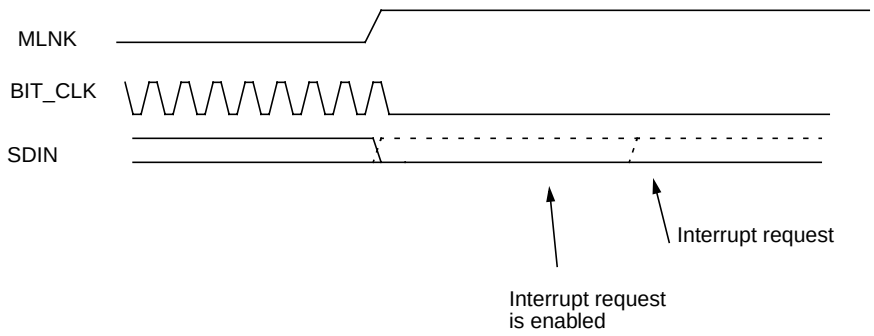


Fig 9. Setting the SDIN for interrupt request

12.4.1 When BIT_CLK is running

The AClink is active and the interrupt request is transmitted by setting the interrupt bit of slot 12 in the AClink frame.

If UCB1510 is configured as a primary codec, this is the case when MLNK is set to 0.

If UCB1510 is configured as a secondary codec, this is the case whether MLNK is set to 0 or 1.

12.4.2 When BIT_CLK is stopped

In order to request an interrupt, the UCB1510 will assert the SDIN pin, if MLNK is set to 1. BIT_CLK is not needed for this to happen. This applies when UCB1510 is used as a primary or secondary codec.

If UCB1510 is configured as a primary codec, BIT_CLK is stopped as a result of MLNK being set to 1.

If UCB1510 is configured as a secondary codec, BIT_CLK is stopped when the controller shuts down the primary codec. For UCB1510 to generate interrupt while BIT_CLK is stopped, MLNK has to be set to 1 before BIT_CLK is stopped.

After BIT_CLK is stopped, SDIN will be brought to 0, unless an interrupt asserts it to 1. It is recommended that a level triggered interrupt detection is used in case the interrupt request is asserted at the same time BIT_CLK is stopped.

12.5 Wake-up request to the UCB1510

A cold reset will program the registers to their default value and will wake up the AClink.

When the AClink is not active (no BIT_CLK present), a rising SYNC will cause a warm reset. If MLNK is set to 1, a rising RESET will also cause a warm reset. After a warm reset, MLNK will be reset to 0.

13. General purpose I/O

The UCB1510 has 8 programmable digital input/output (I/O) pins. These pins can be independently programmed for polarity, value, direction and interrupt through the GPIO control registers.

14. Interrupt generation

The UCB1510 contains a programmable interrupt control block.

The internal interrupt signal presents the 'OR' function of all interrupt status bits and can be used to give an interrupt to the system controller using the AClink interrupt protocol

The interrupt controller is implemented asynchronously. This provides the possibility to generate interrupts when BIT_CLK is stopped, e.g. an interrupt can be generated in power down mode, when the state of one of the IO pins changes (e.g. ring detect).

15. Reset circuit and mode selection

The AC97 specification rev 2.1 describes a number of states and reset functions for a modem codec either in primary or secondary codec.

15.1 Resets

15.1.1 Pulling the $\overline{\text{PON}}$ pin LOW

The $\overline{\text{PON}}$ pin acts as a hardware reset and is typically connected to a power detection circuit.

15.1.2 Activating the $\overline{\text{RESET}}$ pin

Pulling the $\overline{\text{RESET}}$ pin low will start a cold or a warm reset sequence.

If the circuit is active (MLNK = 0). A cold reset is started. The reset sequence will end after the rising edge of $\overline{\text{RESET}}$. Only then will the AClink be available. Vendor test modes are inactive as soon as the reset sequence starts so that mode sensing is possible.

If the MLNK bit is set when the $\overline{\text{RESET}}$ pin is pulled low, a warm reset is activated when $\overline{\text{RESET}}$ goes high again.

15.1.3 Activating the SYNC pin when AClink is inactive

When the AClink is not active (no BIT_CLK present), a rising SYNC will cause a warm reset.

15.1.4 Writing reg 0x3C

When written, the reg 0x3C will initiate a register reset. All registers are set to their default values.

15.2 Vendor test modes

When starting a $\overline{\text{RESET}}$ pin induced cold reset, the AClink pins are sensed for Vendor Test mode selection. BIT_CLK does not need to be running at that moment

Table 29: Mode selection with AC pins

SYNC	SDOUT	Mode
0	0	Normal mode, the AClink is operating properly.
0	1	ATE test mode. All AClink pins are set to input thus allowing board level JTAG testing.
1	0	Vendor test mode.
1	1	ATE test mode.

When the vendor test mode is activated, the vendor test register takes action. This mode is for test only and should not be used in normal operation. Exiting this mode requires a cold reset.

15.3 Primary/secondary codec selection

Secondary codec implementation is selected by wiring the $\overline{\text{A0}}$ pin low.

When $\overline{\text{A0}}$ is low (A0 is 1), the XTAL_IN is used as $\overline{\text{A1}}$ thus allowing ‘01’ and ‘11’ as secondary addresses. ‘10’ is not possible. The ID register will then reflect the A1,A0. Details can be found in the description of register 0x3C.

When the UCB1510 is a secondary codec, it derives its internal clock from BIT_CLK. BITCLK is therefore configured as input.

16. Limiting values

Table 30: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1], [2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+4.0	V
V_i	DC input voltage		–0.5	V_{DD} + 0.5	V
V_o	DC output voltage		–	V_{DD} + 0.5	V
$I_{i(d)}$	diode input current		–	10	mA
$I_{o(d)}$	diode output current		–	10	mA
I_o	continuous output current, digital outputs		–	4	mA
T_{stg}	storage temperature		–55	+150	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Absolute Maximum Rating section of this specification is not implied

[2] Parameters are valid over the ambient operating temperature unless otherwise specified. All voltages are with respect to V_{SSD}, unless otherwise noted.

17. Thermal characteristics

Table 31: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air		55	K/W

18. Static characteristics

Table 32: Static characteristics

V_{SSD} = V_{SSA1} = 0 V; T_{amb} =25 °C; all voltages referenced to V_{SSD}; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD}	digital supply voltage			3.0	3.3	3.6	V
V_{DDA1}	analog supply voltage			3.0	3.3	3.6	V
I_{DDD}	digital supply current		[1]	–	19	–	mA
I_{DDA1}	digital supply current	full functionality	[1]	–		–	mA
I_{DDA2}	analog supply current	Power down, only oscillator is on			t.b.d.		
V_{IL}	LOW level input voltage			–0.5	–	$+0.2V_{DDD}$	V
V_{IH}	HIGH level input voltage			$0.8V_{DDD}$	–	$0.5V_{DDD}$	V
V_{OL}	LOW level output voltage	I_{OL} = 4 mA		–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 4 mA		$0.8V_{DDD}$	–	–	V
f_{BIT_CLK}	serial interface clock frequency				12.288		MHz
T_{amb}	operating ambient temperature			–20	–	70	°C

[1] Indicative value measured during the initial characterization.

19. Dynamic characteristics

Table 33: Dynamic characteristics

V_{SSD} = V_{SSA} = 0 V; V_{DDD} = V_{DDA} = 3.3 V ±10%; T_{amb} = 25 °C; $V_{I(ref)}$ = 1.2 V; f_{BIT_CLK} = 12.288 MHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Telecom input [1]							
f_{st}	sample frequency			–	8	–	kHz
$V_{i(rms)}$	input voltage (RMS value)	differentially applied to TINN and TINP; ADC[3:2] = 1 (6 dB) in register 0x46		330	370	410	mV
$V_{i(bias)}$	DC bias voltage	TINN/TINP		1.2	–	1.6	V
α_i	input gain			0	6	18	dB
	input gain step size	2 LSBs ignored, Bit 3 step		4	6	8	dB
Z_i	input impedance			25	–	–	kΩ
S/N	signal-to-noise ratio			60	75	–	dB
THD	total harmonic distortion			–	–75	–60	dB
$LE_{(d)(ADC)}$	ADC differential linearity error			–	–	2	LSB
RES	codec resolution			–	14	–	bit
PBRR	pass-band ripple rejection	$f_{plt} < f_{sig} < f_{pht}$; no voice filter	[3], [6]	–	–	1.2	dB
		$f_{vht} < f_{sig} < f_{pht}$; voice filter activated	[3], [6]	–	–	1.2	dB
SBR_{vti}	stop-band rejection	$f_{sig} < f_{vti}$; voice filter activated	[3], [6]	30	–	–	dB
SBR_{sht}		$f_{sht} < f_{sig}$	[3], [6]	50	–	–	dB
D_{offset}	digital offset	no signal applied to input		–	–	50	LSB
S_{sup}	sidetone suppression effectiveness	600 Ω line impedance; 1:1 transformer with 156 Ω winding resistance		20	–	–	dB
Telecom output [2]							
f_{st}	sample frequency			–	8	–	kHz
$V_{o(rms)}$	output voltage (RMS value)	differentially measured between TOUTP and TOUTN		1.35	–	1.85	V
$V_{o(bias)}$	DC bias voltage	TOUTP/TOUTN; telecom O/P path enabled		1.2	–	1.6	V
RES	codec resolution			–	14	–	bit
S/N	signal-to-noise ratio			60	75	–	dB
THD	total harmonic distortion			–	–75	–	dB
PBRR	pass-band ripple rejection		[4], [6]	–	–	1.2	dB
SBR	stop-band rejection	$f_{sht} < f < f_{st}$	[4], [6]	50	–	–	dB
$OBR_{(rms)}$	out-of-band rejection (RMS value)	$f > f_{st}$		–	–	25	mV
$Z_{o(load)}$	load impedance			600	–	–	Ω
E_{offset}	offset error		[5]	–	–	100	mV

Table 33: Dynamic characteristics *...continued*

$V_{SSD} = V_{SSA} = 0$ V; $V_{DDD} = V_{DDA} = 3.3$ V ±10%; $T_{amb} = 25$ °C; $V_{I(ref)} = 1.2$ V; $f_{BIT\_CLK} = 12.288$ MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On-chip reference circuit						
$V_{i(ref)}$	reference voltage applied to VREFBYP		1.0	1.2	1.4	V
t_{STRTU}	start-up time of internal reference voltage circuit		–	–	1000	ns
Xtal oscillator						
f_{xtal}	Operating frequency			12.288		MHz
Z_{xtal}	start-up time of internal reference voltage circuit			10		kΩ
AClink control register data transfer						
f_{acclk}	CLK input frequency		0	12.288		MHz
D_{acclk}	CLK duty factor		–	50	–	%
Reset circuit						
$t_{W(NRESET)}$	$\overline{\text{RESET}}$ pulse width		5	–	–	ns
$t_{W(rst)}$	internal reset pulse width			32 t_{CLK}	–	ns

[1] Additional test conditions: Fsample = 8 kHz; input signal 1 kHz, 300 mV (RMS); Line1_ADC_ON = 1; TEL_VOICE_ENA = 0, input gain +6 dB

[2] Additional test conditions: Fsampling 8 kHz; 0 dB output attenuation; 90% of digital full scale input voltage; 1200 Ω load.

[3] See Figure 10.

[4] See Figure 11.

[5] Deviation of the analog output from 0, with 0 code input to telecom output path.

[6] All curves repeat around the sample frequency f_{sa} or f_{st} for telecom codec.

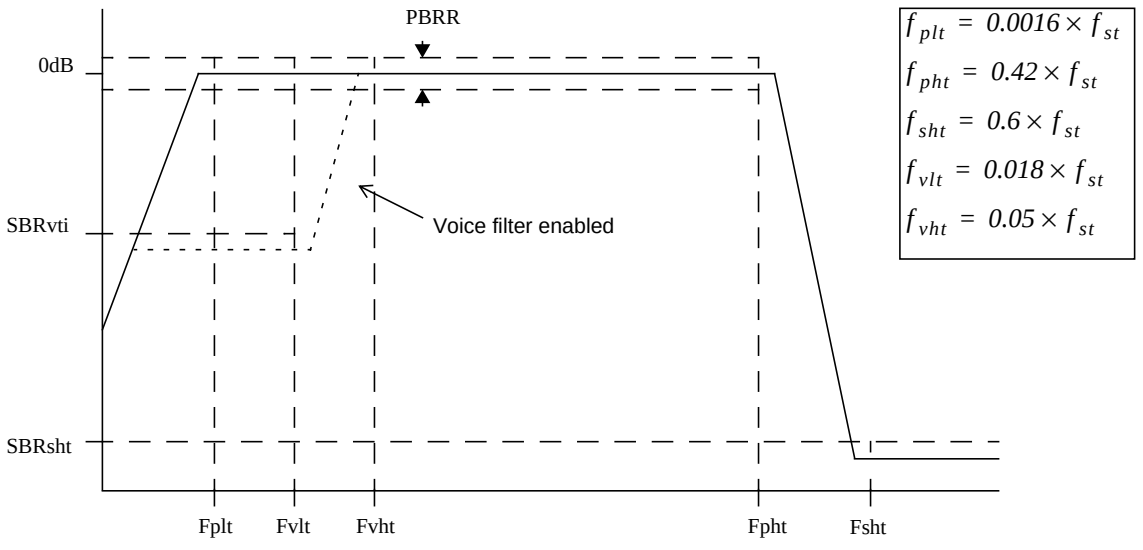


Fig 10. Telecom input frequency response

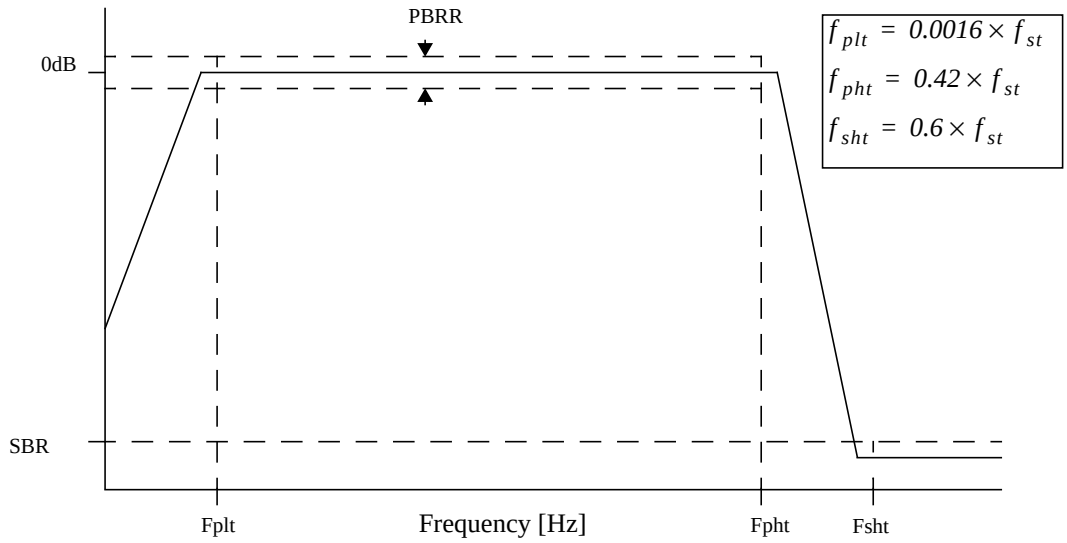
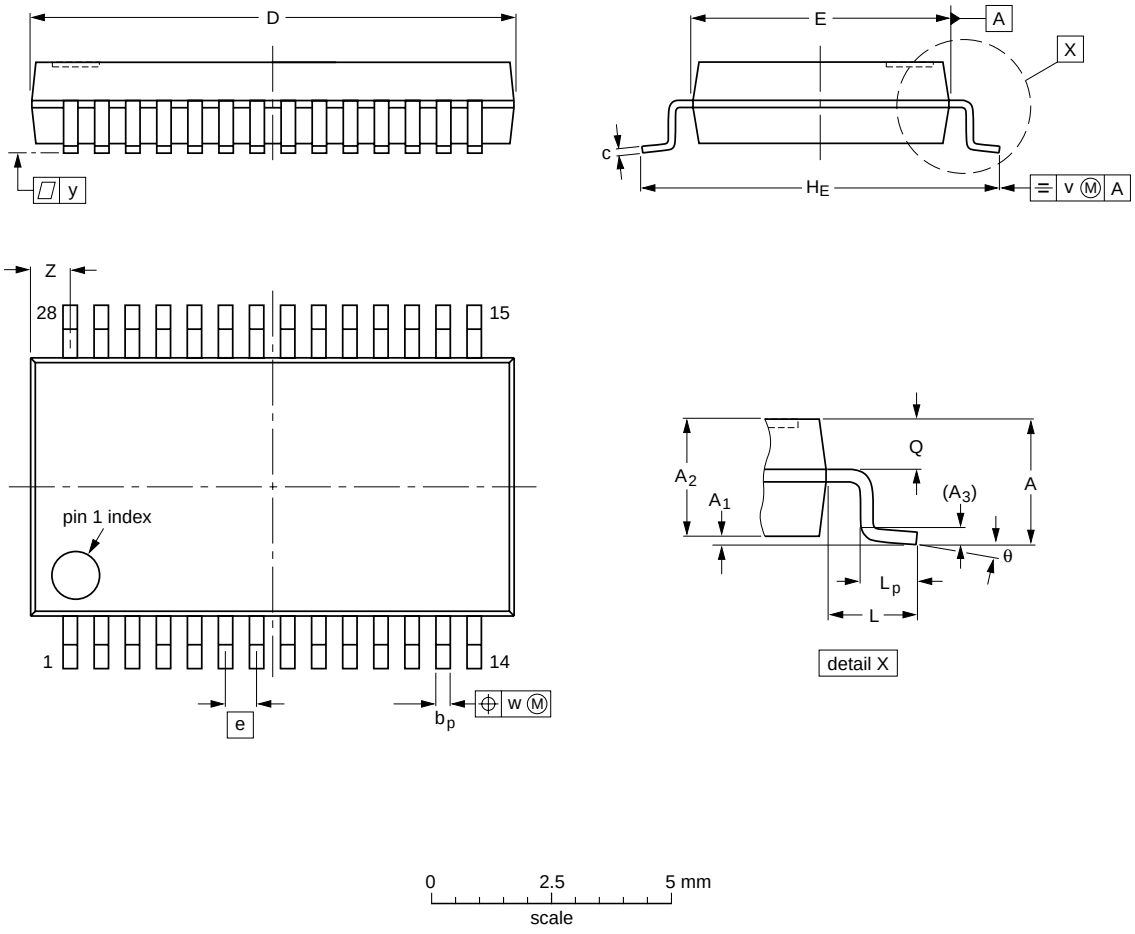


Fig 11. Telecom output frequency response

20. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Fig 12. SSOP28 package; SOT341-1.

21. Soldering

21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

21.5 Package related soldering information

Table 34: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

22. Revision history

Table 35: Revision history

Rev	Date	CPCN	Description
01	991111	-	**Converted to DBII format.** The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard.

23. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

24. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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