# UCC3923, UCC3924, UCC3925, UCC3926, UCC3927, UCC3928
# HIGH-VOLTAGE HOT-SWAP POWER MANAGER

SLUS471 – NOVEMBER 2000
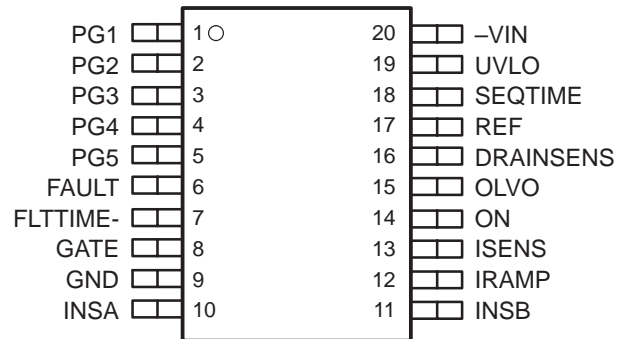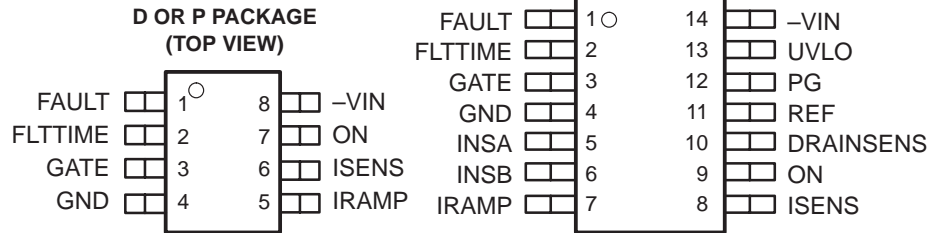
- **Wide Supply Range ±20 V to ±100 V**
- **Smooth Output Ramping Using Linear Current Amplifier**
- **Undervoltage and Overvoltage Shutdown**
- **Sequenced Open-Drain Outputs for Five DC-To-DC Converters**
- **Open-Drain Fault Output**
- **ON Input Referenced to Positive Supply (UCC3923)**
- **ON Input referenced to Negative Supply (possible alternative version)**
- **Dual Insertion Detection Inputs**
- **Electrostatic-Discharge Protection**
  - **Human-Body-Model 2 kV**
  - **Machine Model 200 V**

**PW PACKAGE (TOP VIEW)**

| | | | | |
|---|---|---|---|---|
| PG1 | 1 | | 20 | –VIN |
| PG2 | 2 | | 19 | UVLO |
| PG3 | 3 | | 18 | SEQTIME |
| PG4 | 4 | | 17 | REF |
| PG5 | 5 | | 16 | DRAINSENS |
| FAULT | 6 | | 15 | OLVO |
| FLTTIME- | 7 | | 14 | ON |
| GATE | 8 | | 13 | ISENS |
| GND | 9 | | 12 | IRAMP |
| INSA | 10 | | 11 | INSB |

**D OR P PACKAGE (TOP VIEW)**

| | | | | |
|---|---|---|---|---|
| FAULT | 1 | | 8 | –VIN |
| FLTTIME | 2 | | 7 | ON |
| GATE | 3 | | 6 | ISENS |
| GND | 4 | | 5 | IRAMP |

**PACKAGE (TOP VIEW)**

| | | | | |
|---|---|---|---|---|
| FAULT | 1 | | 14 | –VIN |
| FLTTIME | 2 | | 13 | UVLO |
| GATE | 3 | | 12 | PG |
| GND | 4 | | 11 | REF |
| INSA | 5 | | 10 | DRAINSENS |
| INSB | 6 | | 9 | ON |
| IRAMP | 7 | | 8 | ISENS |

**PRODUCT PREVIEW**

## description

The UCC3923 family of devices are Hot-Swap Power Managers for use with negative power supplies. These devices are optimized for use in systems with nominal –48-V supplies, but are fully functional over a supply range of –20 V to –200 V. These devices can be used both on plug-in cards and on back-planes to limit inrush current, control load turnon and turnoff, report faults, isolate faulty loads, and sequence downstream dc-to-dc converters.

The UCC3923 offers the basic features of controlled turnon, load current ramping, and logic output of fault status in a tiny 8-pin package. The UCC3924 adds undervoltage protection, two insertion detection pins, power-good sensing, one output for downstream converter enabling, and a reference for cascoding, in a 14-pin package. The UCC3925 has all of the previously noted features plus overvoltage protection and supply sequencing for up to five downstream converters in a 20-pin package.

**AVAILABLE OPTIONS**

| $T_A$ | ENABLE | PACKAGED DEVICES[†] | | |
|---|---|---|---|---|
| | | **TSSOP–8** | **TSSOP–14** | **TSSOP–20** |
| –40°C to 85°C | Active high | UCC3923 | UCC3924 | UCC39235 |
| | Active low | UCC3926 | UCC3927 | UCC3928 |

[†] All packages are available left end taped and reeled. Add an R suffix to the device type (e.g., UCC3923PWPR) to order quantities of 2000 devices per reel.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
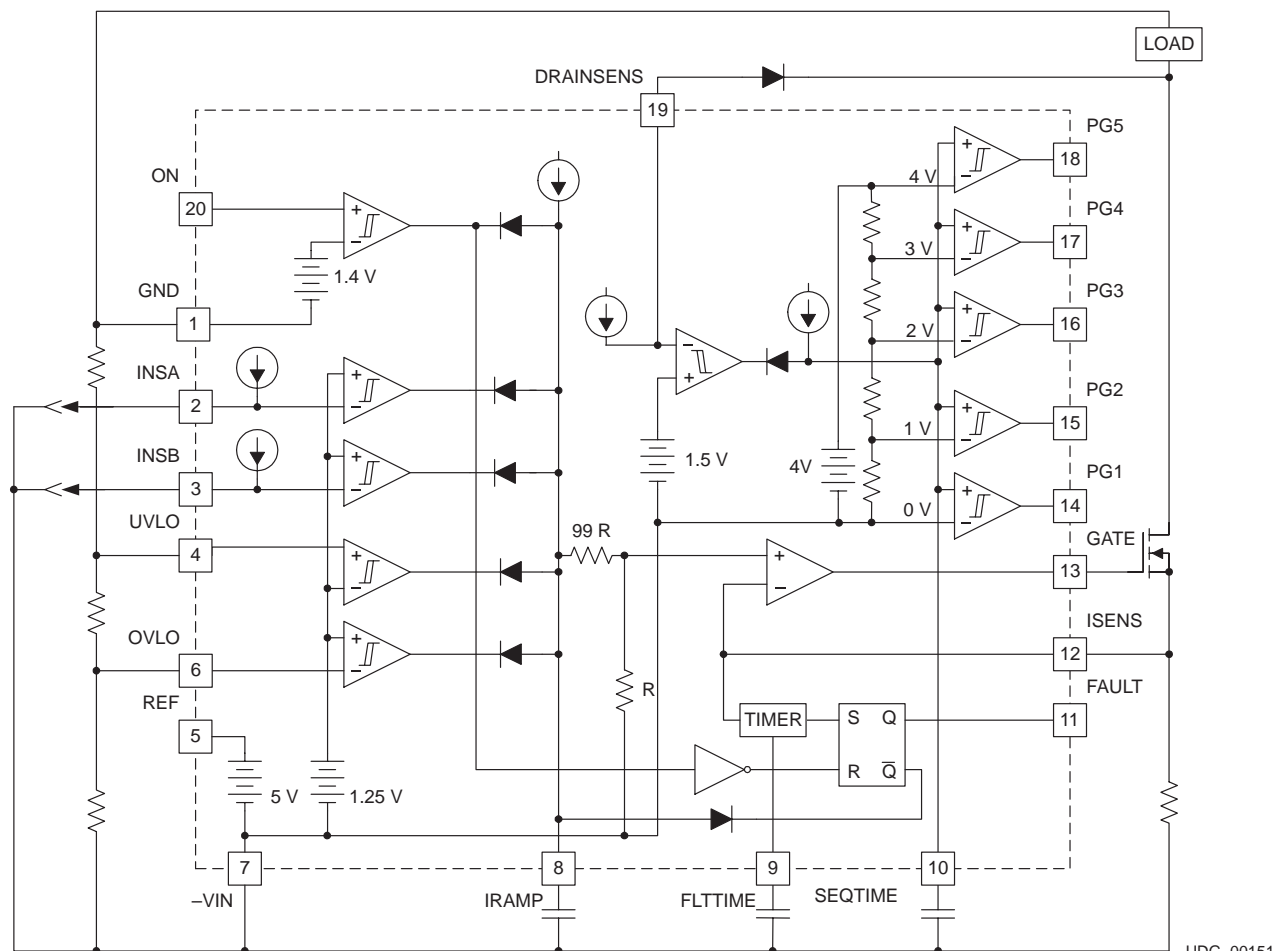
**TEXAS INSTRUMENTS**

# UCC3923, UCC3924, UCC3925, UCC3926, UCC3927, UCC3928
# HIGH-VOLTAGE HOT-SWAP POWER MANAGER

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## functional block diagram



UDG–00151

‡ 20-pin package shown. Pin numbers are for counting purposes only, Actual pin locations are dependent upon customer requirements and precedence of other products.

**PRODUCT PREVIEW**

### DETAILED OPTION MATRIX

| PIN NAME | DESCRIPTION | UCC3923 | UCC3924 | UCC3925 | UCC3926 | UCC3927 | UCC3928 |
|---|---|---|---|---|---|---|---|
| UVLO | Undervoltage input | | X | X | | X | X |
| OVLO | Overvoltage input | | | X | | | X |
| PGx | PG output(s) | | 1 | 5 | | 1 | 5 |
| REF | Reference output | | X | X | | X | X |
| INSA, INSB | Insert detect | | X | X | | X | X |
| DRAINSENS | Power good detection input | | X | X | | X | X |
| SEQTIME | Programming for downstream load sequencing | | | X | | | X |
| Packages | 8–Pin TSSOP | X | | | X | | |
| | 14–Pin TSSOP | | X | | | X | |
| | 20–Pin TSSOP | | | X | | | X |

## Terminal Functions

| NAME | TERMINAL NO. UCC3923 UCC3926 | TERMINAL NO. UCC3924 UCC3927 | TERMINAL NO. UCC3925 UCC3928 | I/O | DESCRIPTION |
|------|---------|---------|---------|-----|-------------|
| DRAINSENS | – | 10 | 16 | I | Power good detection input |
| FAULT | 1 | 1 | 6 | O | Logic fault output |
| FLTTIME | 2 | 2 | 7 | I | Programming for fault timeout |
| GATE | 3 | 3 | 8 | O | Gate drive output |
| GND | 4 | 4 | 9 | I | Ground |
| INSA | – | 5 | 10 | I | Insertion detection input A |
| INSB | – | 6 | 11 | I | Insertion detection input B |
| IRAMP | 5 | 7 | 12 | I | Programming for current ramping |
| ISENS | 6 | 8 | 13 | I | Current sense input |
| ON | 7 | 9 | 14 | O | Logic command to turn on power to load |
| OVLO | – | – | 15 | I | Input overvoltage detection input |
| PG1 | – | 12 | 1 | O | Enable for first downstream load |
| PG2 | – | – | 2 | O | Enable for second downstream load |
| PG3 | – | – | 3 | O | Enable for third downstream load |
| PG4 | – | – | 4 | O | Enable for fourth downstream load |
| PG5 | – | – | 5 | O | Enable for fifth downstream load |
| REF | – | 11 | 17 | O | Reference output |
| SEQTIME | – | – | 18 | I | Programming for downstream load sequencing |
| UVLO | – | 13 | 19 | I | Input undervoltage detection input |
| –VIN | 8 | 14 | 20 | I | Negative supply input |

## detailed description

### power good detection input (UCC3924 and UCC3925 only)

DRAINSENS is an input that senses the voltage across the power FET. When the voltage on DRAINSENS is less than 1V with respect to –VIN and IRAMP is greater than or equal to 5 V with respect to –VIN, then the power FET is considered fully on and the PG outputs are allowed to begin sequencing the loads.

### logic fault output (UCC3923, UCC3924, UCC3925)

FAULT is an open-drain, active-low driver that asserts when the fault latch is set. The UCC3923 UCC3924 and UCC3925 controls the load inrush during starting by closed-loop regulation of load current. When the ON input is low, IRAMP, FLTTIME, and SEQTIME are held low. When ON is asserted high, IRAMP is released and allows $C_{IRAMP}$ to charge. Load current is limited to:

$$I_{LOAD} \leq 0.01 \times \frac{V_{IRAMP}}{R_{SENSE}}$$

During this time, $C_{FLTTIME}$ charges. If $C_{FLTTIME}$ charges to 4 V before the power FET fully enhances, the fault latch sets, the load is immediately turned off, and FAULT pulls low. The fault latch is cleared when ON is pulled low.

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## detailed description (continued)

### programming for fault timeout

During the time when the power FET is regulating current to the load, FLTTIME is pulled high with 10 µA. When the load current drops below the commanded maximum load current, FLTTIME is quickly pulled low. If FLTTIME charges to 4 V before the power FET fully enhances, the fault latch sets and the load is immediately turned off.

### gate drive output

When ON is low, GATE is held low. When ON is asserted high, IRAMP is released and allows $C_{IRAMP}$ to charge. During this time, GATE rises, turning on the external power FET so that:

$$I_{LOAD} = 0.01 \times \frac{\left(V_{IRAMP} - V_{IN}\right)}{R_{SENSE}}$$

IRAMP does not ramp higher than 5 V above –VIN, so load current is programmed to a maximum of $0.05/R_{SENSE}$. If the load is unable to accept the current, GATE rises up to 12 V above –VIN, fully enhancing the power FET. If load current ever spikes above that maximum value, the current limiting amplifier reduces GATE voltage to a level that maintains $I_{LOAD}$ at $0.05/R_{SENSE}$.

### ground

GND is the ground input to the IC in negative supply systems. The ON input signal is measured with respect to GND. All other signals are with respect to –VIN.

### insertion detection

INSA and INSB are active-low inputs that must be asserted for the IC to drive the load. These inputs have internal pullup current sources of 10 µA so they can be driven by open-drain logic. These inputs can also be used as board insertion detection inputs. In this case, these inputs would be connected to corner pins of a connector. The mating pins of the connector would be connected to –VIN. This would prevent operation before both corners of the connector are mated.

### current ramping

When ON is low, IRAMP is held low. When ON is asserted high, IRAMP is released and allows $C_{IRAMP}$ to charge. During this time, GATE rises, turning on the external power FET so that:

$$I_{LOAD} = 0.01 \times \frac{\left(V_{IRAMP} - V_{IN}\right)}{R_{SENSE}}$$

IRAMP does not ramp higher than 5 V above –VIN, so load current is programmed to a maximum of $0.05/R_{SENSE}$.

### current sensing

Load current is sensed by the voltage between ISENS and –VIN. A current sense resistor, RSENSE is connected between ISENS and –VIN. Maximum load current is limited to:

$$I_{LOAD} = 0.01 \times \frac{\left(V_{IRAMP} - V_{IN}\right)}{R_{SENSE}} \text{ during current ramp and } I_{LOAD} \leq \frac{0.05}{R_{SENSE}}$$

when IRAMP reaches final value.

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## detailed description (continued)

### logic command to turn on power-to-load

Three logic inputs enable the load: INSA, INSB, and ON. To turn on the load, INSA and INSB must be lower than a TTL threshold above –VIN and ON must be more than a TTL threshold above GND.

### overvoltage/undervoltage lockout

In addition to the logic inputs INSA, INSB, and ON, two other inputs enable load current: OVLO and UVLO. Specifically, OVLO must be less than 1.25 V with respect to –VIN and UVLO must be more than 1.25 V with respect to –VIN to enable load current. These pins can be used as logic inputs or as precision overvoltage shutdown and undervoltage lockout inputs by connecting these inputs to a voltage divider from GND to –VIN.

### enable downstream power converter

The IC has five outputs to enable downstream power converters or loads. These outputs are open-drain active-low drivers. During power–up, all five outputs are high–impedance. When load current is ramped up to maximum command and the output power FET has $V_{DS} < 1$ V, $C_{SEQTIME}$ starts to charge and PG1 immediately asserts low. When $C_{SEQTIME}$ charges up to 1 V, PG2 asserts low. When $C_{SEQTIME}$ charges up to 2 V, PG3 asserts low. When $C_{SEQTIME}$ charges up to 3 V, PG4 asserts low and when $C_{SEQTIME}$ charges up to 4 V, PG4 asserts low.

### reference output

REF is a voltage reference output 5 V higher than –VIN. This output is enabled whenever –VIN to GND is greater than 20 V. This reference can be used as a bias for cascode devices to buffer low-voltage logic outputs. This reference should not be loaded with more than 50 μA.

### programming for downstream load sequencing

These outputs turn on sequentially, with PG1 turning on first, PG2 second, etc. The delay from PG1 to PG2 is the time required to charge the capacitor from SEQTIME to –VIN by 1 V. SEQTIME is pulled high through a 10-μA current source, so the delay between output enables is C/10 μA.

### negative supply input

–VIN is the negative supply input to the IC. All signals are measured with respect to –VIN except ON. In positive supply systems, –VIN is the ground input to the IC.

PRODUCT PREVIEW

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**absolute maximum ratings over operating free–air temperature range (unless otherwise noted)†**

Input voltage range, all pins except GND, ON, DRAINSENS‡ . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to 15 V
Input voltage range, GND, ON, DRAINSENS‡ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to 80 V
Output voltage range, PG1, PG2, PG3, PG4, PG5‡ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to 15 V
Output voltage range, FAULT‡ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to 65 V
Continuous output current, PG1, PG2, PG3, PG4, PG5, FAULT . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10 mA
Continuous total power dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –40°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . . . . . . . . . . . . . . . . . . . 260°C
ESD Protection: . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . HBM 2 kV
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . CDM 1 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to –VIN unless otherwise stated.

### DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| TSSOP–8 | 800 mW | 10 mW/°C | 200 mW |
| TSSOP–14 | 800 mW | 10 mW/°C | 200 mW |
| TSSOP–20 | 800 mW | 10 mW/°C | 200 mW |

**recommended operating conditions**

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage (–VIN to GND) | –20 | –80 | V |
| Input voltage (FLTTIME, INSA, INSB, IRAM, OVLO, SEQTIME, UVLO to –VIN) | 0 | 7 | V |
| Input voltage (ISENS to –VIN) | 0 | 0.2 | V |
| Input voltage (DRAINSENS to –VIN) | 0 | 80 | V |
| Input voltage (ON to GND) | 0 | 80 | V |
| Output current (PG1, PG2, PG3, PG4, PG5, FAULT, REF) | | 2 | mA |
| Operating virtual junction temperature, $T_J$ | –40 | 125 | °C |

**electrostatic discharge protection**

| | MIN | MAX | UNIT |
|---|---|---|---|
| Human body model | | 2 | kV |
| Charged device model | | 1 | kV |
| Machine model | | 0.2 | kV |

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**electrical characteristics over recommended operating junction temperature range,**
**−VIN to GND = −48 V, ON to GND = 2.8 V, INSA = INSB = −VIN, ISENS = −VIN, UVLO = 2.5 V, OVLO = VIN, all outputs unloaded (unless otherwise noted)**

### power fet drive

| PARAMETER | TEST CONDITIONS (See Note 1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| GATE output voltage | $V_{ISENS}$ = 0 V | 10 | 12 | 14 | V |
| GATE pulldown current in fault | $V_{ISENS}$ = 0.1 V | 100 | 250 | | mA |
| ISENS input current | ON = high,      0 V < $V_{ISENS}$ < 0.1 V | −1 | | 1 | µA |

### timers

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| IRAMP pullup current during start | ON = high,      0 V < $V_{IRAMP}$ < 5 V | | 10 | | µA |
| IRAMP low voltage | ON = low | | | 2 | mV |
| IRAMP to ISENS gain | ON = high,      0 V < $V_{IRAMP}$ < 5 V | | 0.01 | | V/V |
| IRAMP offset voltage referred to ISENS | ON = high,      $V_{IRAMP}$ = 0 V | −2 | | 2 | mV |
| IRAMP clamp voltage referred to ISENS | ON = high | 45 | 50 | 55 | mV |
| FLTTIME pullup current during current limit | ON = high,      Fault latch not set | | 10 | | µA |
| FLTTIME low voltage | ON = low | | | 10 | mV |
| FLTTIME fault threshold voltage | ON = high,      $V_{ISENS}$ = 0.1 V | 3.75 | 4.00 | 4.25 | V |
| FLTTIME discharge current | ON = low | 10 | | | mA |
| SEQTIME pullup current | ON = high,      $V_{IRAMP}$ = 5 V,   $V_{ISENS}$ = 0 V | | 10 | | µA |
| SEQTIME low-level input voltage | ON = low | | | 10 | mV |
| SEQTIME to PG2 threshold voltage | ON = high,      $V_{IRAMP}$ = 5 V,   $V_{ISENS}$ = 0 V | 0.9 | 1.0 | 1.1 | V |
| SEQTIME to PG3 threshold voltage | ON = high,      $V_{IRAMP}$ = 5 V,   $V_{ISENS}$ = 0 V | 1.9 | 2.0 | 2.1 | V |
| SEQTIME to PG4 threshold voltage | ON = high,      $V_{IRAMP}$ = 5 V,   $V_{ISENS}$ = 0 V | 2.9 | 3.0 | 3.1 | V |
| SEQTIME to PG5 threshold voltage | ON = high,      $V_{IRAMP}$ = 5 V,   $V_{ISENS}$ = 0 V | 3.9 | 4.0 | 4.1 | V |
| SEQTIME discharge current | ON = low | 10 | | | mA |

### power good

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| PG1, PG2, PG3, PG4, PG5 on resistance | ON = high,      $V_{SEQTIME}$ = 5 V, $V_{ISENS}$ = 0 V | | | 100 | Ω |
| DRAINSENS threshold voltage | To PG1 rising | 0.85 | 1.00 | 1.15 | V |
| DRAINSENS pullup current | DRAINSENS = −VIN | | 10 | | µA |

### fault output

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| FAULT on resistance | ON = high,      $V_{ISENS}$ = 0.1 V, $V_{FLTTIME}$ = 5 V | | | 100 | Ω |

**PRODUCT PREVIEW**

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electrical characteristics over recommended operating junction temperature range,
−VIN to GND = −48 V, ON to GND = 2.8 V, INSA = INSB = −VIN, ISENS = −VIN, UVLO = 2.5 V, OVLO
= VIN, all outputs unloaded (unless otherwise noted) (continued)

### voltage reference output

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| REF voltage | −50 µA < $I_{REF}$ < 0 µA | 4.9 | 5.0 | 5.1 | V |

### undervoltage/overvoltage lockout

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| UVLO falling threshold | ON = high,     to GATE falling | 1.20 | 1.25 | 1.30 | V |
| UVLO hysteresis | ON = high,     to GATE rising | | 25 | | mV |
| UVLO input current | $V_{UVLO}$ = 2.5 V | −1 | | 1 | µA |
| OVLO rising threshold | ON = high,     to GATE falling | 1.20 | 1.25 | 1.30 | V |
| OVLO hysteresis | ON = high,     to GATE rising | | 25 | | mV |
| OVLO input current | $V_{OVLO}$ = 2.5 V | −1 | | 1 | µA |

### supply and control inputs

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| −VIN input current | | | 250 | | µA |
| INSA, INSB threshold voltage | ON = high,     to GATE rising | 1.0 | 1.4 | 1.8 | V |
| INSA, INSB pullup current | $V_{INSA}$ = $V_{INSB}$ = −VIN | | 10 | | µA |
| ON threshold voltage with respect to GND | To GATE rising | 1.0 | 1.4 | 1.8 | V |
| ON input current | $V_{ON} − V_{GND}$ = 5 V | | 10 | | µA |

**TYPICAL CHARACTERISTICS**

TYPICAL TURNON CYCLE



**Figure 1**

TURNON INTO EXCESSIVELY HEAVY LOAD
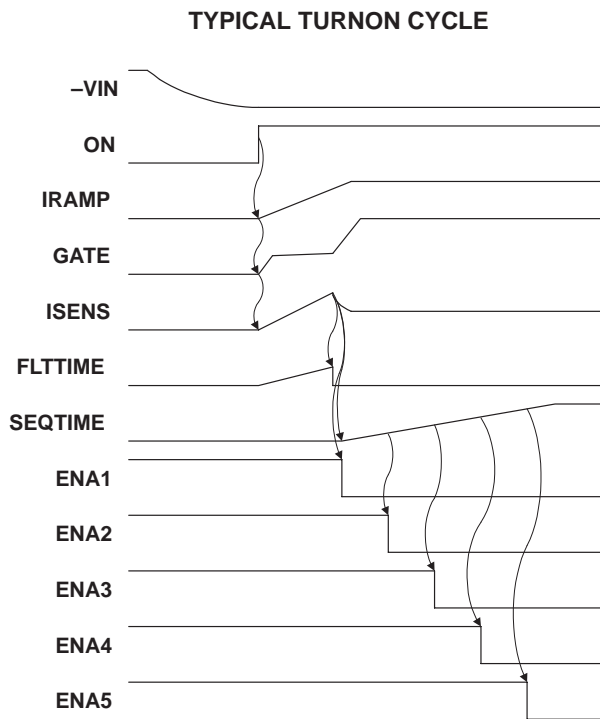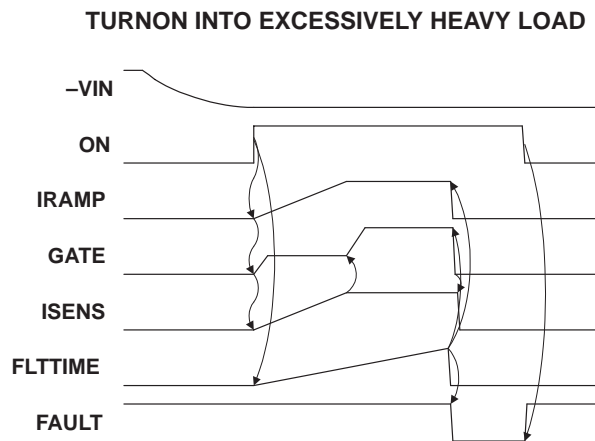


**Figure 2**

**APPLICATION INFORMATION**

**ESD Protection**

All UCC3923, UCC3924, and UCC3925 terminals incorporated ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL–STD–883C.

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