



UF840

MOSFET

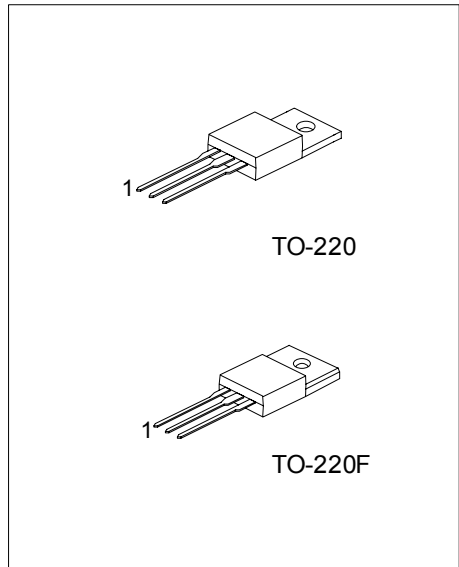
8A, 500V, 0.85Ω, N-CHANNEL POWER MOSFET

DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

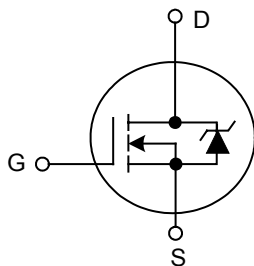
FEATURES

- * 8A, 500V, Low $R_{DS(ON)}$ (0.85Ω)
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance



*Pb-free plating product number: UF840L

SYMBOL



ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UF840-TA3-T	UF840L-TA3-T	TO-220	G	D	S	Tube
UF840-TF3-T	UF840L-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: GATE D: DRAIN S: SOURCE

<p>UF840L-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) T: Tube (2) TA3: TO-220, TF3: TO-220F (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ **ABSOLUTE MAXIMUM RATINGS** (Ta = 25 , unless Otherwise Specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J = 25 ~ 125)	V _{DSS}	500	V
Drain to Gate Voltage (R _{GS} = 20kΩ, T _J = 25 ~ 125)	V _{DGR}	500	V
Gate to Source Voltage	V _{GS}	±20	V
Drain Current	Continuous	8.0	A
	T _C = 100	5.1	A
	Pulsed	I _{DM}	32
Total Power Dissipation (Ta = 25)	P _D	125	W
Derating above 25		1.0	W/
Single Pulse Avalanche Energy Rating (V _{DD} =50V, starting T _J =25 , L=14mH, R _G =25Ω, peak I _{AS} = 8A)	E _{AS}	510	mJ
Operating Temperature Range	T _{OPR}	-55 ~ +150	
Storage Temperature Range	T _{STG}	-55 ~ +150	

Note: 1. Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.

2. Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ _{JA}	62.5	/W
Thermal Resistance Junction-Case	θ _{Jc}	1.0	

■ **ELECTRICAL SPECIFICATIONS** (Ta = 25 , unless Otherwise Specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 16)	500			V
Gate to Threshold Voltage	V _{GS(THR)}	V _{GS} = V _{DS} , I _D = 250μA	2		4	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V	8			A
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			25	μA
		V _{DS} = 0.8 × Rated BV _{DSS} , V _{GS} = 0V, T _J = 125			250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	R _{DS(ON)}	I _D = 4.4A, V _{GS} = 10V (Figure 14, 15)		0.8	0.85	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} ≥ 50V, I _D = 4.4A (Figure 18)	4.9	7.4		S
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 250V, I _D ≈ 8A, R _G = 9.1Ω, R _L = 30Ω (Note 2)		15	21	ns
Rise Time	t _r			21	35	ns
Turn-Off Delay Time	t _{DLY(OFF)}			50	74	ns
Fall Time	t _f			20	30	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, I _D = 8A, V _{DS} = 0.8 × Rated BV _{DSS}		42	63	nC
Gate to Source Charge	Q _{GS}	I _{G(REF)} = 1.5mA (Figure 20)		7		nC
Gate to Drain "Miller" Charge	Q _{GD}	(Note 3)		22		nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz (Figure 17)		1225		pF
Output Capacitance	C _{OSS}			200		pF
Reverse - Transfer Capacitance	C _{RSS}			85		pF

NOTE : 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

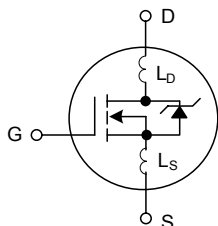
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance	L_D		3.5		nH
Measured from the contact screw on tab to center of die			4.5		nH
Internal Source Inductance	L_S		7.5		nH
Measured from the source lead(6mm from header) to source bond pad					

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

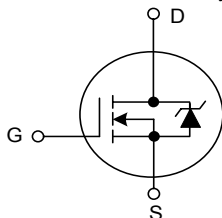


SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $V_{GS} = 0\text{V}$ (Figure 19)			2	V
Continuous Source to Drain Current	I_{SD}	Note 2			8	A
Pulse Source to Drain Current	I_{SDM}				32	A
Reverse Recovery Time	t_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	210	475	970	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	2	4.6	8.2	μC

NOTE : 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycles $\leq 2\%$.

2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



■ TEST CIRCUITS AND WAVEFORMS

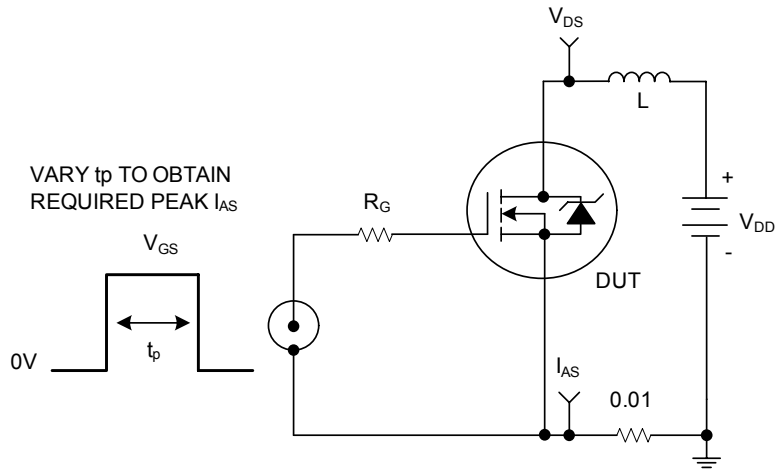


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

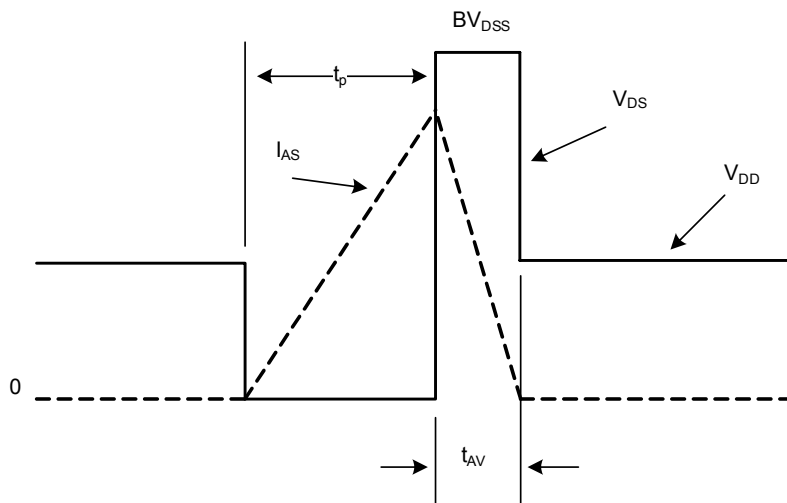


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

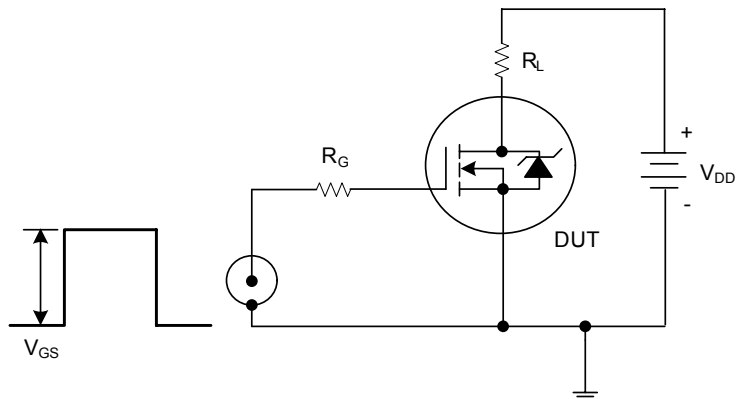


FIGURE 3. SWITCHING TIME TEST CIRCUIT

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

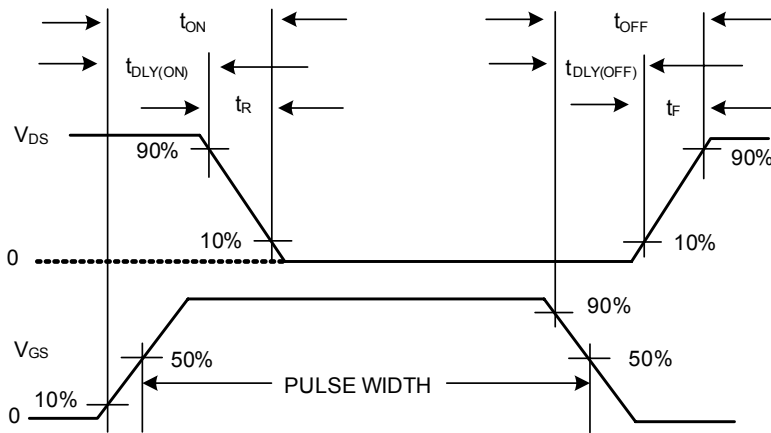


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

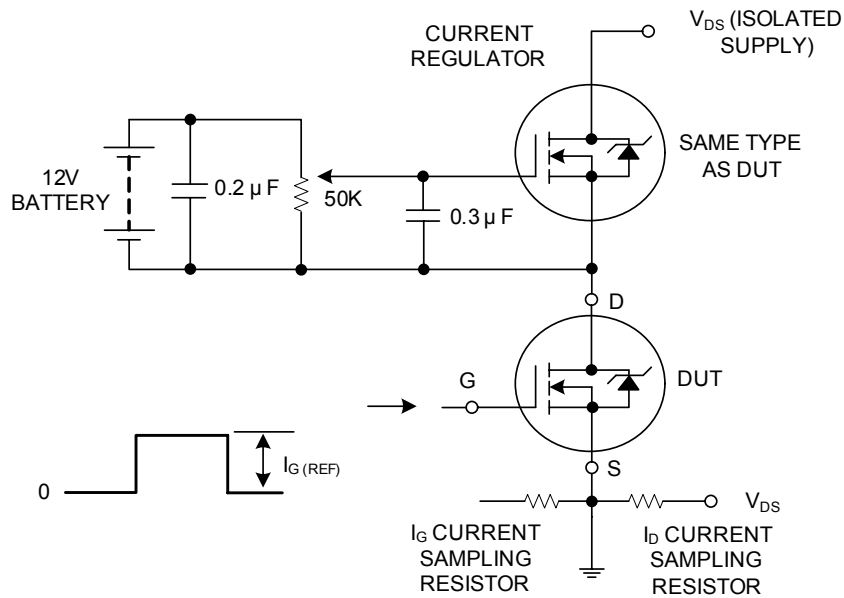


FIGURE 5. GATE CHARGE TEST CIRCUIT

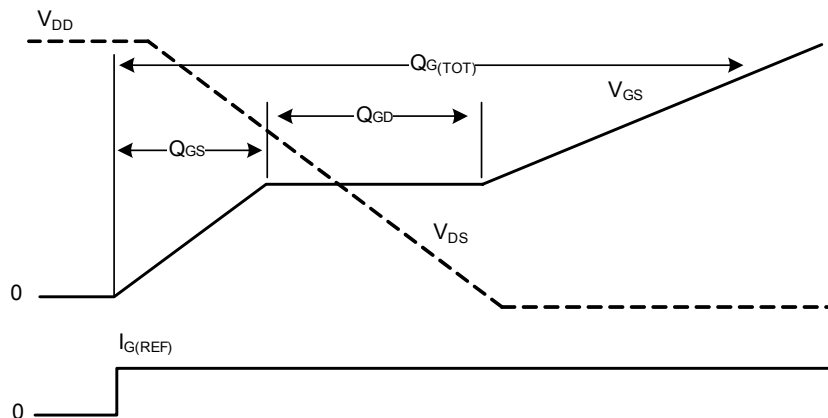


FIGURE 6. GATE CHARGE WAVEFORMS

■ TYPICAL CHARACTERISTICS

Figure 7. Normalized Power Dissipation vs. Case Temperature

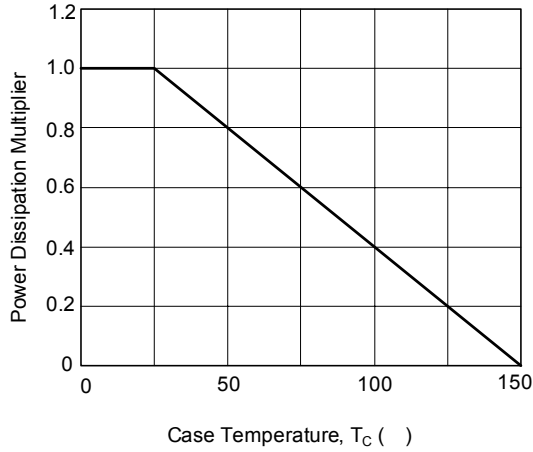


Figure 8. Maximum Continuous Drain Current vs. Case Temperature

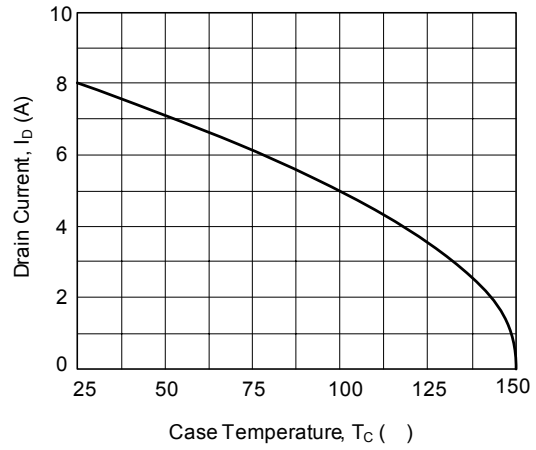


Figure 9. Normalized Maximum Transient Thermal Impedance

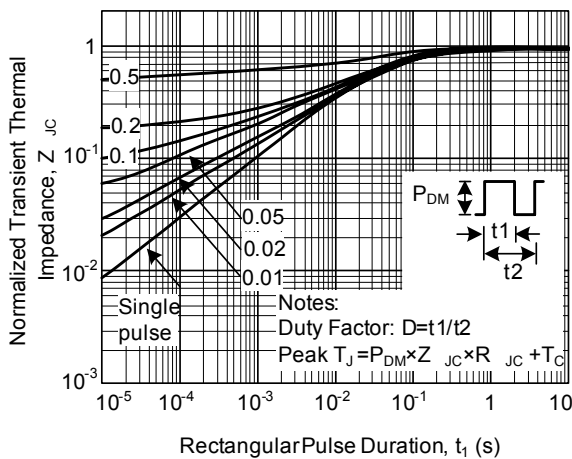


Figure 10. Forward Bias Safe Operating Area

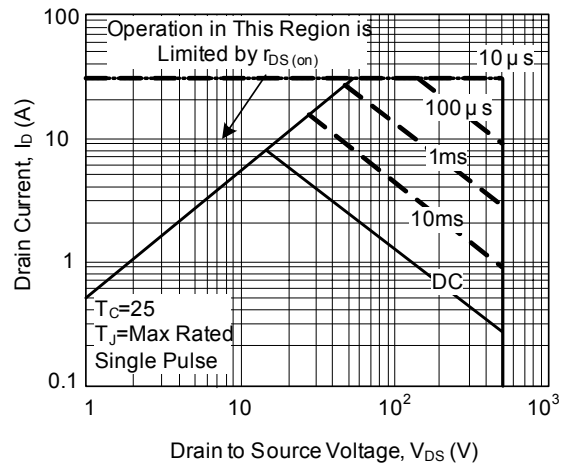


Figure 11. Output Characteristics

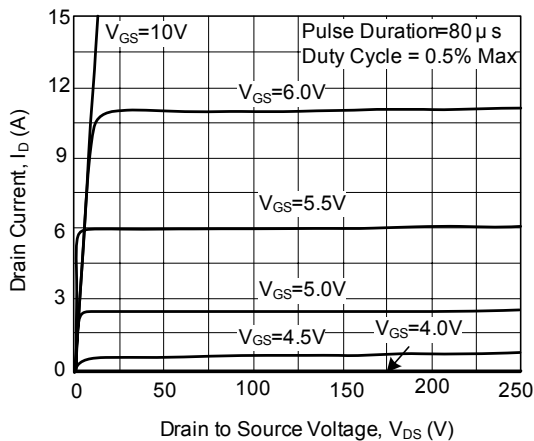
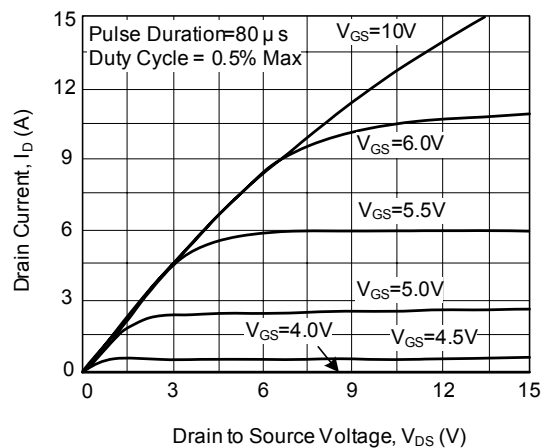


Figure 12. Saturation Characteristics



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 13. Transfer Characteristics

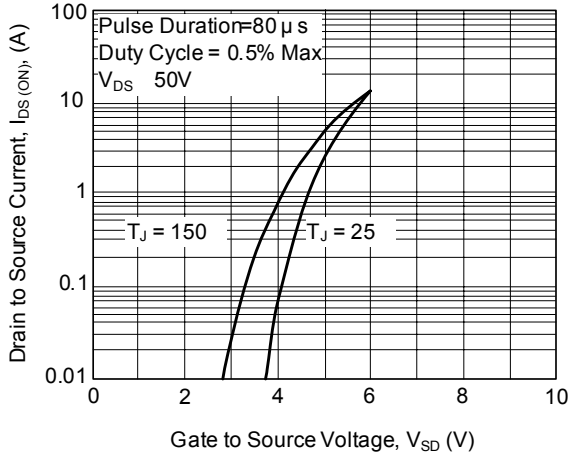


Figure 14. Drain to Source on Resistance vs. Voltage and Drain Current

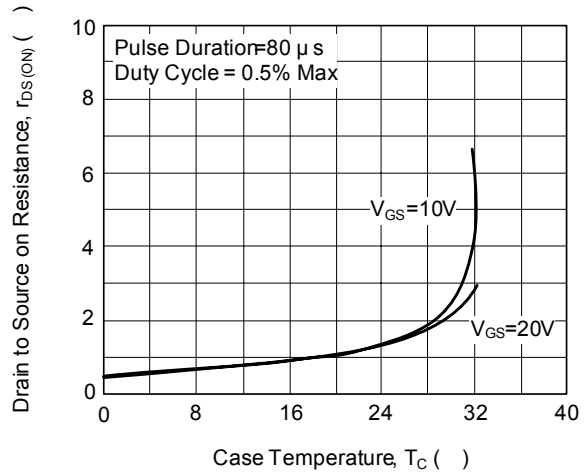


Figure 15. Normalized Drain to Source on Resistance vs. Junction Temperature

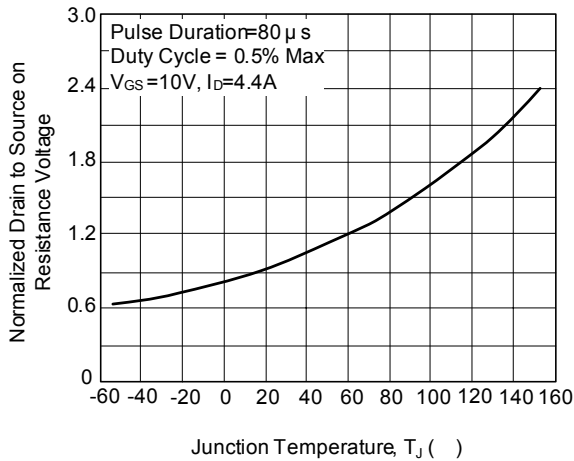


Figure 16. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

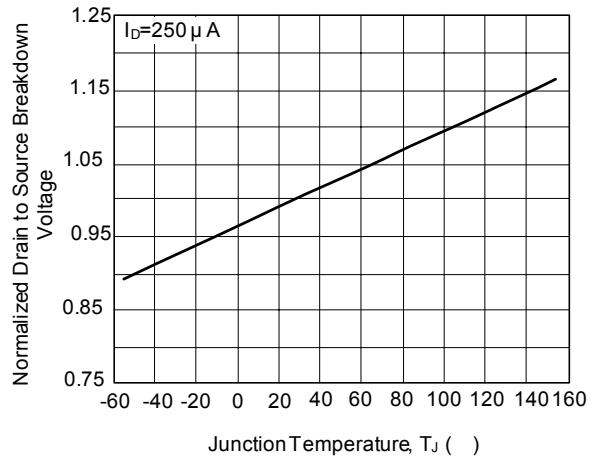


Figure 17. Capacitance vs. Drain to Source Voltage

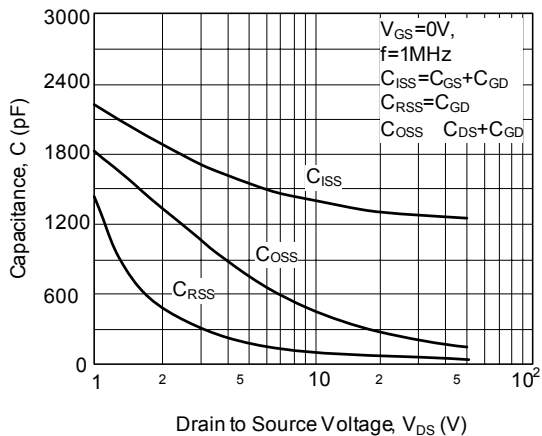
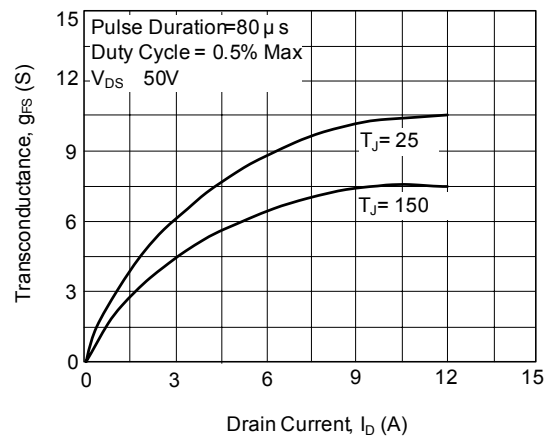


Figure 18. Transconductance vs. Drain Current



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 19. Source to Drain DIODE Voltage

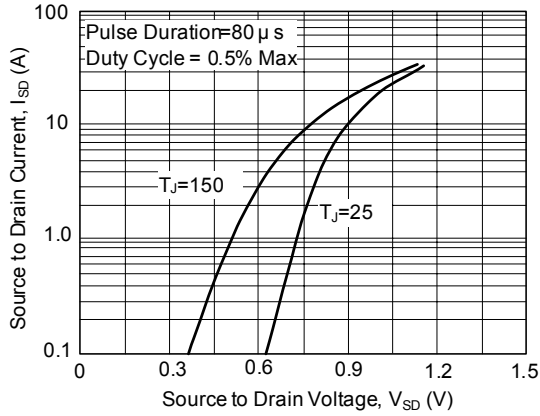
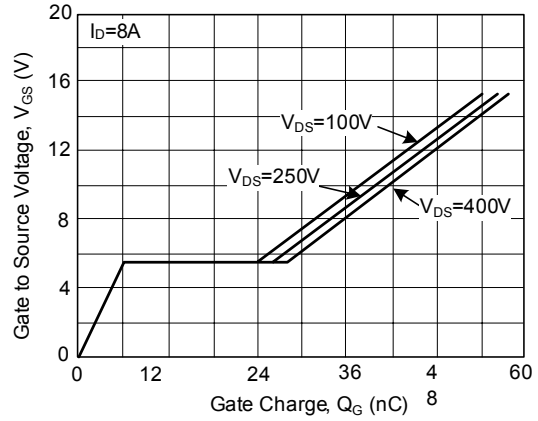


Figure 20. Gate to Source Voltage vs. Gate Charge



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