

P-CHANNEL POWER MOS FET ARRAY  
SWITCHING  
INDUSTRIAL USE

DESCRIPTION

The  $\mu$ PA1523B is P-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- Full Mold Package with 4 Circuits
- -4 V driving is possible
- Low On-state Resistance  
 $R_{DS(on)1} = 0.8 \Omega$  MAX. (@  $V_{GS} = -10$  V,  $I_D = -1$  A)  
 $R_{DS(on)2} = 1.3 \Omega$  MAX. (@  $V_{GS} = -4$  V,  $I_D = -1$  A)
- Low Input Capacitance  $C_{iss} = 190$  pF TYP.

ORDERING INFORMATION

Type Number	Package
$\mu$ PA1523BH	10 Pin SIP

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS(AC)}$	$\mp 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 2.0$	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ *1	$\mp 8.0$	A/unit
Total Power Dissipation	$P_{T1}$ *2	28	W
Total Power Dissipation	$P_{T2}$ *3	3.5	W
Channel Temperature	$T_{CH}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current	$I_{AS}$ *4	-2.0	A
Single Avalanche Energy	$E_{AS}$ *4	0.4	mJ

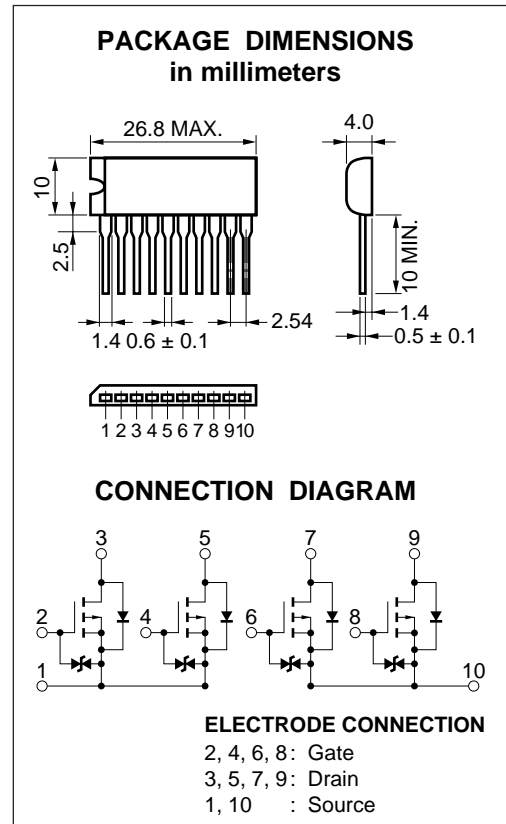
\*1  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

\*2 4 Circuits,  $T_C = 25^\circ\text{C}$

\*3 4 Circuits,  $T_A = 25^\circ\text{C}$

\*4 Starting  $T_{CH} = 25^\circ\text{C}$ ,  $V_{DD} = -30$  V,  $V_{GS} = -20$  V  $\rightarrow$  0,  $R_G = 25 \Omega$ ,  
 $L = 100 \mu H$

Build-in Gate Diodes are for protection from static electricity in handling.  
 In case high voltage over  $V_{GSS}$  is applied, please append gate protection circuits.

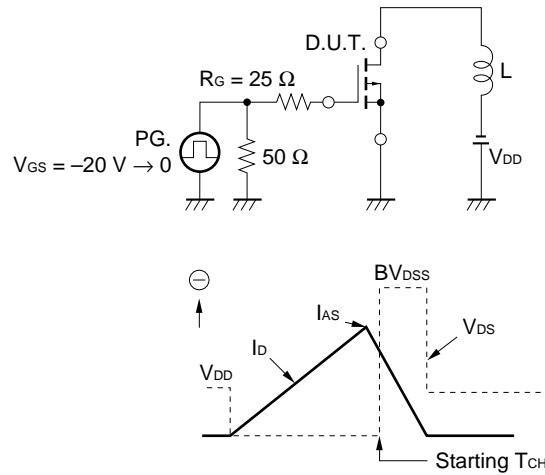


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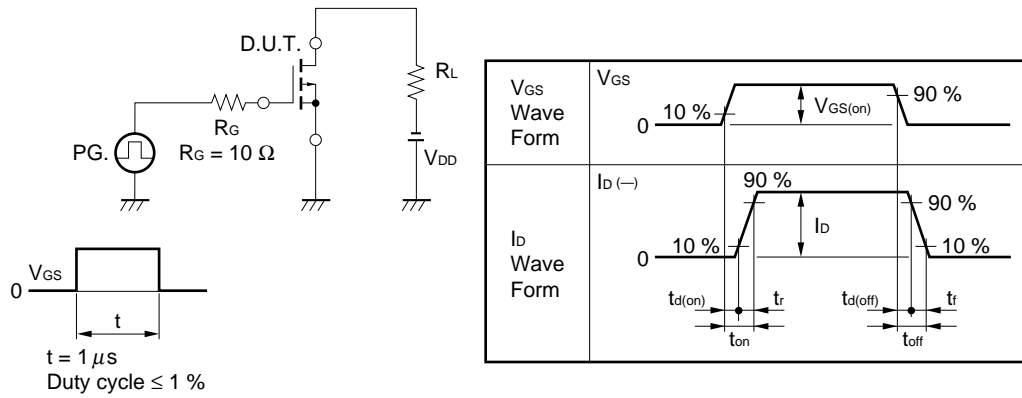
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Gate Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 mA	-1.0		-2.0	V
Forward Transfer Admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 A	0.8			S
Drain to Source ON-Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A		0.5	0.8	Ω
Drain to Source ON-Resistance	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -1.0 A		0.8	1.3	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1.0 MHz		190		pF
Output Capacitance	C <sub>oss</sub>			115		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			43		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -1.0 A, V <sub>GS(on)</sub> = -10 V, V <sub>DD</sub> ≐ -30 V, R <sub>L</sub> = 30 Ω		8		ns
Rise Time	t <sub>r</sub>			53		ns
Turn-off Delay Time	t <sub>d(off)</sub>			400		ns
Fall Time	t <sub>f</sub>			230		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.0 A, V <sub>DD</sub> = -48 V		10		nC
Gate to Source Charge	Q <sub>GS</sub>			1.1		nC
Gate to Drain Charge	Q <sub>GD</sub>			3.5		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0, di/dt = 50 A/μs		180		ns
Reverse Recovery Charge	Q <sub>rr</sub>			250		nC

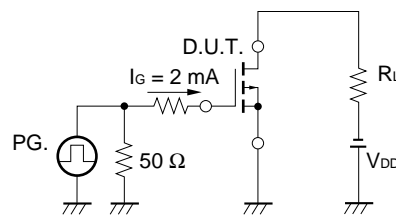
**Test Circuit 1 Avalanche Capability**



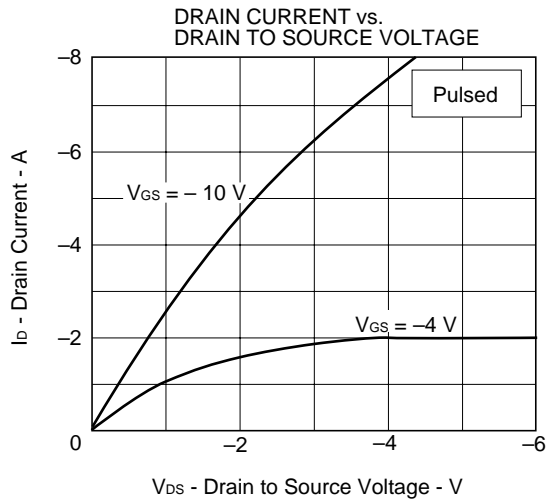
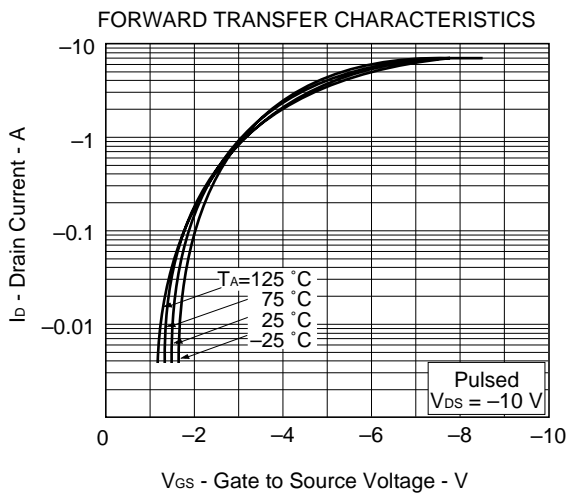
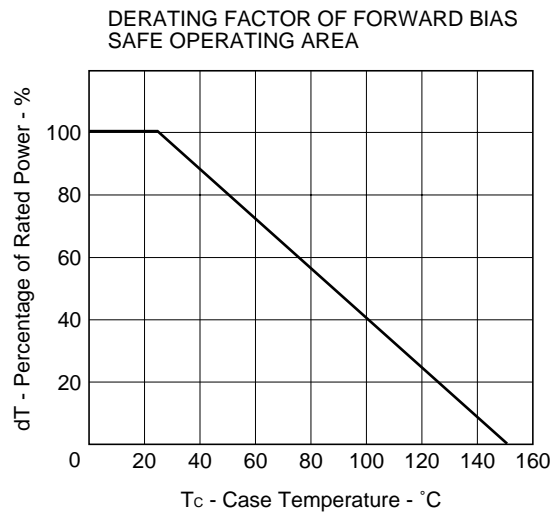
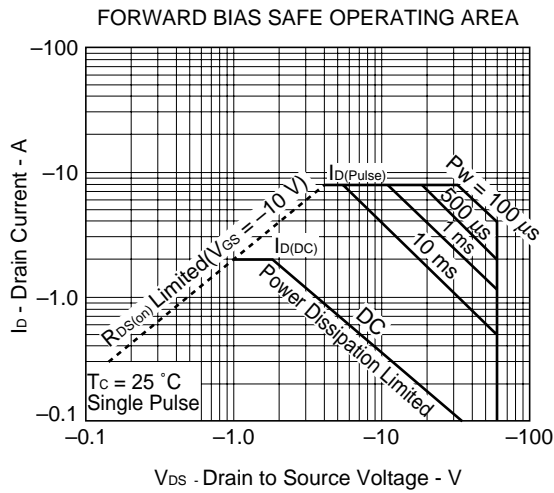
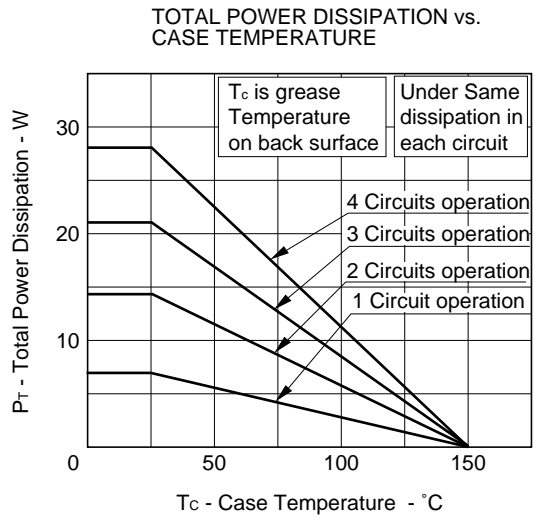
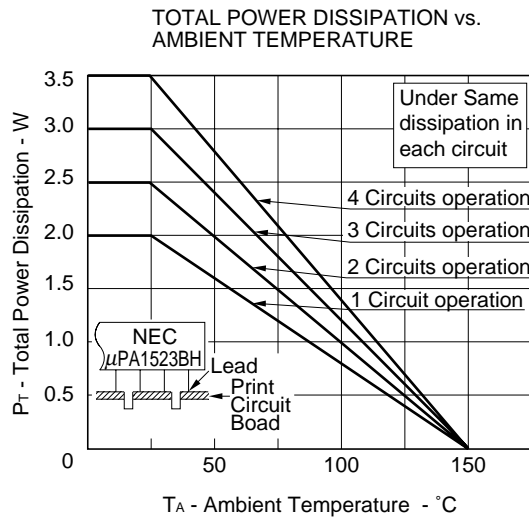
**Test Circuit 2 Switching Time**



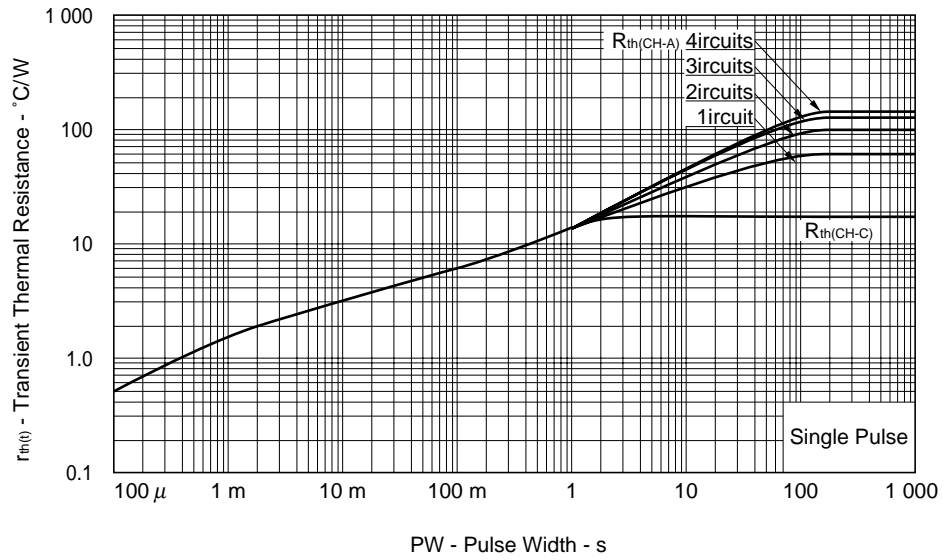
**Test Circuit 3 Gate Charge**



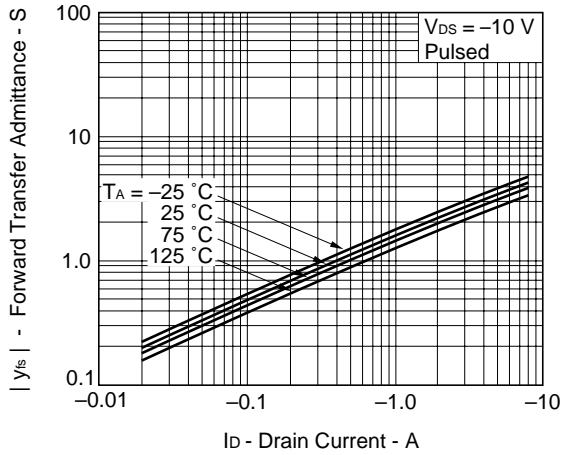
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



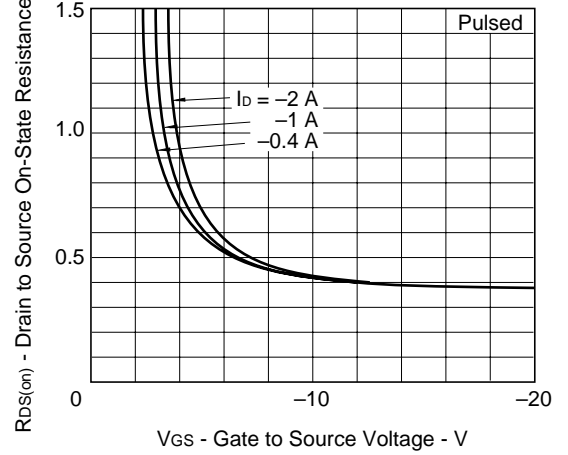
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



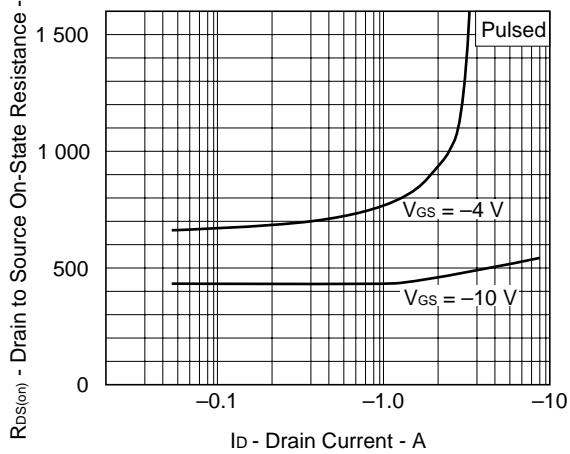
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



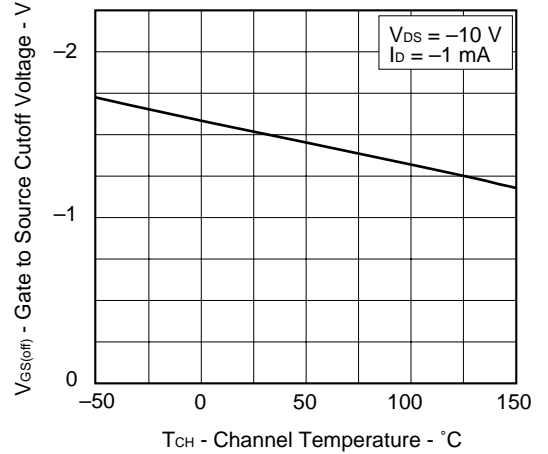
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

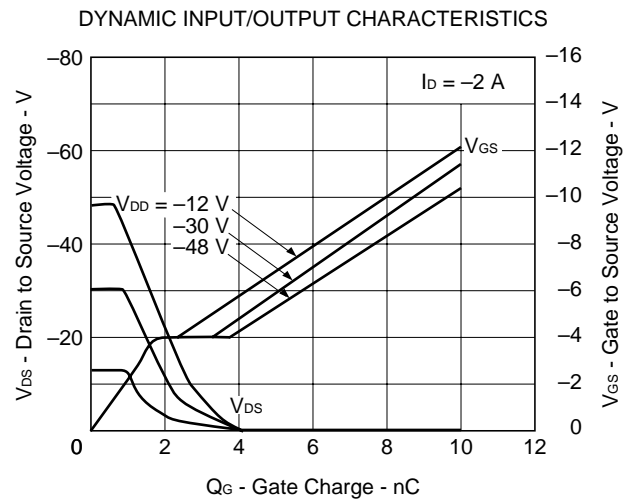
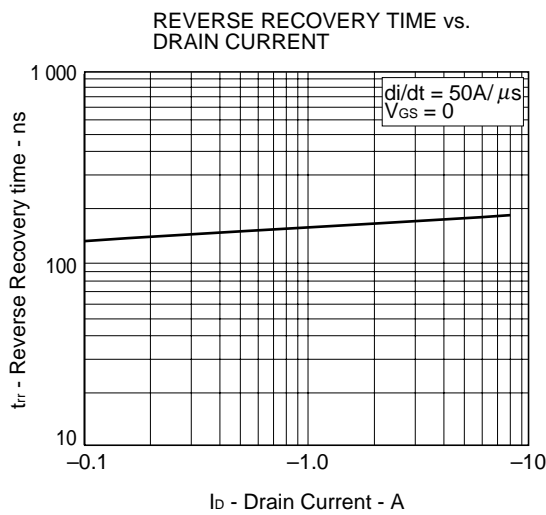
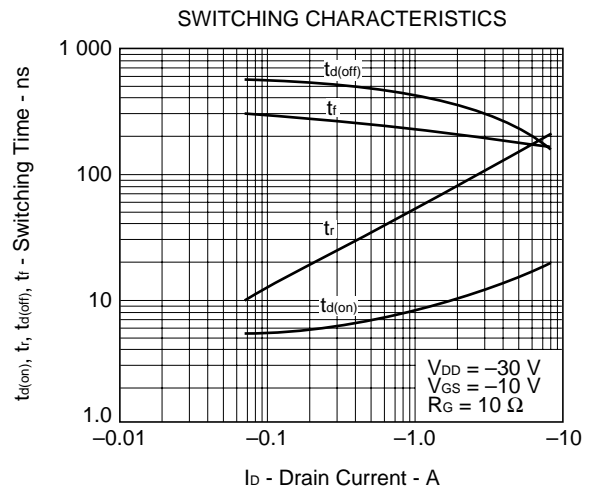
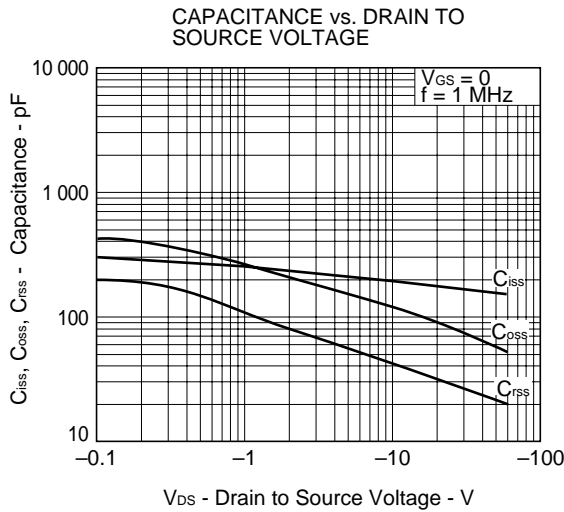
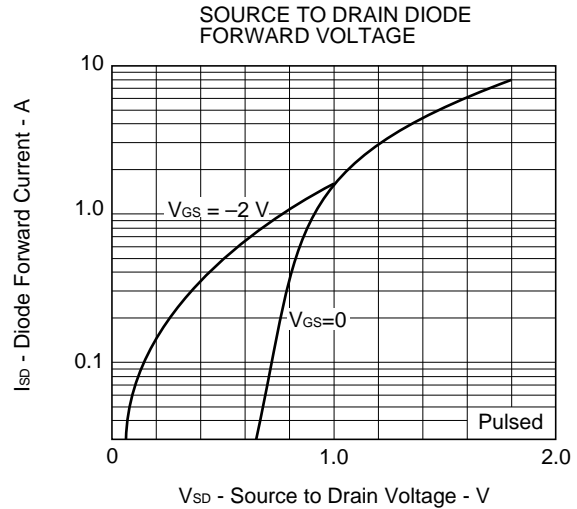
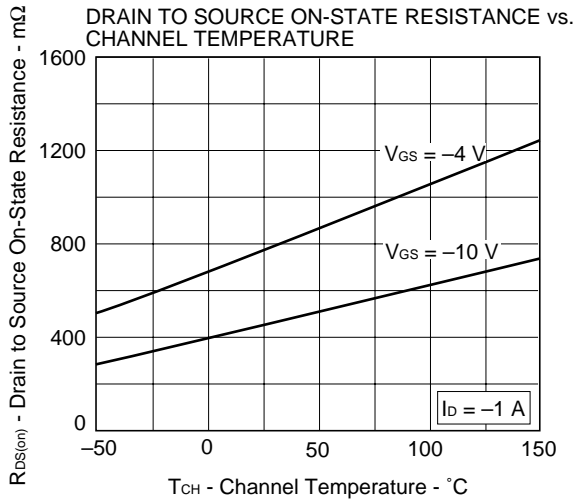


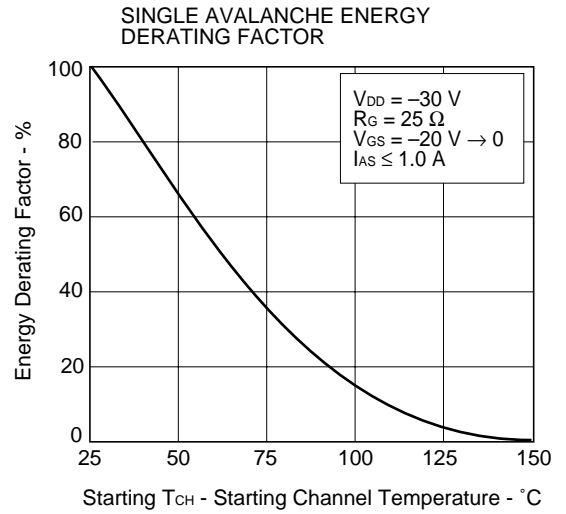
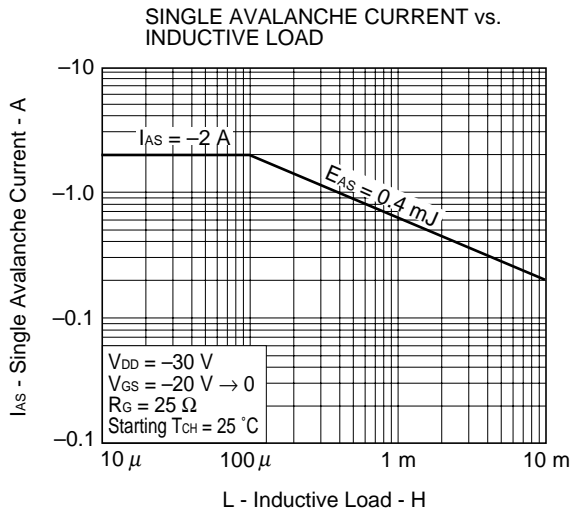
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







REFERENCE

Document Name	Document No.
NEC semiconductor for device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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