

FEATURES

- **SMALL PACKAGE OUTLINE:**
SOT-363 package measures just 2 mm x 1.25 mm
- **LOW HEIGHT PROFILE:**
Just 0.60 mm high
- **HIGH COLLECTOR CURRENT:**
Ic MAX = 100 mA

DESCRIPTION

The UPA809TF contains two NE688 NPN high frequency silicon bipolar chips. NEC's new low profile TF package is ideal for all portable wireless applications where reducing component height is a prime consideration. Each transistor chip is independently mounted and easily configured for two stage cascade LNAs and other similar applications.

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcbo	Collector to Base Voltage	V	9
Vceo	Collector to Emitter Voltage	V	6
Vebo	Emitter to Base Voltage	V	2
Ic	Collector Current	mA	100
PT	Total Power Dissipation		
	1 Die	mW	110
	2 Die	mW	200
Tj	Junction Temperature	°C	150
Tstg	Storage Temperature	°C	-65 to +150

Note:

1. Operation in excess of any one of these parameters may result in permanent damage.

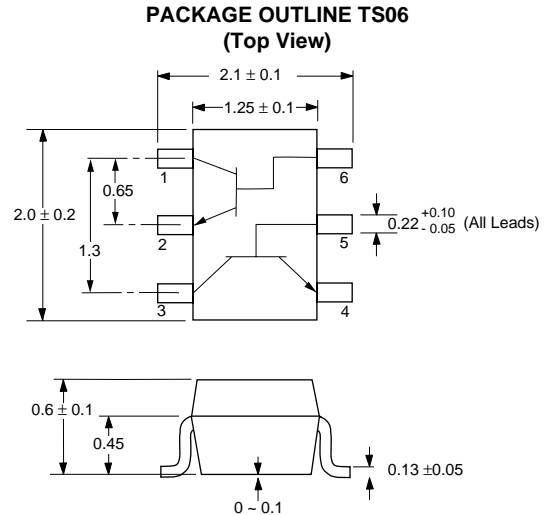
ELECTRICAL CHARACTERISTICS (TA = 25°C)

PART NUMBER PACKAGE OUTLINE			UPA809TF TS06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Icbo	Collector Cutoff Current at Vcb = 5V, Ie = 0	µA			0.1
Iebo	Emitter Cutoff Current at Veb = 1V, Ic = 0	µA			0.1
hFE	Forward Current Gain ¹ at Vce = 1V, Ic = 3mA		80	110	160
ft	Gain Bandwidth at Vce = 3V, Ic = 20mA, f = 2GHz	GHz		9.0	
Cre	Feedback Capacitance ² at Vcb = 1V, Ie = 0, f = 1MHz	pF		0.75	0.85
S21E ²	Insertion Power Gain at Vce = 3V, Ic = 20mA, f = 2GHz	dB		6.5	
NF	Noise Figure at Vce = 3V, Ic = 7mA, f = 2GHz	dB		1.5	
hFE1/hFE2	hFE Ratio: hFE1 = Smaller Value of Q1, or Q2 hFE2 = Larger Value of Q1 or Q2		0.85		

Notes: 1. Pulsed measurement, pulse width ≤ 350 µs, duty cycle ≤ 2 %.

2. The emitter terminal should be connected to the ground terminal of the 3 terminal capacitance bridge. For Tape and Reel version use part number UPA809TF-T1, 3K per reel.

OUTLINE DIMENSIONS (Units in mm)



PIN OUT

1. Collector Transistor 1
2. Emitter Transistor 1
3. Collector Transistor 2
4. Emitter Transistor 2
5. Base Transistor 2
6. Base Transistor 1

Note:

Pin 1 is the lower left most pin as the package lettering is oriented and read left to right.