PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8158K

RF UP-CONVERTER WITH AGC FUNCTION + IF QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

DESCRIPTION

The μPC8158K is a silicon microwave monolithic integrated circuit designed as quadrature modulator for digital mobile communication systems. This MMIC consists of 0.8 GHz to 1.5 GHz up-converter and 100 MHz to 300 MHz quadrature modulator which are equipped with AGC and power save functions. This configuration suits to IF modulation system. The package is 28-pin QFN suitable for high density mounting. The chip is manufactured using NEC's. 20 GHz f_T silicon bipolar process NESAT™ III to realize low power consumption. Consequently the μPC8158K can contribute to make RF blocks smaller size, higher performance and lower power consumption.

FEATURES

- Supply voltage: V_{CC} = 2.7 to 4.0 V, I_{CC} = 28 mA @ V_{CC} = 3.0 V
- Built-in LPF suppresses spurious multipled by TX local (LO1)
- AGC amplifier is installed in local port of up converter: GCR = 35 dB MIN. @ fout = 1.5 GHz
- Excellent performance: P_{adj} = –65 dBc TYP. @ Δf = ±50 kHz, EVM = 1.2 % rms TYP.
- External IF filter can be applied between modulator output and up converter input terminal.

APPLICATIONS

- Digital cellular phones (PDC800M, PDC1.5G and so on)

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8158K-E1	28-pin plastic QFN (5.1 × 5.5 × 0.95 mm)	Embossed tape 12 mm wide. Pin 1 is in pull-out direction. QTY 2.5 kp/Reel.

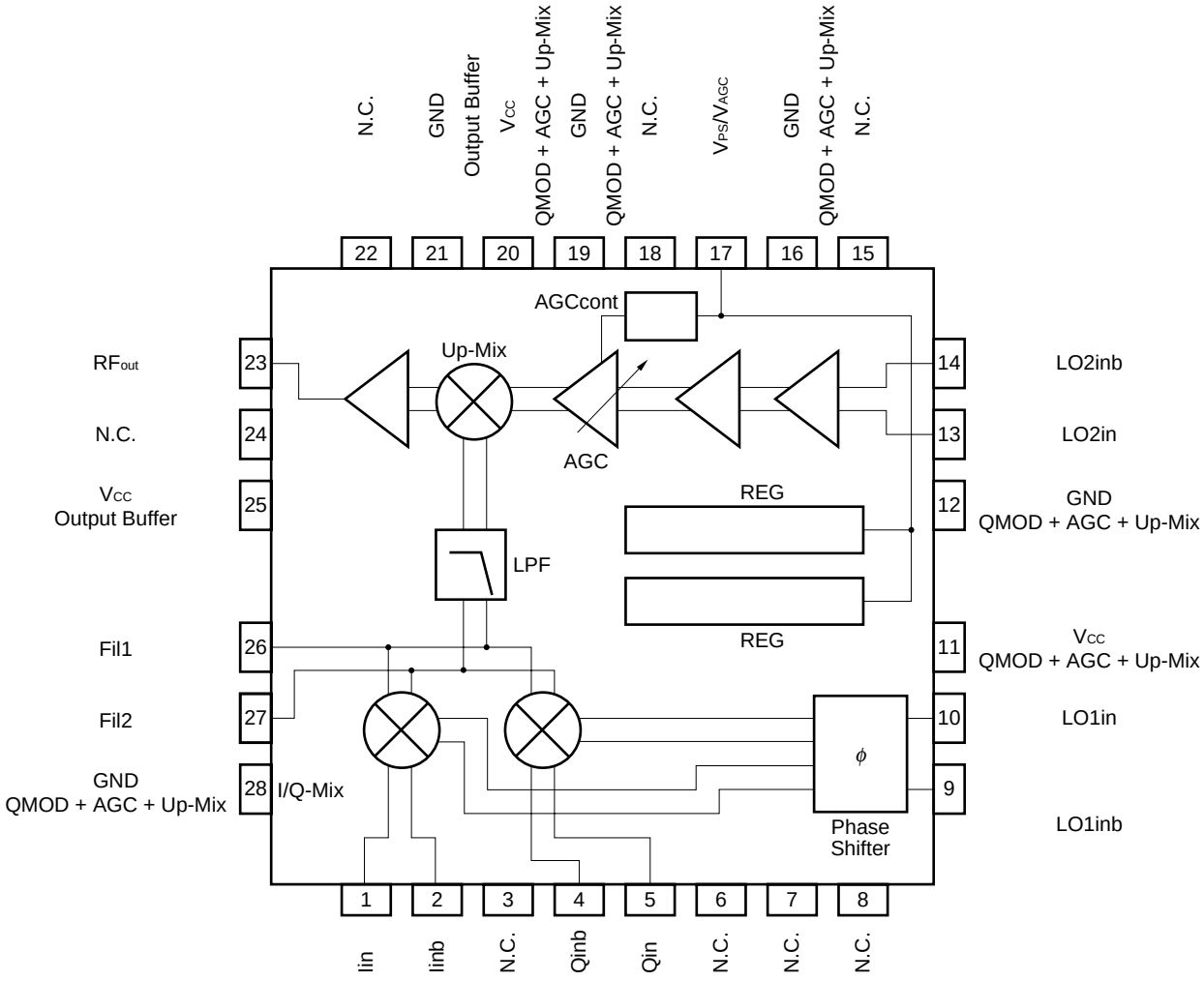
Remark To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPC8158K)

Caution Electro-static sensitive device

The information in this document is subject to change without notice.

Document No. P13831EJ1V1DS00 (1st edition)
Date Published January 1999 N CP(K)
Printed in Japan

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (TOP View)



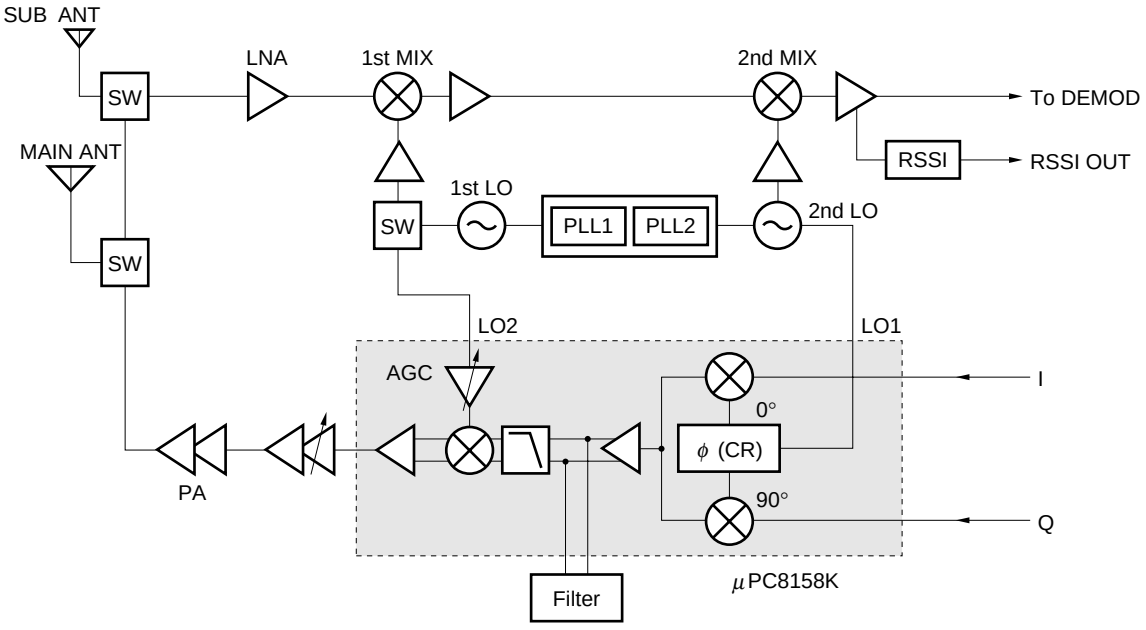
QUADRATURE MODULATOR SERIES

Part Number	Functions	I_{CC} (mA)	f_{LO1in} (MHz)	f_{MODout} (MHz)	Up-Converter f_{RFout} (MHz)	Phase Shifter	Package	Application
μPC8101GR	150 MHz Quad. Mod	15/@ 2.7 V	100 to 300	50 to 150	External	F/F	20-pin SSOP (225 mil)	CT-2, etc.
μPC8104GR	RF Up-Converter + IF Quad. Mod	28/@ 3.0 V	100 to 400		900 to 1 900	Doubler + F/F		Digital Comm.
μPC8105GR	400 MHz Quad. Mod	16/@ 3.0 V	100 to 400		External		16-pin SSOP (225 mil)	
μPC8110GR	1GHz Direct Quad. Mod	24/@ 3.0 V	800 to 1 000		Direct		20-pin SSOP (225 mil)	PDC800 MHz, etc.
μPC8125GR	RF Up-Converter + IF Quad. Mod + AGC	36/@ 3.0 V	220 to 270		1 800 to 2 000			PHS
μPC8126GR	900 MHz Direct Quad. Mod with Offset-Mixer	35/@ 3.0 V	915 to 960		915 to 960 (LO pre-mixer)			PDC800 MHz
μPC8126K			889 to 960				28-pin QFN	
μPC8129GR	×2LO IF Quad. Mod + RF Up-Converter	28/@ 3.0 V	200 to 800	100 to 400	800 to 1900	F/F	20-pin SSOP (225 mil)	GSM, DCS1800, etc.
μPC8139GR-7JH	Transceiver IC (1.9 GHz Indirect Quad. Mod + RX-IF + IF VCO)	TX: 32.5 RX: 4.8 /@ 3.0 V	220 to 270		1 800 to 2 000	CR	30-pin TSSOP (225 mil)	PHS
μPC8158K	RF Up-Converter + IF Quad. Mod + AGC	28/@ 3.0 V	100 to 300		800 to 1 500		28-pin QFN	PDC800 M/ 1.5 G

For outline of the quadrature modulator series, please refer to the application note 'Usage of μPC8101, 8104, 8105, 8125, 8129' (Document No. P13251E) and so on.

SYSTEM APPLICATION EXAMPLE

[PDC800 MHz/1.5 GHz]



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	Pin11, 20 and 25, T_A = +25°C	5.0	V
Power Save and AGC Control Pin Applied Voltage	V_{PS}/V_{AGC}	Pin17, T_A = +25°C	5.0	V
Power Dissipation	P_D	T_A = +85°C[Note]	430	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

Note Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	Pin11, 20 and 25	2.7	3.0	4.0	V
Power Save Voltage	V_{PS}	Pin17	0	–	0.3	V
AGC Control Voltage	V_{AGCPS}	Pin17	1.0	–	2.5	V
Operating Ambient Temperature	T_A		–30	+25	+80	°C
Up-converter RF Output Frequency	f_{RFout}		800	–	1500	MHz
LO2 Input Frequency	f_{LO2in}	P_{LO2in} = –15 dBm	600	–	1750	MHz
I/Q Input Frequency	$f_{I/Qin}$	$V_{I/Qin}$ = 500 mV_{P-P} MAX. (Differential input)	DC	–	10	MHz
LO1 Input Level	P_{LO1in}		–18	–15	–12	dBm
LO2 Input Level	P_{LO2in}		–18	–15	–12	dBm
I/Q Input Amplitude	$V_{I/Qin}$	I, Ib, Q, Qb each	–	420	500	mV_{P-P}
Up-converter Input Frequency	$f_{UPCONin}$		100	–	300	MHz
Modulator Output Frequency	f_{MODout}					
LO1 Input Frequency	f_{LO1in}	P_{LO1in} = –15 dBm				

ELECTRICAL CHARACTERISTICS

Conditions (Unless otherwise specified):

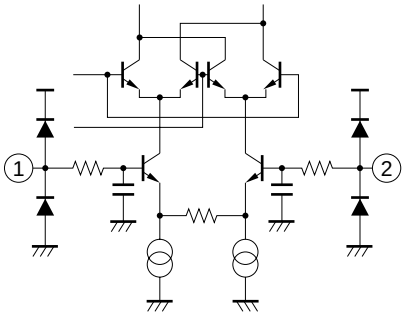
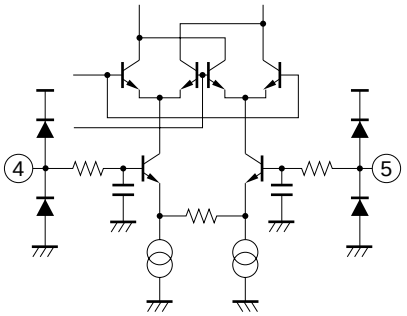
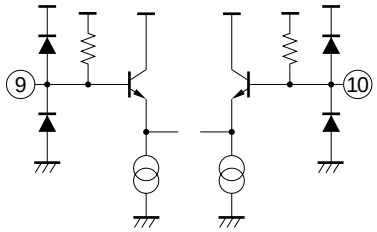
T_A = +25 °C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 3.0 V, V_{PS}/V_{AGC} = 2.5 V,
I/Q (DC) = Ib/Qb (DC) = $V_{CC}/2$ = 1.5 V, $V_{I/Ibin} = V_{Q/Qbin}$ = 500 mV_{P-P} (each), $f_{I/Qin}$ = 2.625 kHz,
π/4DQPSK wave input, transmission rate 42 kbps, filter roll-off α = 0.5,
Modulation Pattern: <0000>
f_{LO1in} = 178.05 MHz, P_{LO1in} = –15 dBm
f_{LO2in} = 1619.05 MHz, P_{LO2in} = –15 dBm
$f_{RFout} = 1441\ MHz - f_{I/Qin}$

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
UP-CONVERTER + QUADRATURE MODULATOR TOTAL						
Total Circuit Current	$I_{CC\ (TOTAL)}$	No input signal	23.7	28	37.6	mA
Total Circuit Current at Power Save Mode	$I_{CC\ (PS)\ TOTAL}$	$V_{PS} \leq 0.5$ V (Low), No input signal	–	0.3	10	μA
Total Output Power 1	$P_{RFout}1$	V_{AGC} = 2.5 V	–15	–11.5	–8	dBm
Total Output Power 2	$P_{RFout}2$	V_{AGC} = 1.0 V	–56.5	–52	–46.5	dBm
LO Carrier Leak	LOL	$f_{LOL} = f_{LO1} + f_{LO2}$	–	–40	–30	dBc
Image Rejection (Side Band Leak)	ImR		–	–40	–30	dBc
I/Q 3rd order distortion	$IM_{3\ (I/Q)}$		–	–50	–30	dBc
AGC Gain Control Range	GCR	V_{AGC} = 2 V → 1 V	35	40	–	dB
Error Vector Magnitude	EVM	MOD Pattern: PN9	–	1.2	3.0	%rms
Adjacent channel interference	P_{adj}	Δf = ±50 kHz, MOD Pattern: PN9	–	–65	–60	dBc
Spurious suppression	P_{out} (8fLO1)	fLO1 × 8, fLO1 × 8 (image)[Note]	–	–70	–65	dBc
Power Save Rise Time	$T_{PS\ (Rise)}$	$V_{PS\ (Low)} \rightarrow V_{PS\ (High)}$	–	2	5	μs
Power Save Fall Time	$T_{PS\ (Fall)}$	$V_{PS\ (High)} \rightarrow V_{PS\ (Low)}$	–	2	5	μs
I/Q input impedance	$Z_{I/Q}$	Between pin I/Ib, Q/Qb	80	200	–	kΩ
I/Q input bias current	$I_{I/Q}$	Between pin I/Ib, Q/Qb	–	5	13	μA
LO1 input VSWR	Z_{LO1}	f_{LO1} = 100 M to 300 MHz	–	1.5:1	–	–

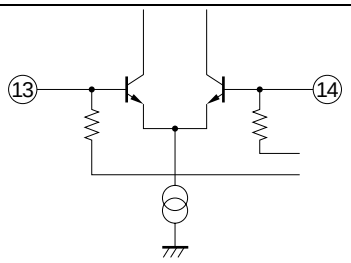
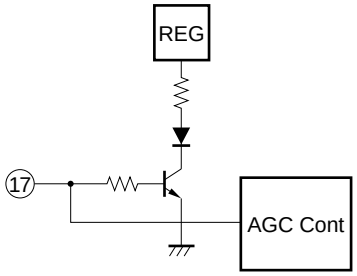
Note Without external LC between Fil1 and Fil2 pin on this frequency conditions.
Spectrum analyzer conditions: VBW = 300 Hz, RBW = 300 Hz.

Remark Electrical characteristics in this document is described for 1.5 GHz system.

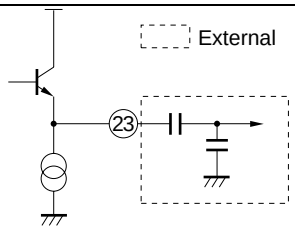
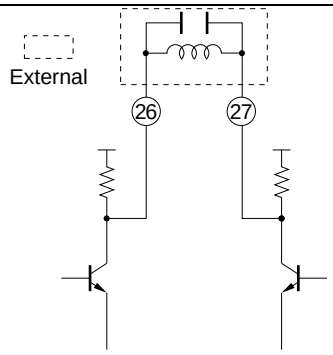
PIN EXPLANATIONS

Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V)[Note]	Function and Application	Internal Equivalent Circuit
1	Iin	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended, amplitude of the signal is 500 m V_{P-P} max.	
2	Iinb	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended, V_{CC}/2 biased DC signal should be input. In the case of the I/Q input signals are differential, amplitude of the signal is 500 m V_{P-P} max.	
3	N.C.	–	–	This pin is not connected to internal circuit. This pin should be opened or grounded.	
4	Qinb	V_{CC}/2	–	Input for Q signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended, amplitude of the signal is 500 m V_{P-P} max.	
5	Qin	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended, V_{CC}/2 biased DC signal should be input. In case of the I/Q input signals are differential, amplitude of the signal is 500 m V_{P-P} max.	
6	N.C.	–	–	These pins are not connected to internal circuit. These pins should be opened or grounded.	
7	N.C.				
8	N.C.				
9	LO1inb	–	2.98	Bypass pin of modulator's local input. This pin should be decoupled with 330 pF capacitor.	
10	LO1in	–	2.98	Local signal input for modulator. This pin must be coupled with DC cut capacitor 330 pF and should be terminated with 51 Ω resistor.	
11	V_{CC}	2.7 to 4.0	–	Supply voltage pin for modulator, up-converter and AGC circuits.	

Note Pin Voltages are measured on V_{CC} = 3.0 V.

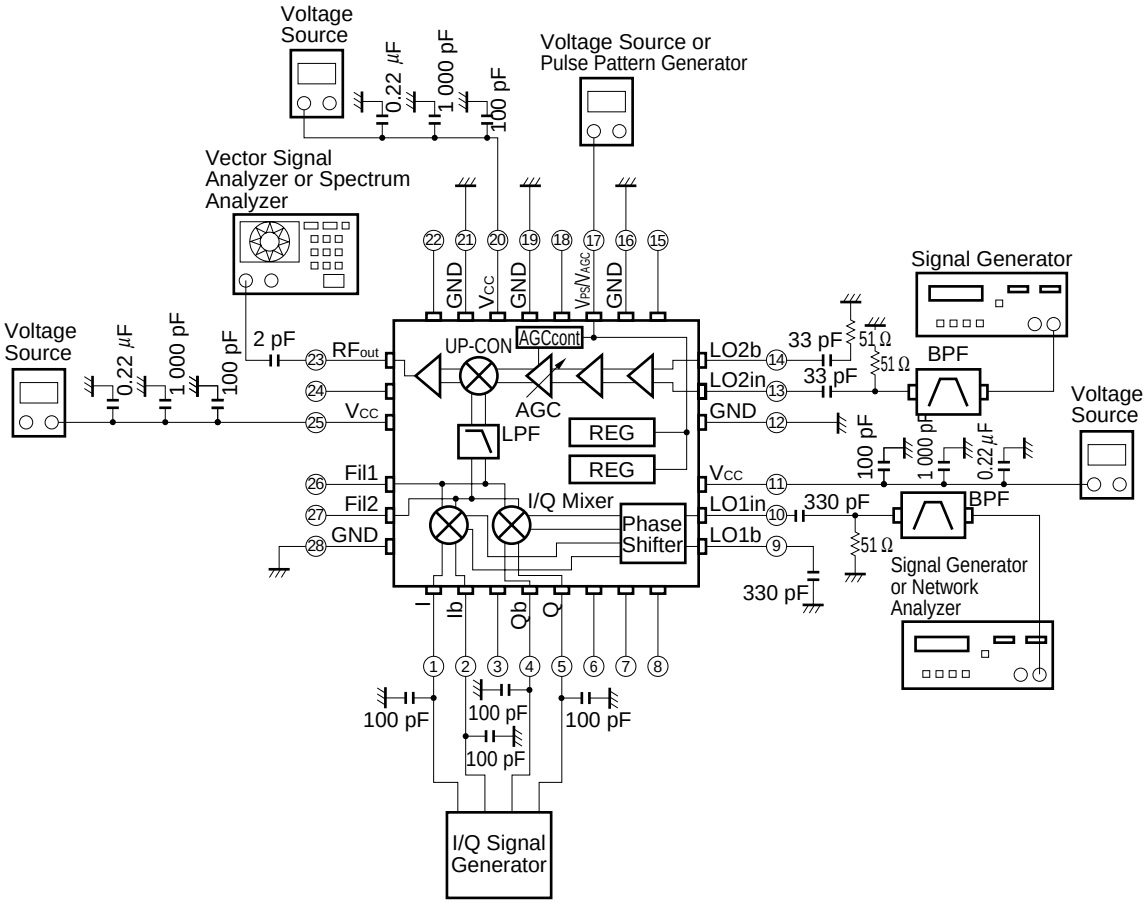
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage (V)</th><th>Pin Voltage (V)^{Note}</th><th>Function and Application</th><th>Internal Equivalent Circuit</th></tr>
<tr><td>12</td><td>GND</td><td>0</td><td>–</td><td>Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.</td><td></td></tr>
<tr><td>13</td><td>LO2in</td><td>–</td><td>1.8</td><td>Local signal input for modulator. This pin must be coupled with DC cut capacitor 33 pF and should be terminated with 51 Ω resistor.</td><td rowspan="2"> 
</td></tr>
<tr><td>14</td><td>LO2inb</td><td>–</td><td>1.8</td><td>Bypass pin of up-converter's local signal input. This pin should be decoupled with 33 pF capacitor.</td></tr>
<tr><td>15</td><td>N.C.</td><td>–</td><td>–</td><td>This pin is not connected to internal circuit. This pin should be opened or grounded.</td><td></td></tr>
<tr><td>16</td><td>GND</td><td>0</td><td>–</td><td>Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance.</td><td></td></tr>
<tr><td>17</td><td>V_{PS}/V_{AGC}</td><td>V_{PS}/V_{AGC}</td><td>–</td><td>Power save control pin for modulator, up-converter and AGC circuits. This pin also assigned as gain control pin for AGC circuits. Operation status with applied voltages are as follows.
<table>
<tr><th>V_{PS}/V_{AGC} (V)</th><th>STATE</th></tr>
<tr><td>0 to 0.4</td><td>OFF (Sleep Mode)</td></tr>
<tr><td>1 to 2.5</td><td>On (AGC Mode)</td></tr>
</table></td><td> 
</td></tr>
<tr><td>18</td><td>N.C.</td><td>–</td><td>–</td><td>This pin is not connected to internal circuit. This pin should be opened or grounded.</td><td></td></tr>
<tr><td>19</td><td>GND</td><td>0</td><td>–</td><td>Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance.</td><td></td></tr>
<tr><td>20</td><td>V_{CC}</td><td>2.7 to 4.0</td><td>–</td><td>Supply voltage pin for modulator, up-converter and AGC circuits.</td><td></td></tr>
<tr><td>21</td><td>GND</td><td>0</td><td>–</td><td>Ground pin for RF output buffer. This pin should be grounded with minimum inductance.</td><td></td></tr>
</table>

Note Pin Voltages are measured on V_{CC} = 3.0 V.

Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) Note	Function and Application	Internal Equivalent Circuit
22	N.C.	–	–	This pin is not connected to internal circuit. This pin should be opened or grounded.	
23	RFout	–	1.75	RF output pin. This pin is emitter follower which is low impedance output port. This pin can be easily matched to 50 Ω impedance using external coupling and decoupling capacitors.	
24	N.C.	–	–	These pins are not connected to internal circuit. These pins should be opened or grounded.	
25	V_{CC}	2.7 to 4.0	–	Supply voltage pin for RF output buffer.	
26	Fil1	–	2.76	External inductor and capacitor can supress harmonics spurious of LO1 frequency. LC value should be determined according to LO1 input frequency and suppression level.	
27	Fil2	–	2.76		
28	GND	0	–	Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	

Note Pin Voltages are measured on V_{CC} = 3.0 V.

TEST CIRCUIT



TEST CONDITIONS

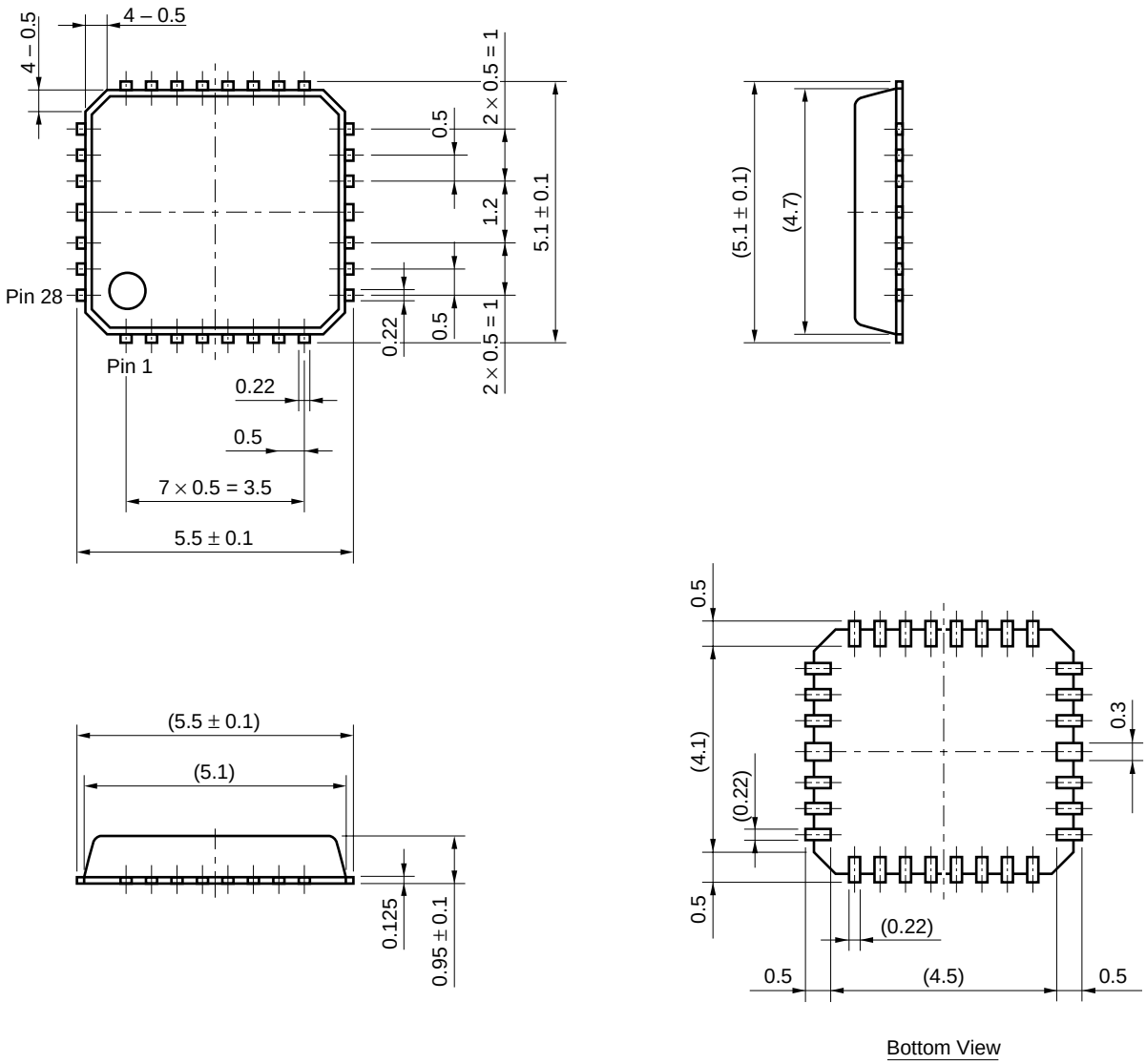
f_{LO1in} = 178.05 MHz, P_{LO1in} = –15 dBm

f_{LO2in} = 1619.05 MHz, P_{LO2in} = –15 dBm

f_{RFout} = 1441 MHz – $f_{I/Qin}$

PACKAGE DIMENSIONS

28 pin plastic QFN (UNIT: mm)



Bottom View

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPC8158K

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 2, Exposure limit[Note]: None	IR35-00-2
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit[Note]: None	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

ATTENTION
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FOR HANDLING
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SENSITIVE
DEVICES

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M4 96.5