NEC

MOS INTEGRATED CIRCUIT
μPD16662

240 OUTPUT LCD COLUMN (SEGMENT) DRIVER WITH BUILT-IN RAM

The μPD16662 is a column (segment) driver which contains a RAM capable of full dot LCD drive.

With 240 outputs, this driver has a display RAM of 240 x 160 x 2 bits built in, and 4 gray scales of display are possible. Any 4 gray scales can be selected from 25 levels of the gray scale pallet. The driver can be combined with the μPD16667 to display from 240 x 160 dots to 480 x 320 dots.

Features

• Display RAM incorporated: 240 x 160 x 2 bits

• Logic voltage: 3.0V to 3.6V

• Duty: 1/160

• Output count: 240 outputs

• Capable of gray scale display: 4 gray scales (can be selected from 25 levels of the gray scale pallet)

• Memory management: packed pixel system

• 8/16-bit data base

Ordering Information

Part number	Package
μPD16662N -xxx	TCP(TAB)
μPD16662N - 051	Standard TCP (OLB: 0.2 mm pitch; folding)

★

The TCP's external shape is custom-ordered. Therefore, if you have a shape in mind, please contact an NEC salesperson.

**The information in this document is subject to change without notice.**

The mark ★ shows major revised points.

Pin name

Classification	Voltage	Pin Name[Note]	I/O	Function
CPU I/F	3.3 V	D0 to D15	I/O	Data bus 16
		A0 to A16	I	Address bus 17
		/CS	I	Chip select
		/OE	I	Read signal
		/WE	I	Write signal
		/UBE	I	High byte enable
		RDY	O	Ready signal to CPU (Ready state at H)
Control signals	3.3 V	PL0	I	Specifies the LSI allocation locations (No. 0 to 3).
		PL1	I	Specifies the LSI allocation locations (No. 0 to 3).
		DIR	I	Specifies the liquid-crystal panel allocation direction (longitudinal; lateral)
		MS	I	Master/slave switching (Master mode at H)
		BMODE	I	Data bus bit select pin ("H" = 8bit, "L" = 16bit)
		/REFRH	I/O	Self diagnostic reset pin (Wired OR connection)
		TEST	I	Test pin (Test mode at H, using the pull-down buffer)
		/RESET	I	Reset
		/DOFF	I	Display OFF signal input
		OSC1	-	Oscillator pin
		OSC2	-	Oscillator pin
	5.0 V	STB	I/O	Column driving signal strobe (MS signal "H" = output, MS signal "L" = input)
		/FRM	I/O	Frame signal(MS pin "H" = output , MS pin "L" = input)
		PULSE	I/O	25-gray level pulse modulation clock
		L1	I/O	Row driver drive level selection signal (1st line)
		L2	I/O	Row driver drive level selection signal (2nd line)
		/DOUT	O	Display OFF signal output
Liquid-crystal drive		Y1 to Y240	O	Liquid-crystal drive output
Powers		GND	-	Ground (two 5-V pins; three 3-V pins)
		V_{CC1}	-	5-V power level
		V_{CC2}	-	3.3-V power level
		V_0	-	Liquid-crystal drive analog power
		V_1	-	Liquid-crystal drive analog power
		V_2	-	Liquid-crystal drive analog power

Remark /xxx indicates active low signal.

Note 3.3-V power pins : D0 - D15, A0 - A16, /CS, /OE, /WE, /UBE, RDY, BMODE, PL0, PL1, DIR, OSC1, OSC2, /RESET, /DOFF, TEST, MS

5-V power pins : STB, /FRM, L1, L2, /DOUT, PULSE

Block Diagram
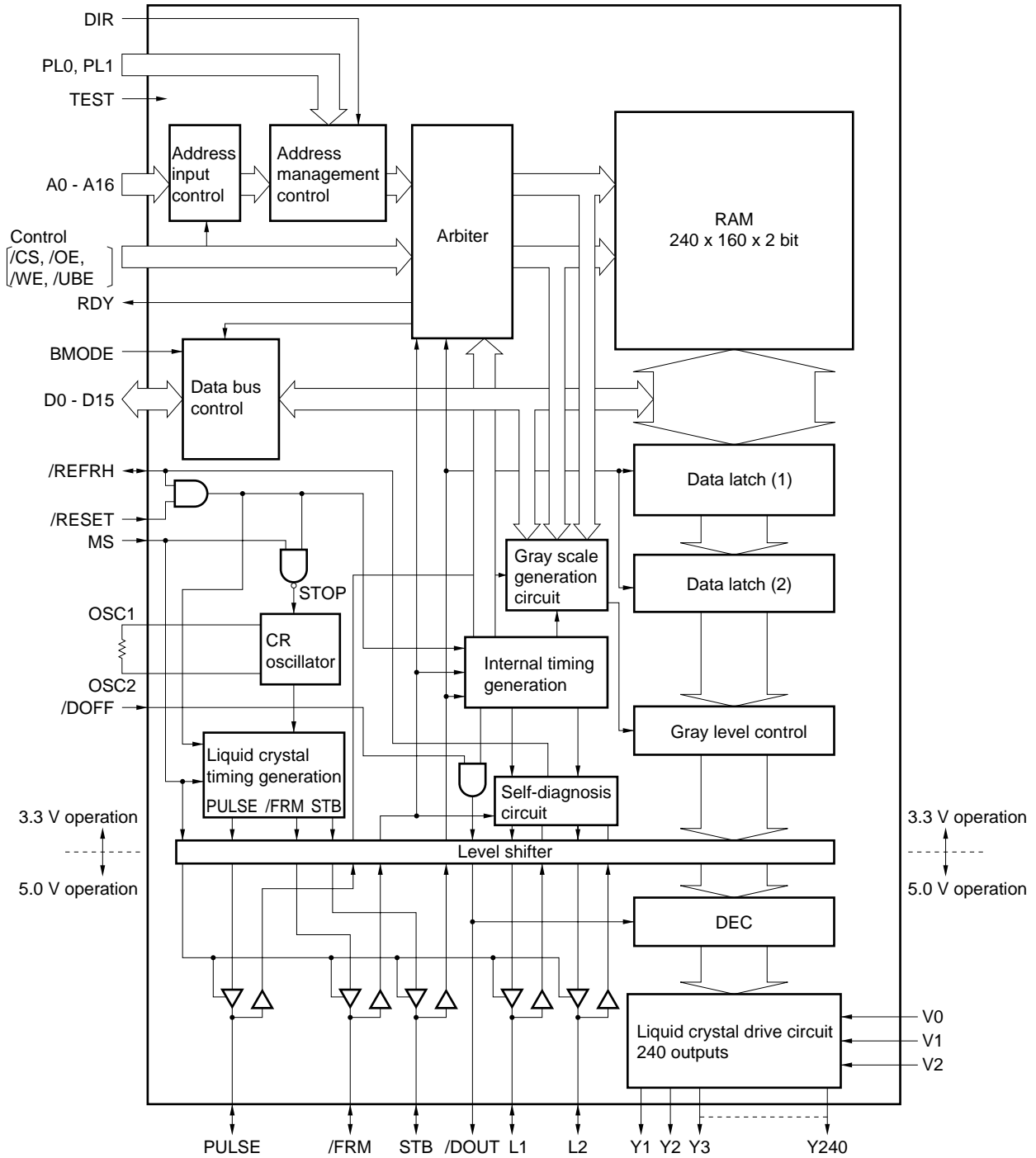
Block Functions

(1) Address management circuit

The address management circuit converts addresses transferred from the system through A0 to A16 into addresses compatible with the memory map of the built-in RAM. This function can be used to address up to 480 x 320 dots with four of these LSIs, thus making it possible to configure a liquid crystal display system without difficulty. Moreover, addresses 1FFF0H to 1FFFFH are allocated to the gray scale pallet register, making it possible to choose any 4 gray scales from the 25-level pallet.

(2) Arbiter

The arbiter adjusts the contention between the RAM access from the system and the RAM read on the liquid-crystal drive side.

(3) RAM

Static RAM (single port) of 240 by 160 by 2 bits

(4) Data bus control

This circuit controls the data transfer directions through the read/write from the system. It also performs an 8/16-bit switch via the BMODE pin.

(5) Gray scale generation circuit

This circuit realizes the 25 levels by frame thinning out and pulse width modulation.

(6) Internal timing generation

Internal timing to each block is generated from /FRM and STB signals.

(7) CR oscillator

The CR oscillator generates the clock which will become a criterion of the frame frequency in master mode. 1/2592 of this oscillation becomes the frame frequency. For example, if the frame frequency is 70 Hz, the required oscillation frequency is 181.44 kHz. As the CR oscillator has a built-in capacitor, adjust the required oscillation frequency with an external resistor.

In slave mode, the oscillation is stopped.

(8) Liquid crystal timing generation

In master mode, /FRM (frame signal), STB (column drive signal strobe), and PULSE (25-gray-scale pallet pulse modulation clock) are generated.

(9) Gray scale control

This circuit realizes a four-gray scale display.

(10) Data latch (1)

Reads and latches 240-pixel data from the RAM.

(11) Data latch (2)

Latches 240-pixel data synchronously with the STB signal.

(12) Level shifter

   The level shifter converts from the operating voltage (3.3 V) of the internal circuit to the liquid-crystal drive circuit and low driver interface voltage (5 V).

(13) DEC

   Decodes the gray scale display data to make it compatible with the liquid-crystal drive voltages V_0, V_1 and V_2 .
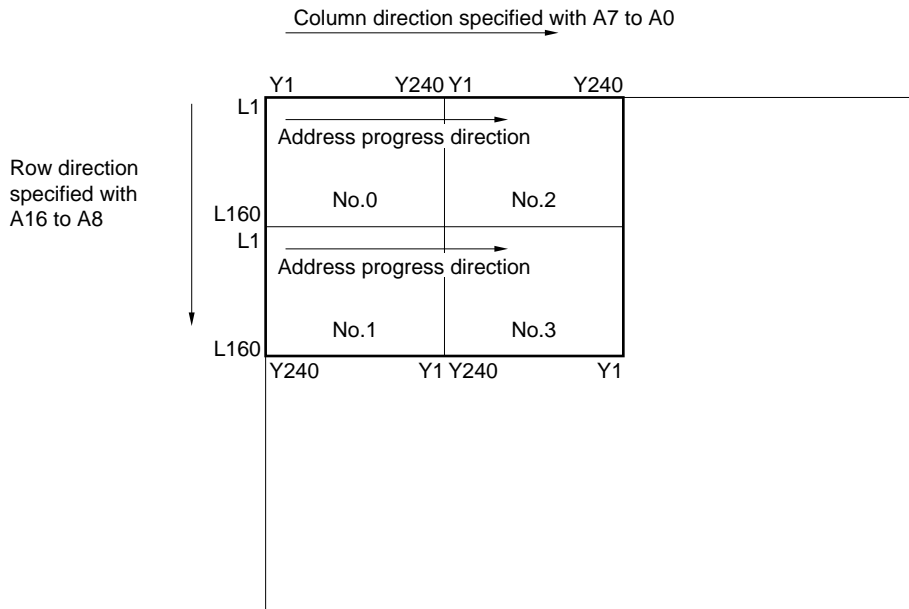
(14) Liquid crystal drive circuit

   This circuit selects one of the liquid-crystal drive powers V_0, V_1, and V_2, which are compatible with the gray scale display data and the display OFF signal (/DOFF), to generate the liquid crystal applied voltage.

(15) Self diagnostic circuit

   If the operation timing of the master chip and slave chip has deviated due to external noise, this circuit will detect the problem and generate a total column/driver refresh signal.

Address map image diagram (Example of VGA-half size configuration)

Column direction specified with A7 to A0

Row direction specified with A16 to A8

	Y1	Y240	Y1	Y240
L1	Address progress direction			
L160	No.0		No.2	
L1	Address progress direction			
L160	No.1		No.3	
	Y240	Y1	Y240	Y1

Data bus

The byte data lined up on the data bus is based on the Little Endian - an NEC/Intel-series bus.

1. 16 bit data bus (BMODE = L)

• Bytes (8 bytes) access

Addresses proceed as → shown on right.

D0 to D7	D8 to D15
00000H	00001H
00002H	00003H
00004H	00005H
⋮	⋮

• Words (16 bits) access

Addresses proceed as → shown on right.

D0 to D7	D8 to D15
00000H	
00002H	
00004H	
⋮	

For the access from the system to be performed in units of words (16 bits), or of bytes (8 bytes), the /UBE (high byte enable) and A0 are used to show whether valid data are in the bytes of either (or both) of D0 to D7 and D8 to D15.

/CS	/OE	/WE	/UBE	A0	MODE	I/O	
						D0 to D7	D8 to D15
H	X	X	X	X	Not Selected	Hi-Z	Hi-Z
L	L	H	L	L	Read	Dout	Dout
			L	H		Hi-Z	Dout
			H	L		Dout	Hi-Z
L	H	L	L	L	Write	Din	Din
			L	H		X	Din
			H	L		Din	X
L	H	H	X	X	Output disable	Hi-Z	Hi-Z
L	X	X	H	H		Hi-Z	Hi-Z

Remark X : Don't Care

Hi-Z : High impedance

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2. 8 bit data bus (BMODE = H)

D0 to D7
00000H
00001H
00002H
⋮

Addresses proceed as →
shown on right.

/CS	/OE	/WE	MODE	I/O	
				D0 to D7	D8 to D15
H	X	X	Not Selected	Hi-Z	Note
L	L	H	Read	Dout	Note
L	H	L	Write	Din	Note
L	H	H	Output disable	Hi-Z	Note

Remark   X   : Don't Care

         Hi-Z : High impedance

Note   Use D8 - D15 and /UBE to open or connect to the GND because they are internally pulled down when
      BMODE = H.

Relationship between data bits and pixels

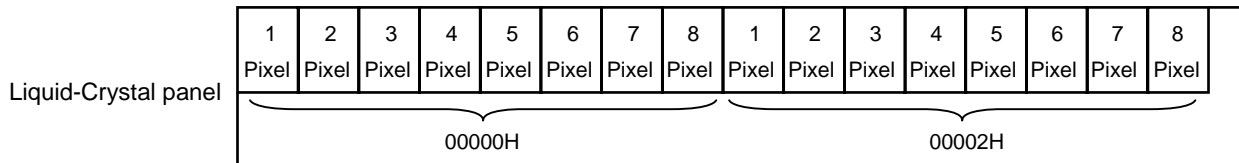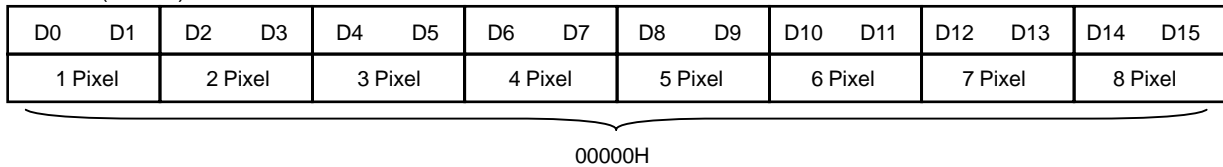As the display is in four gray scales, each pixel consists of two bits.
The RAM is configured with four pixels (8 pixels per word) using the packed pixel system.
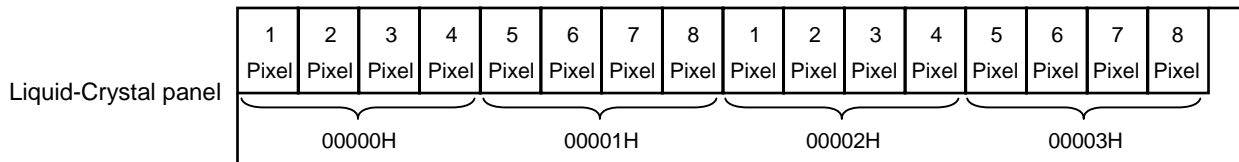
(1) BMODE = L

Bytes (8 bits) access

D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15
1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H   00001H

Liquid-Crystal panel

1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel	1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H   00001H   00002H   00003H

Words (16 bits) access

D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15
1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H

Liquid-Crystal panel

1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel	1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H   00002H

(2) BMODE = H

D0 D1	D2 D3	D4 D5	D6 D7	D0 D1	D2 D3	D4 D5	D6 D7
1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H   00001H

Liquid-Crystal panel

1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel	1 Pixel	2 Pixel	3 Pixel	4 Pixel	5 Pixel	6 Pixel	7 Pixel	8 Pixel

00000H   00001H   00002H   00003H

Gray scale control

The µPD16662 gray scale control realizes 25 levels of the gray scale pallet through frame thinning and pulse width modulation. It chooses four gray scales and records them in the gray scale pallet register before use.

Gray scale pallet register

Through the use of the gray scale pallet register, four gray scales are pre-selected from 25 levels. The gray scale pallet register is allocated in addresses 1FFF0H to 1FFFFH, and the relationship between the register and the gray scale data is shown in the following table. The initial values are also allocated as below. The gray scale pallet register can set each column/driver configuration position (No.0 to 3) decided by PL0 and PL1.

Address	Configuration position	Gray scale data (Display data)		Initial value
	No.	D_{n+1} [Note]	D_n [Note]	
1FFF0H	No.0	0	0	00000B
1FFF1H		0	1	01000B
1FFF2H		1	0	10000B
1FFF3H		1	1	11000B
1FFF4H	No.1	0	0	00000B
1FFF5H		0	1	01000B
1FFF6H		1	0	10000B
1FFF7H		1	1	11000B
1FFF8H	No.2	0	0	00000B
1FFF9H		0	1	01000B
1FFFAH		1	0	10000B
1FFFBH		1	1	11000B
1FFFCH	No.3	0	0	00000B
1FFFDH		0	1	01000B
1FFFEH		1	0	10000B
1FFFFH		1	1	11000B

Note n = 0, 2, 4, 6

Relationship between gray scale and gray scale pallet data

The relationship between the gray scale and the gray scale pallet data that is set by the gray scale pallet register is as follows.

PMODE	Gray scale palette data					Remark
	D4	D3	D2	D1	D0	
Pixel 0	0	0	0	0	0	OFF
Pixel 1	0	0	0	0	1	
Pixel 2	0	0	0	1	0	
Pixel 3	0	0	0	1	1	
Pixel 4	0	0	1	0	0	
Pixel 5	0	0	1	0	1	
Pixel 6	0	0	1	1	0	
Pixel 7	0	0	1	1	1	
Pixel 8	0	1	0	0	0	1/3
Pixel 9	0	1	0	0	1	
Pixel 10	0	1	0	1	0	
Pixel 11	0	1	0	1	1	
Pixel 12	0	1	1	0	0	
Pixel 13	0	1	1	0	1	
Pixel 14	0	1	1	1	0	
Pixel 15	0	1	1	1	1	
Pixel 16	1	0	0	0	0	2/3
Pixel 17	1	0	0	0	1	
Pixel 18	1	0	0	1	0	
Pixel 19	1	0	0	1	1	
Pixel 20	1	0	1	0	0	
Pixel 21	1	0	1	0	1	
Pixel 22	1	0	1	1	0	
Pixel 23	1	0	1	1	1	
Pixel 24	1	1	0	0	0	ON

LSI arrangement and address management

Addresses can be managed to allow up to four of these LSIs to be used to configure a liquid-crystal display of up to half VGA size (320 x 480 dots). Up to four of these LSIs can be connected on the same bus sharing the /CS, /WE, and /OE pins. On the system side, one screen of the liquid crystal display can be treated as one memory area, and it is not necessary to decode for more than one μPD16662. The PL0 and PL1 pins are used to specify LSI No. and to determine the LSI arrangement. The DIR pins are used to determine the directions (vertical, horizontal) of the liquid-crystal display.

PL1	PL0	LSI No.
0	0	No. 0
0	1	No. 1
1	0	No. 2
1	1	No. 3

1. Addresses of the VGA half-size horizontally (DIR = "0")

2. Addresses of the VGA half-size horizontally (DIR = "1")

Specified with A16 to A8

| Row | Row |

Specified with A7 to A0

Column

No.0

X160 Y240
00000
00100
00002
09E00
09F00 X1
09F02
0A000 X160
0A100
13E00
13F00 Y1
13F02

No.1

00038
0003A
0013A
09E3A
09F38
09F3A
0A038
0A03A
0A13A
13E3A
13F38
13F3A

Y240 Y1
Y240 Y1 Y240

0003C
0013C
09E3C
09F3C
0A03C
0A13C
13E3C
13F3C

0003E
09F3E
0A03E
13F3E

Column

No.2

No.3

00074
09F74
0A074
13F74

00076
00176
09E76
09F76
0A076
0A176
13E76
13F76

Y1
Y240

Column

Column

13 F 00... Y1

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CPU Interface

1. Function of the RDY (Ready) pin

The built-in RAM is a single-port RAM. To prevent contention between the access from the CPU side and the reading by the liquid-crystal drive side, the RDY pin performs a Wait operation on the CPU.

★ ● **Timing**
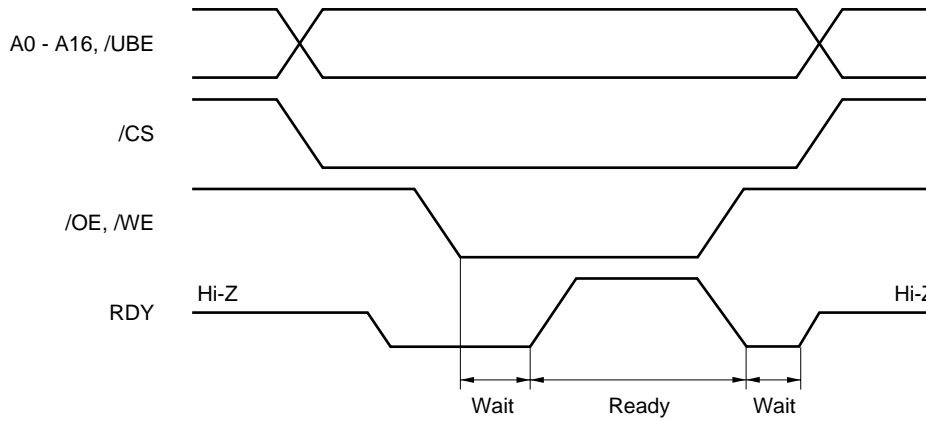
● **Connection of the RDY pin**

The RDY pin uses a three-state buffer. The RDY pin should be connected to an external pull-up resister. If more than one LSI are used, the RDY pins of each LSI are wired together.
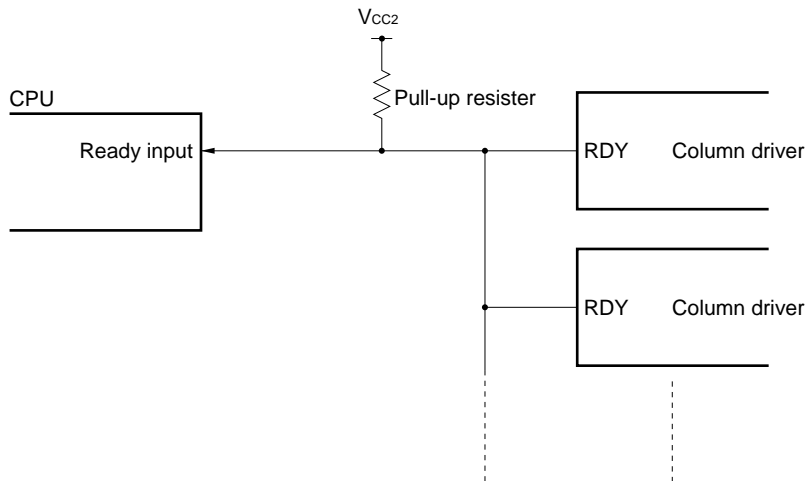
★ **2. Access Timing**

(1) Display data read timing

A16 - A0

/UBE

/CS

/OE

RDY   Hi-Z   Hi-Z

D15 - D0   Hi-Z   Dout   Hi-Z
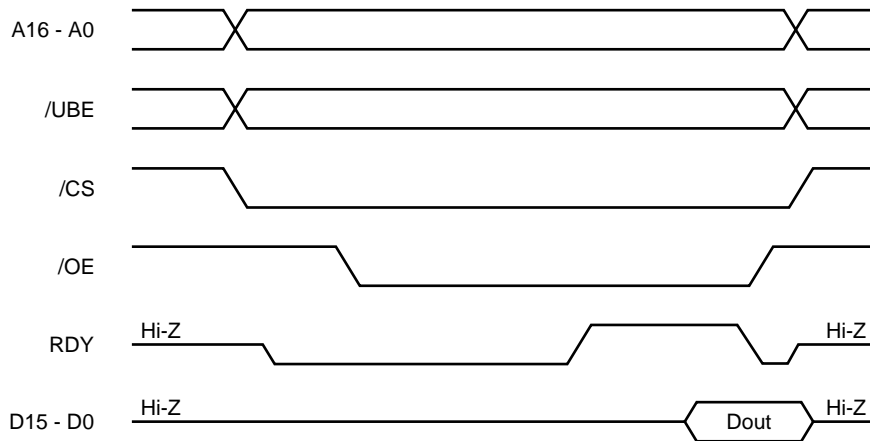
(2) Display data write timing

A16 - A0

/UBE

/CS

/OE

RDY   Hi-Z   Hi-Z

D15 - D0   Din
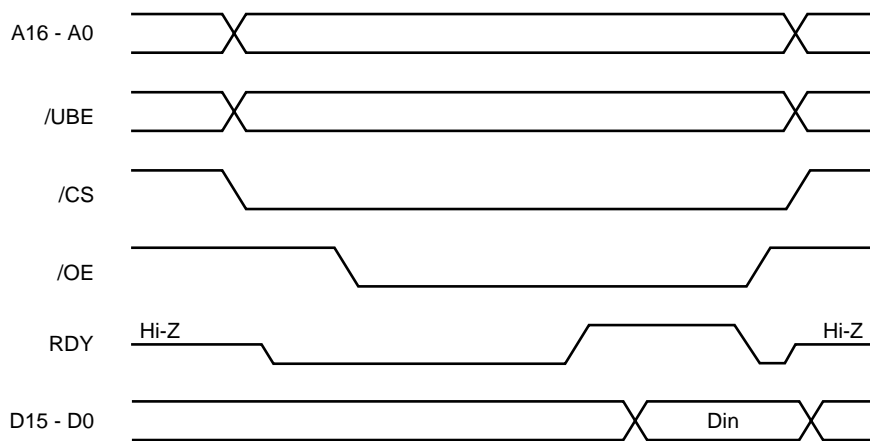
(3) Gray scale pallet data write timing

A16 - A0

/UBE

/CS

/OE

RDY   Hi-Z

D4 - D0   Din

14
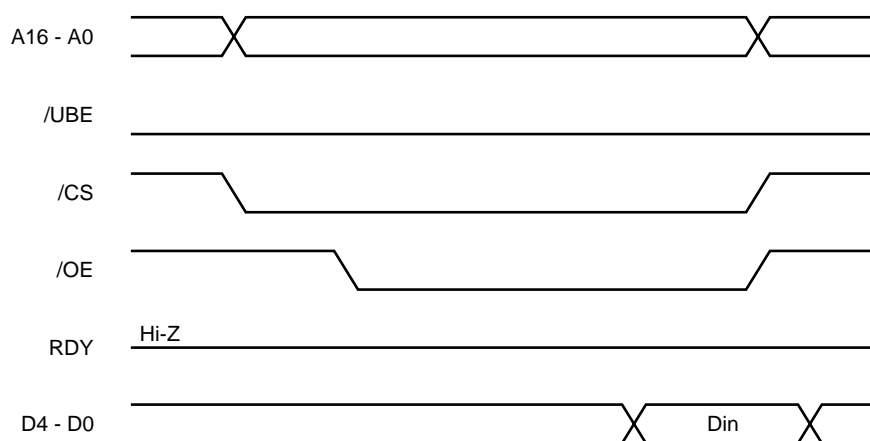
Liquid-Crystal Timing Generation

1. Reset State

If the circuit is placed in the reset state, the internal counter is zero-cleared.

After cancelling the reset, the display OFF function operates during the 4-frame cycle even when the /DOFF pin is at H.
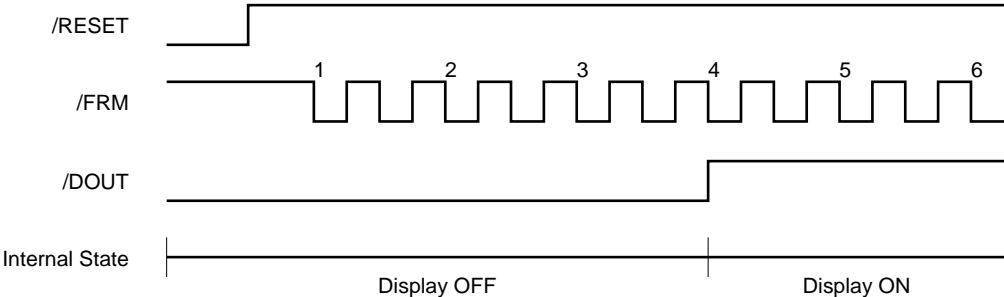
2. Liquid-Crystal Timing Generating Circuit

   If the circuit is set to Master mode when MS = H, the /FRM and STB signals are generated timed with a duty ratio 1/160.

   Generates the driver drive voltage selection signals L1 and L2 for the row driver.

   The /FRM is generated twice per frame. The STB is generated 81 times per half a frame; and 162 times per frame.

● **Generation of /FRM and STB signals**
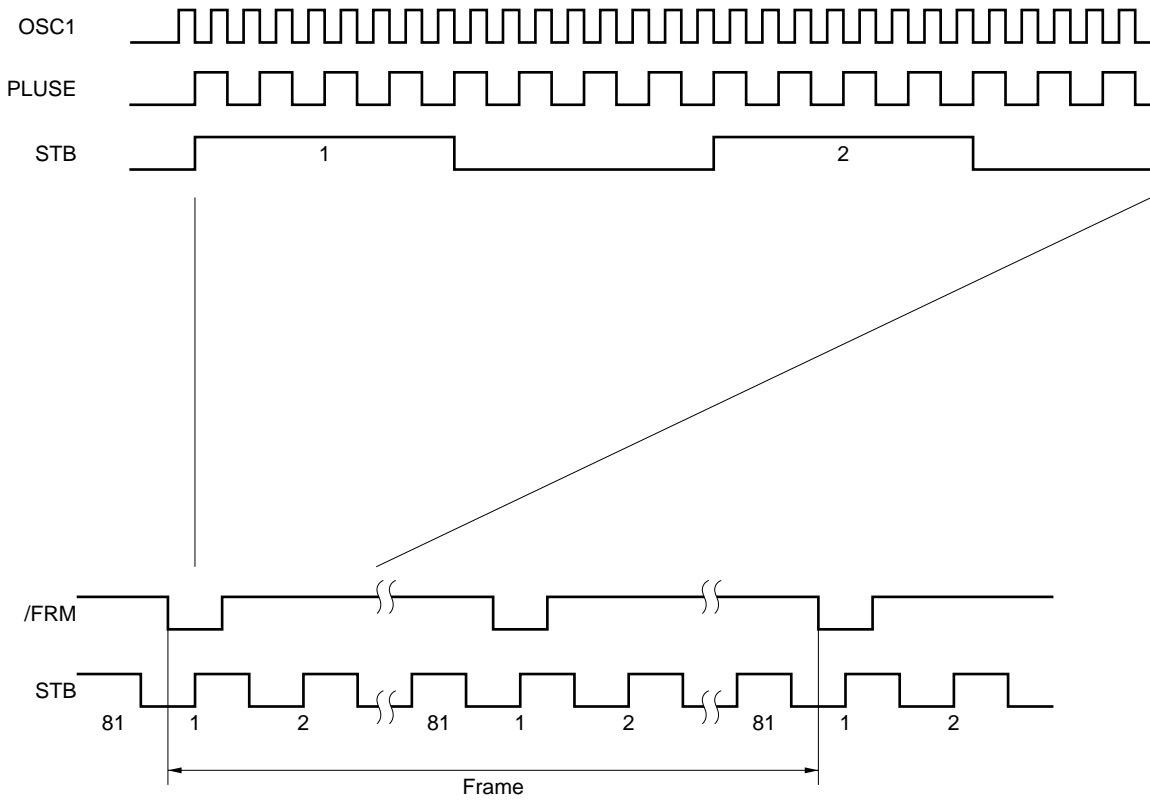
● **Generation of L1 and L2 signals**

STB	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…
L1	1	1	1	1	…	1	1	1	1	…	0	0	0	0	…	0	0	0	0	…
L2	1	0	1	0	…	0	1	0	1	…	0	1	0	1	…	1	0	1	0	…

Self diagnostic function

This is a function to check whether the timing of each column/driver has deviated due to external noise. The slave chip compares the L1 and L2 generated internally with the L1 and L2 of the master chip, and when there is discordance, it sends a total column/driver refresh signal. When a refresh signal is received, the internal reset is activated and timing is initialized. In this case, the /REFRH = L time and the four frame interval display are turned OFF. The L1, L2 discordance will be monitored at the rising edge of the FRM once every 1/2 frame.
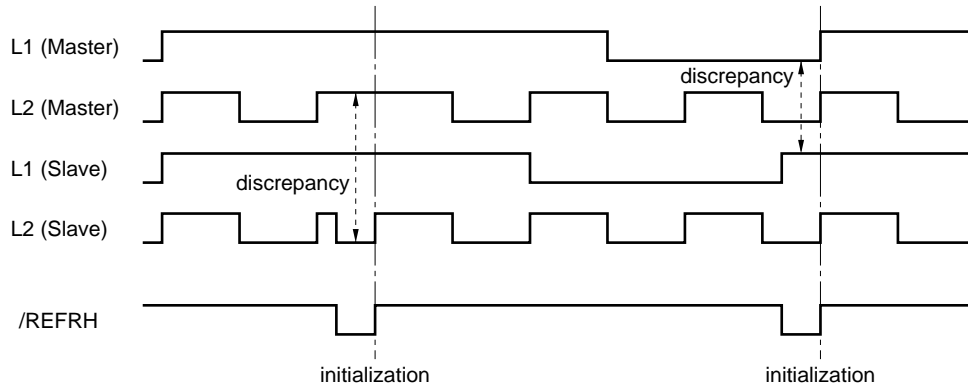
- **Block configuration drawing (slave side)**
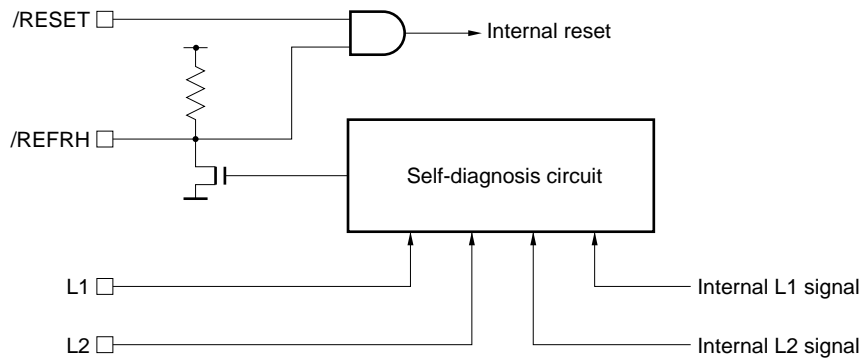
System Configuration Example

An example of configuring a liquid-crystal panel of VGA half-size (480 × 320 dots lengthwise) by using four LSIs and two row drivers.

- Each column driver sets the LSI No. with PL0, PL1 pins.
- The DIR pins of each column driver are all set to low level.
- Only one of the column drivers is set to the master; all the others are set to the slave. Signals are supplied from the master column driver to the slave column driver and to the row driver.
- Connect a resistor for the oscillator to the OSC1 and OSC2 pins of the master. Leave the OSC1 and OSC2 pins of the slave open.
- The signals from the system (D0 through D15, A0 through A16, /CS, /OE, /WE, /UBE, RDY, /RESET, and /DOFF) are connected to all the column drivers in parallel. Connect a pull-up resistor to the RDY signal.
- The TEST pin is used to test the LSI. Open or connect this pin to GND when the system is configured.
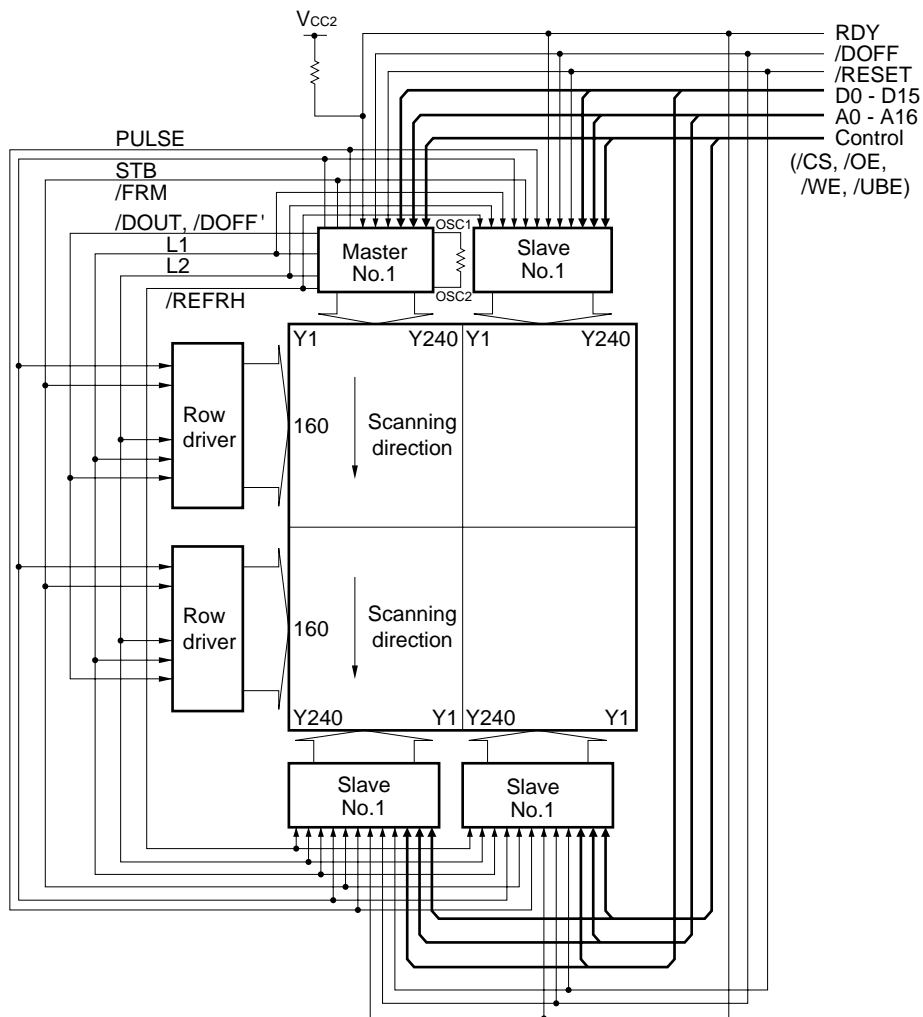
Remark The /DOFF' pin is an input pin of μPD16667.

Chip set power-ON sequence

It is recommended to turn on power in the following sequence:

$V_{CC2} \rightarrow V_{CC1} \rightarrow$ input $\rightarrow V_{DD}, V_{EE} \rightarrow V_1, V_2$

Be sure to turn on LCD driving power supplies V_1 and V_2 last.
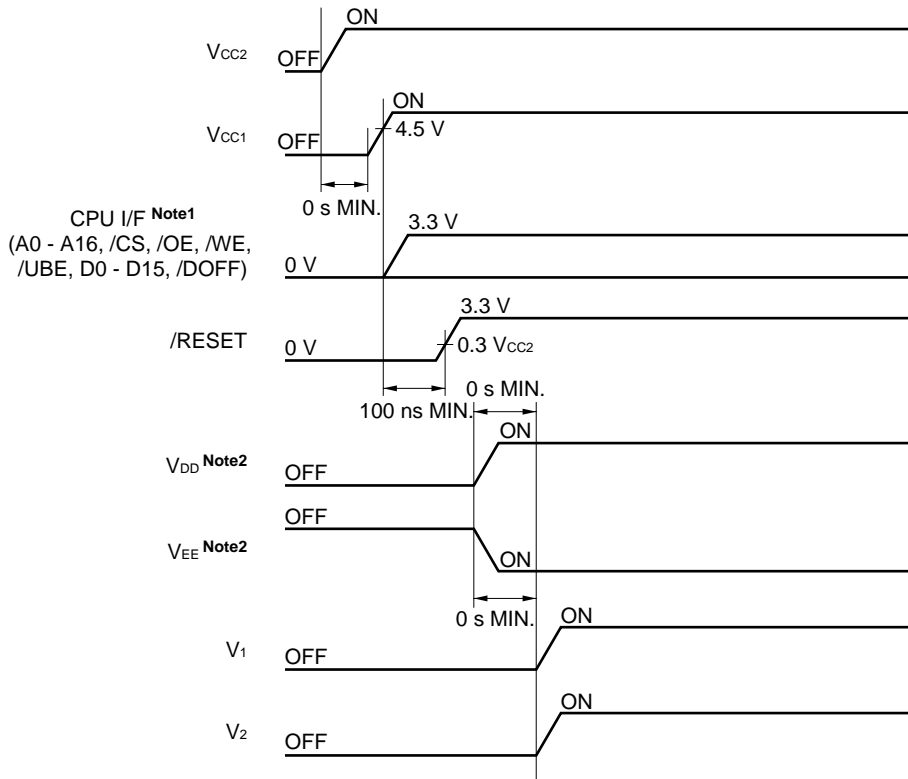
Notes 1. It is possible to input the selected pins (PI0, PL1, DIR, MS, and BMODE) at the same time as V_{CC2}.

  2. It is not necessary to have V_{DD} and V_{EE} ON at the same time. V_{DD} and V_{EE} are the liquid crystal power supply of row driver.

Caution Turn off power to the chip set in the reverse sequence to the turn-on sequence.

Example of layout of internal Schottky barrier diode of module to reinforce power supply protection

(Use a Schottky barrier diode with Vf = 0.5 V MAX.)
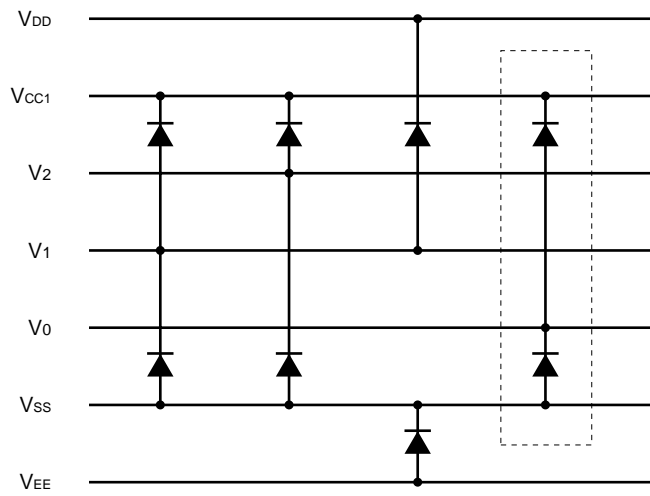
Include the diodes enclosed in the dotted line in the above figure when V_0 is not 0 V (GND).

Note V_{DD} and V_{EE} are the liquid crystal power supply of row driver.

Electrical specifications

1. Absolute Maximum Ratings (T$_A$ = +25 °C)

Parameter	Symbol	Rating	Unit	Notes
Supply voltage (1)	V$_{CC1}$	−0.5 to +6.5	V	1
Supply voltage (2)	V$_{CC2}$	−0.5 to +4.5	V	2
Input/Output voltage (1)	V$_{I/O1}$	−0.5 to V$_{CC1}$ +0.5	V	1
Input/Output voltage (2)	V$_{I/O2}$	−0.5 to V$_{CC2}$ +0.5	V	2
Input/Output voltage (3)	V$_{I/O3}$	−0.5 to V$_{CC1}$ +0.5	V	3, 4
Operating temperature	T$_A$	−20 to +70	°C	
Storage temperature	T$_{stg.}$	−40 to +125	°C	

Notes 1. 5 V power signal (/FRM, STB, /DOUT, L1, L2, PULSE)

2. 3.3 V power signal (MS, DIR, PL0 to PL1, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 to D15, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH)

3. Liquid-crystal drive powers (V$_0$, V$_1$, V$_2$, Y1 to Y240)

4. V$_0$ < V$_1$ < V$_2$

2. Recommended Operating Range (T$_A$ = 20 to +70 C, V$_O$ = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notes
Supply voltage (1)	V$_{CC1}$	4.5	5.0	5.5	V	
Supply voltage (2)	V$_{CC2}$	3.0	3.3	3.6	V	
Input voltage (1)	V$_{I1}$	0		V$_{CC1}$	V	1
Input voltage (2)	V$_{I2}$	0		V$_{CC2}$	V	2
V1 Input voltage	V$_1$	V$_0$		V$_2$	V	
V2 Input voltage	V$_2$	V$_1$		V$_{CC1}$	V	
★ External resistance for OSC	R$_{OSC}$	30	62	90	kΩ	

Notes 1. 5 V power signal (/FRM, STB, L1, L2, PULSE)

2. 3.3 V power signal (MS, DIR, PL0 to PL1, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 to D15, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH)

3. DC Characteristics

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V. V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20 to +70 °C)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remark	Notes
High-level input voltage (1)	V_{CC1}	V_{IH1}	0.7 V_{CC1}			V		1
Low-level input voltage (1)		V_{IL1}			0.3V_{CC1}	V		1
High-level input voltage (2)	V_{CC2}	V_{IH2}	0.7 V_{CC2}			V		2
Low-level input voltage (2)		V_{IL2}			0.3V_{CC2}	V		2
High-level output voltage (1)		V_{IH3}	0.8 V_{CC2}			V		4
Low-level output voltage (1)		V_{IL4}			0.2V_{CC2}	V		4
High-level output voltage (2)	V_{CC1}	V_{OH1}	V_{CC1} −0.4			V	I_{OH} = −1 mA	3
Low-level output voltage (2)		V_{OL1}			0.4	V	I_{OL} = 2 mA	3
High-level output voltage (3)		V_{OH2}	V_{CC1} −0.4			V	I_{OH} = −2 mA	1
Low-level output voltage (3)		V_{OL3}			0.4	V	I_{OL} = 4 mA	1, 4
High-level output voltage (3)	V_{CC2}	V_{OH3}	V_{CC2} −0.4			V	I_{OH} = −1 mA	5
Low-level output voltage (3)		V_{OL3}			0.4	V	I_{OL} = 2 mA	5
Input leakage current (1)		I_{I1}			±10	μA	Without TEST pin, V_I = V_{CC2} or GND	
Input leakage current (2)		I_{I2}	10	40	100	μA	Pull down (TEST pin) V_I = V_{CC2}	
Current consumption for display operation (1)	V_{CC1}	I_{MAS1}			100	μA	master	6
Current consumption for display operation (2)	V_{CC2}	I_{MAS2}			250	μA	master	6
Current consumption for display operation (3)	V_{CC1}	I_{SLV1}			60	μA	slave	6
Current consumption for display operation (4)	V_{CC2}	I_{SLV2}			150	μA	slave	6
Liquid crystal drive output on resistance		R_{ON}		1	2	kΩ		7

Notes 1. 5 V signal (/FRM, STB, L1, L2, PULSE)

  2. 3.3 V signal (MS, DIR, PL0 to PL1, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 to D15, /RESET, /DOFF, TEST, BMODE)

  3. /DOUT pin

  4. /REFRH pin

  5. D0 to 15, RDY, and OSC2 pins

  6. With the frame frequency at 70 Hz without output load and CPU no access (D0 to D15, A0 to A16, /UBE = GND, /CS, /OE, /WE = V_{CC2})

  7. This refers to the resistance value between a Y pin and a V pin (either of V_0, V_1 and V_2) when the load current (I_{ON} = 100 μA) is passed to a pin of Y1 to Y240.

4. AC Characteristics 1 Display data transfer timing

(1) Master mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V. V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20 to +70 °C, frame frequency 70 Hz (f_{OSC} = 181.44 kHz), output load: 100 pF)
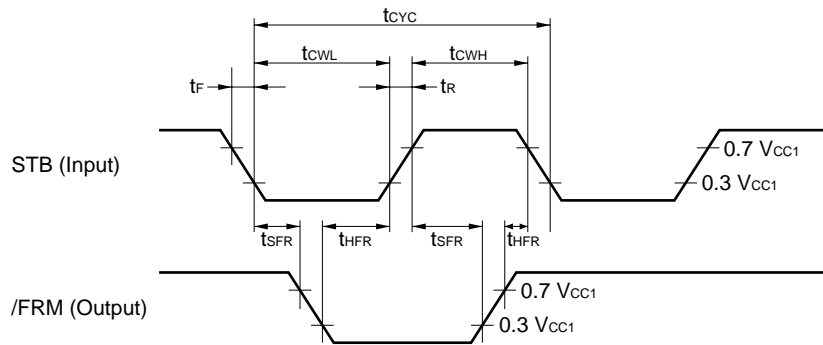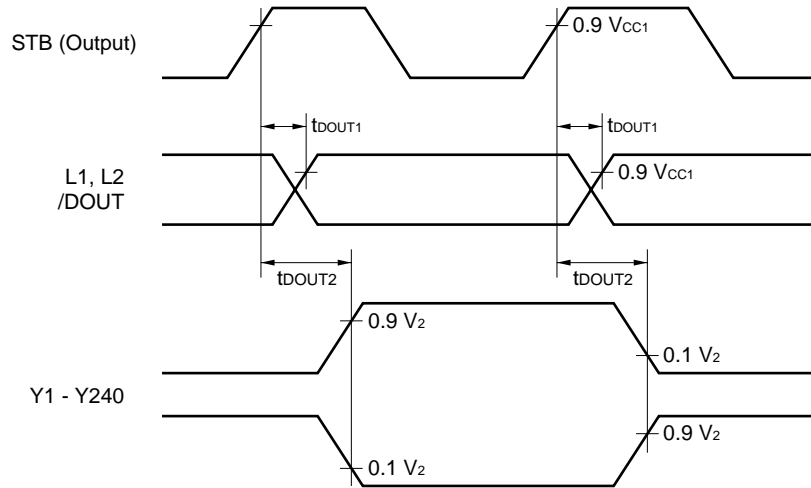
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
STB clock cycle time	t_{CYC}	87	$16/f_{OSC}$		μs	
STB high-level width	t_{CWH}	43	$8/f_{OSC}$		μs	
STB low-level width	t_{CWL}	43	$8/f_{OSC}$		μs	
STB rise time	t_R			100	ns	
STB fall time	t_F			100	ns	
STB -/FRM delay time	t_{PSF}	20			μs	
/FRM -STB delay time	t_{PFS}	20			μs	
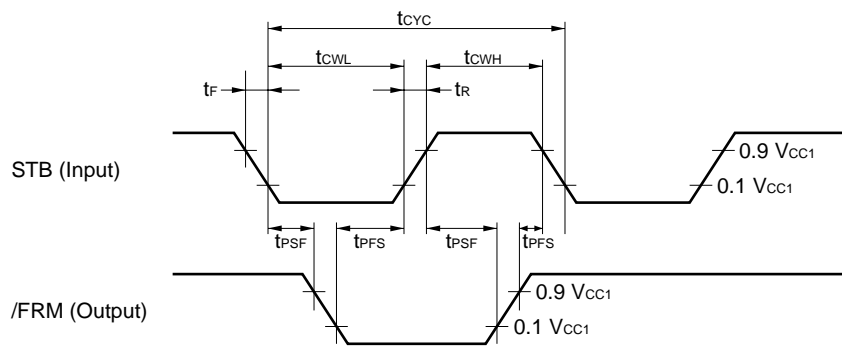
(2) Slave mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V. V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
STB clock cycle time	t_{CYC}	10			μs	
STB High-level width	t_{CWH}	4			μs	
STB low-level width	t_{CWL}	4			μs	
STB rise time	t_R			150	ns	
STB fall time	t_F			150	ns	
/FRM setup time	t_{SFR}	1			μs	
/FRM hold time	t_{HFR}	1			μs	

(3) Items common to the master and slaves

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V. V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Output delay time (L1, L2, /DOUT)	t_{DOUT1}		50	100	ns	Without output load
Output delay time (Y1 to Y240)	t_{DOUT2}		90	150	ns	Without output load

5. AC Characteristics 2 Graphic Access Timing

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V. V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20 to +70 °C, t_r = t_f = 5 ns)

	Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark	Notes
	/OE, /WE recovery time	t_{RY}	30			ns		
	Address setup time	t_{AS}	10			ns		
	Address hold time	t_{AH}	20			ns		
	RDY output delay time	t_{RYR}			30	ns	CL = 15 pF	
★	RDY float time	t_{RYZ}			30	ns		3
★	Wait state time	t_{RYW}			35	ns		1
	Ready state time (without contention)	t_{RYF1}		60	100	ns		1
	Ready state time (with contention)	t_{RYF2}		650	1,200	ns		1
	Data access time (Read cycle)	t_{ACS}			100	ns		2
★	Data float time (Read cycle)	t_{HZ}			40	ns		3
	/CS - /OE time (Read cycle)	t_{CSOE}	10			ns		
	/OE - /CS time (Read cycle)	t_{OECS}	20			ns		
	Write pulse width 1 (Write cycle 1)	t_{WP1}	50			ns		1
	Write pulse width 2 (Write cycle 2)	t_{WP2}	50			ns		1
	Data setup time (Write cycle 1, 2)	t_{DW}	20			ns		
	Data hold time (Write cycle 1, 2)	t_{DH}	20			ns		
	/CS - /WE time (Write cycle 1, 2)	t_{CSWE}	10			ns		
	/WE - /CS time (Write cycle 1, 2)	t_{WECS}	20			ns		
	Reset pulse width	t_{WRES}	100			ns		
	RDY - /OE time	t_{RDOE}			−	−		4
	RDY - /WE time	t_{RDWE}			−	−		4

Notes 1. Load circuit
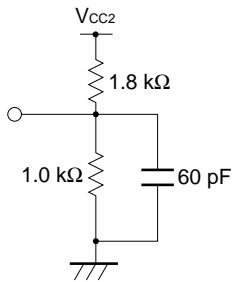
2. Load circuit
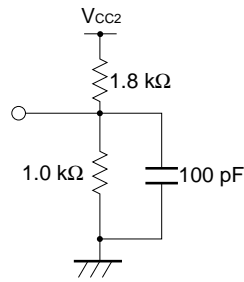
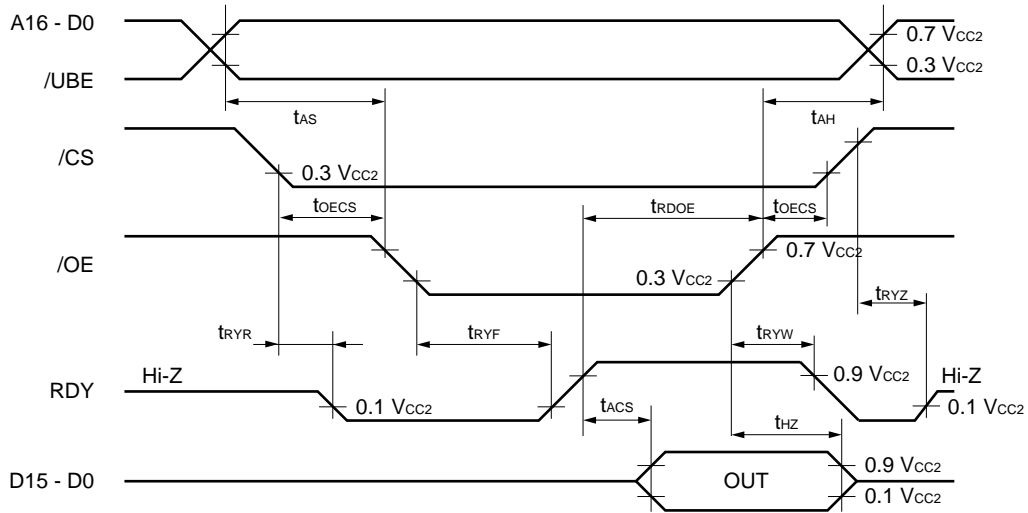★ **3.** Load circuit
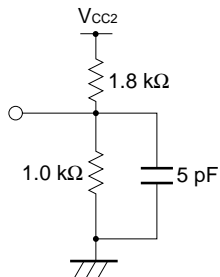
4. The display may be affected if the time from the rising of RDY to /OE or /WE is too long. It is recommended that t_{RDOE} and t_{RDWE} be 1,000 ns MAX.
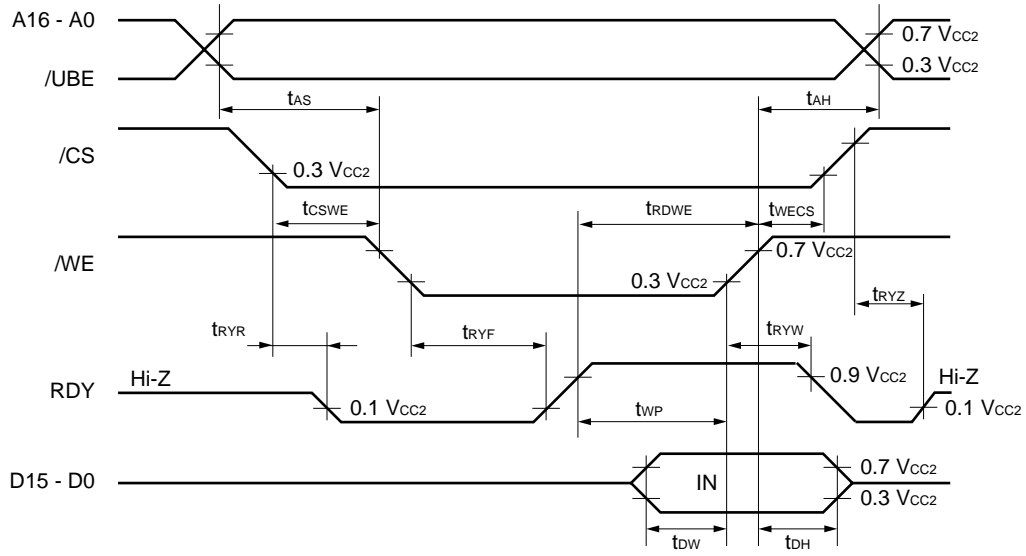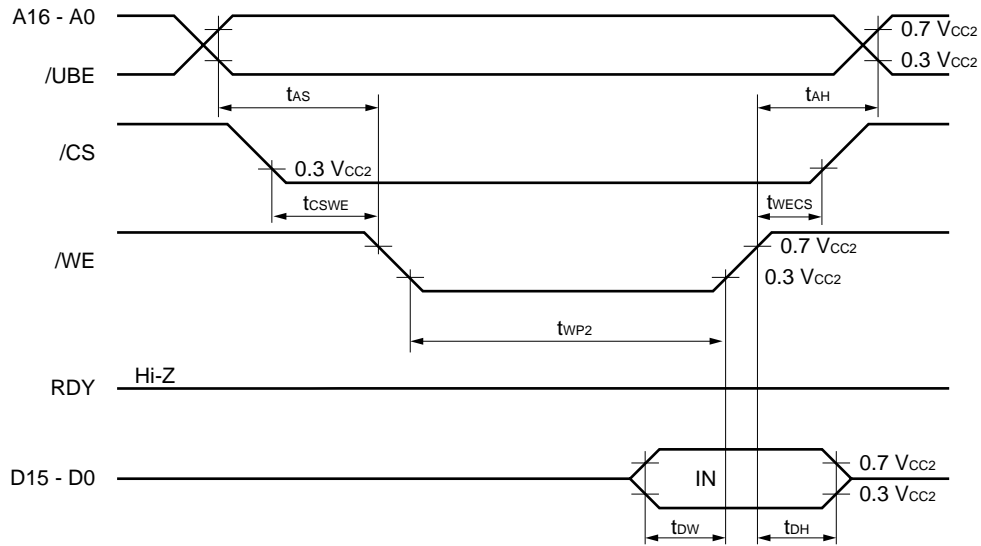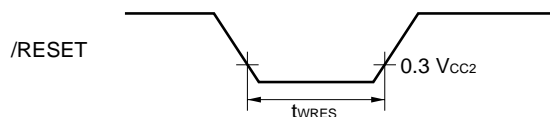
/OE, /WE recovery time
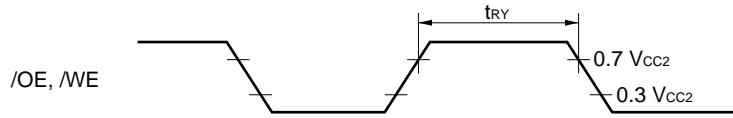
★   **Read cycle**

★ **Write cycle 1 (Display data write)**

Write cycle 2 (Gray scale pallet data write)

Reset pulse width

/RESET ⎯⎯⎯⎯⎯⎯ 0.3 V$_{CC2}$

t_{WRES}

6. AC Characteristics 3 CR Oscillator

(V$_{CC2}$ = 3.0 to 3.6 V, TA = −20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Oscillation frequency	f$_{OSC}$	160	190	220	kHz	External resistance: 62 kΩ
Frame frequency	–	61.7	73.3	84.9	Hz	External resistance: 62 kΩ

Relation between oscillation frequency, frame frequency, and STB frequency

The relation between the oscillation frequency, frame frequency, and STB frequency is as follows:

$$\text{Frame frequency} = \frac{1}{162 \times 2 \times 8} \times \text{Oscillation frequency}$$

$$\text{STB frequency} = \frac{1}{2 \times 8} \times \text{Oscillation frequency}$$

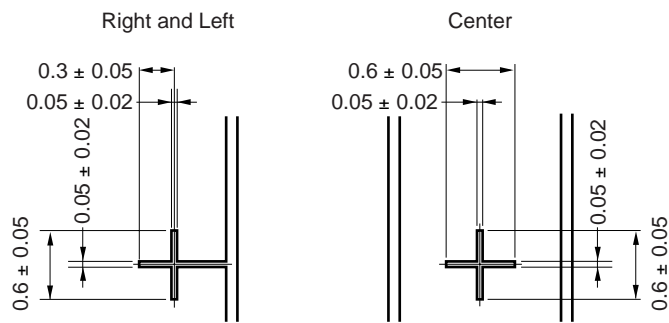★   **Package drawings**

Standard TCP package (μPD16662N - 051)(1/3)
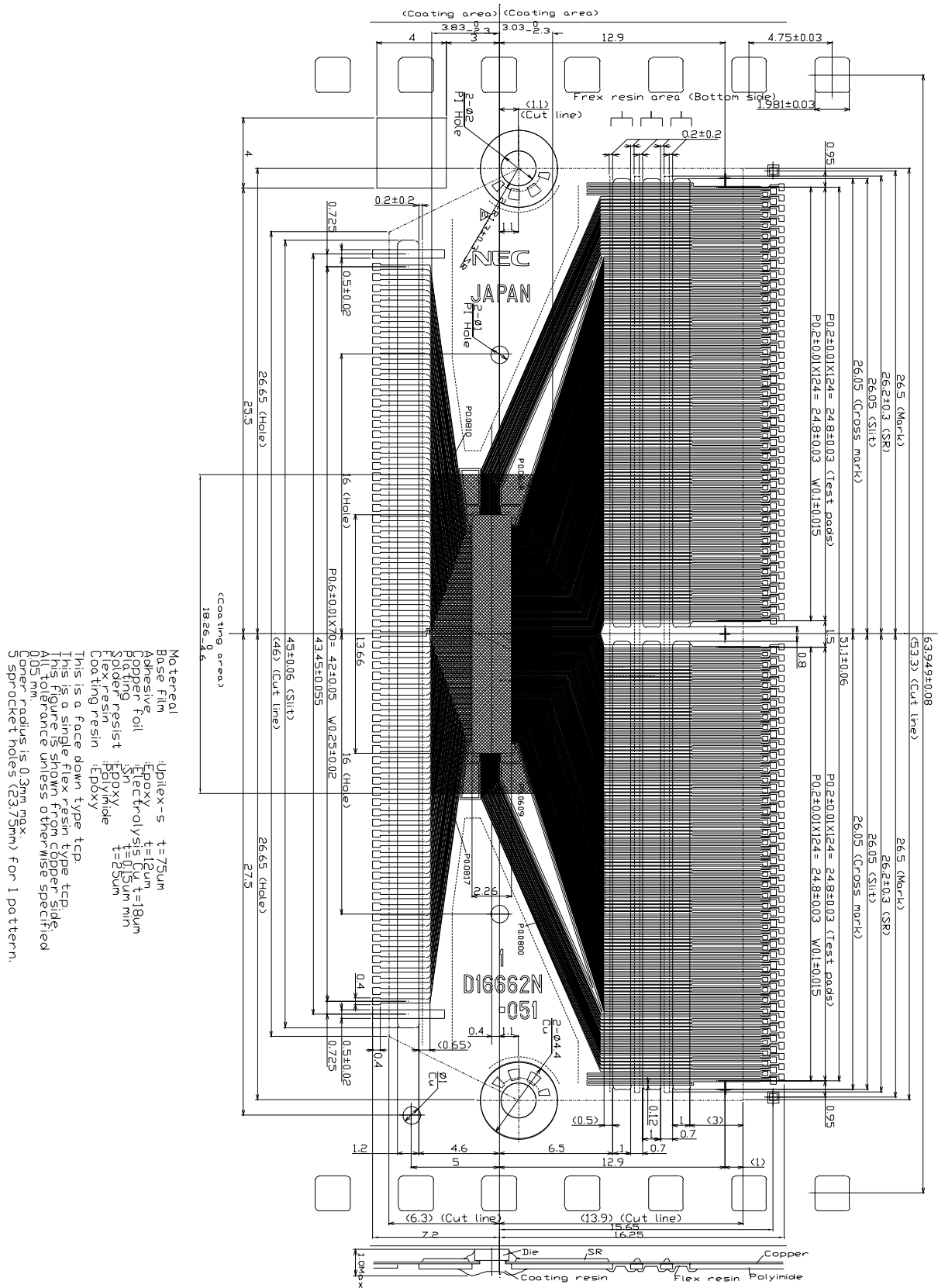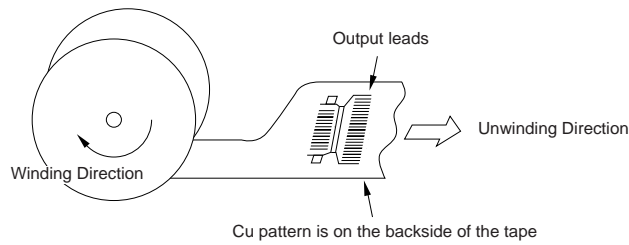
Standard TCP package (μPD16662N - 051)(2/3)

Detail of output side test pad and alignment mark
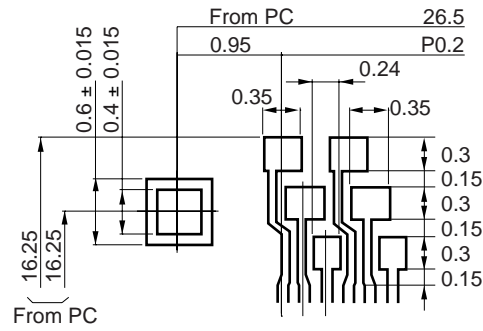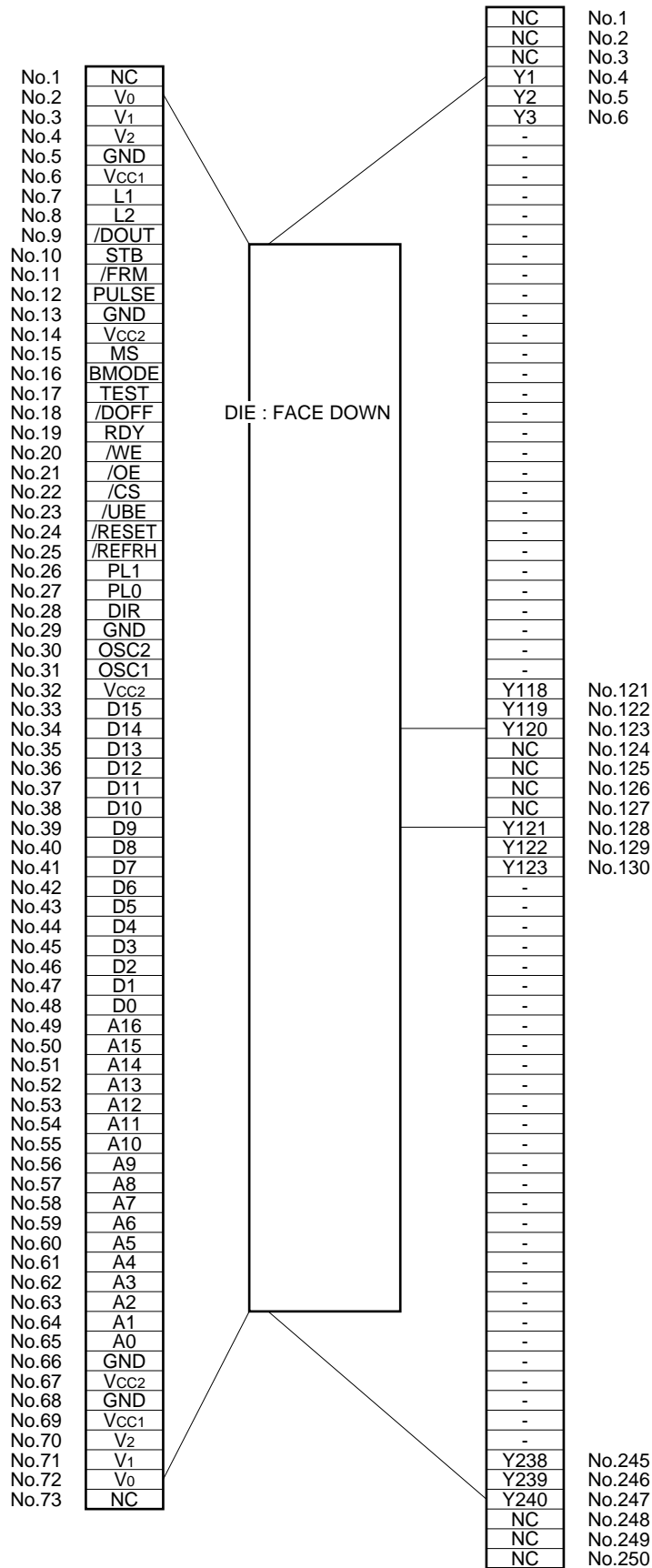

Detail of cross mark

TCP tape winding direction

Output leads

Unwinding Direction

Winding Direction

Cu pattern is on the backside of the tape

Standard TCP package (μPD16662N - 051) (3/3)

Pin connection

No.	Left Pin			Right Pin	No.
				NC	No.1
				NC	No.2
				NC	No.3
No.1	NC			Y1	No.4
No.2	V0			Y2	No.5
No.3	V1			Y3	No.6
No.4	V2			-	
No.5	GND			-	
No.6	VCC1			-	
No.7	L1			-	
No.8	L2			-	
No.9	/DOUT			-	
No.10	STB			-	
No.11	/FRM			-	
No.12	PULSE			-	
No.13	GND			-	
No.14	VCC2	DIE : FACE DOWN		-	
No.15	MS			-	
No.16	BMODE			-	
No.17	TEST			-	
No.18	/DOFF			-	
No.19	RDY			-	
No.20	/WE			-	
No.21	/OE			-	
No.22	/CS			-	
No.23	/UBE			-	
No.24	/RESET			-	
No.25	/REFRH			-	
No.26	PL1			-	
No.27	PL0			-	
No.28	DIR			-	
No.29	GND			-	
No.30	OSC2			-	
No.31	OSC1			-	
No.32	VCC2			Y118	No.121
No.33	D15			Y119	No.122
No.34	D14			Y120	No.123
No.35	D13			NC	No.124
No.36	D12			NC	No.125
No.37	D11			NC	No.126
No.38	D10			NC	No.127
No.39	D9			Y121	No.128
No.40	D8			Y122	No.129
No.41	D7			Y123	No.130
No.42	D6			-	
No.43	D5			-	
No.44	D4			-	
No.45	D3			-	
No.46	D2			-	
No.47	D1			-	
No.48	D0			-	
No.49	A16			-	
No.50	A15			-	
No.51	A14			-	
No.52	A13			-	
No.53	A12			-	
No.54	A11			-	
No.55	A10			-	
No.56	A9			-	
No.57	A8			-	
No.58	A7			-	
No.59	A6			-	
No.60	A5			-	
No.61	A4			-	
No.62	A3			-	
No.63	A2			-	
No.64	A1			-	
No.65	A0			-	
No.66	GND			-	
No.67	VCC2			-	
No.68	GND			-	
No.69	VCC1			-	
No.70	V2			-	
No.71	V1			Y238	No.245
No.72	V0			Y239	No.246
No.73	NC			Y240	No.247
				NC	No.248
				NC	No.249
				NC	No.250

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[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.