NEC

MOS INTEGRATED CIRCUIT

μPD30500, 30500A, 30500B

VR5000™, VR5000A™, VR5000B™
64-BIT MICROPROCESSOR

DESCRIPTION

The μPD30500 (VR5000), μPD30500A (VR5000A), and μPD30500B[Note] (VR5000B) are a high-performance, 64-bit RISC (Reduced Instruction Set Computer) type microprocessors employing the RISC architecture developed by MIPS™ Technologies Inc.

The instructions of the VR5000, VR5000A, and VR5000B are compatible with those of the VR3000™ Series and VR4000™ Series and higher, and completely compatible with those of the VR10000™. Therefore, present applications can be used as they are.

Note Under development

Detailed functions are described in the following manual. Be sure to read the manual when designing your system.

- **VR5000, VR5000A, VR5000B User's Manual (U11761E)**

FEATURES

- Employs 64-bit MIPS-based RISC architecture
- High-speed processing
  - 2-way super scalar 5-stage pipeline
  - 5.5 SPECint95, 5.5 SPECfp95, 278 MIPS (μPD30500)
    6.6 SPECint95, 6.6 SPECfp95, 353 MIPS (μPD30500A)
    8 SPECint95, 8 SPECfp95, 423 MIPS (μPD30500B)
- High-speed translation buffer mechanism (TLB) (48 entries)
- Address space Physical: 36 bits, Virtual: 40 bits
- Floating-point unit (FPU)
  - Sum-of-products operation instruction supported
- Primary cache memory (instruction/data: 32 Kbytes each)
- Secondary cache controller
- Maximum operating frequency Internal: 200 MHz (μPD30500), 250 MHz (μPD30500A), 300 MHz (μPD30500B)
  External: 100 MHz
  - Selectable external/internal multiple rate from twice to eight times
- Instruction set compatible with VR3000 and VR4000 Series and higher (conforms to MIPS I, II, III, and IV)
- Supply voltage: 3.3 V ±5% (μPD30500)
  Core: 2.5 V ±5%, I/O: 3.3 V ±5% (μPD30500A)
  Core: 1.8 V ±0.1 V, I/O: 3.3 V ±5% (μPD30500B)

Unless otherwise specified, the VR5000 (μPD30500) is treated as the representative model throughout this document.

Document No. U12031EJ4V0DS00 (4th edition)
Date Published May 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

- High-performance embedded systems
- Multimedia systems
- Entry-class computers
- Image processing systems

★ ORDERING INFORMATION

Part number	Package	Maximum operating frequency (MHz)
μPD30500RJ-150	223-pin ceramic PGA (48 × 48)	150
μPD30500RJ-180	223-pin ceramic PGA (48 × 48)	180
μPD30500RJ-200	223-pin ceramic PGA (48 × 48)	200
μPD30500S2-150	272-pin plastic BGA (C/D advanced type) (29 × 29)	150
μPD30500S2-180	272-pin plastic BGA (C/D advanced type) (29 × 29)	180
μPD30500S2-200	272-pin plastic BGA (C/D advanced type) (29 × 29)	200
μPD30500AS2-250	272-pin plastic BGA (C/D advanced type) (29 × 29)	250
μPD30500BS2-300**Note**	272-pin plastic BGA (C/D advanced type) (29 × 29)	300

Note Under development

MAIN DIFFERENCES BETWEEN VR5000, VR5000A, AND VR5000B

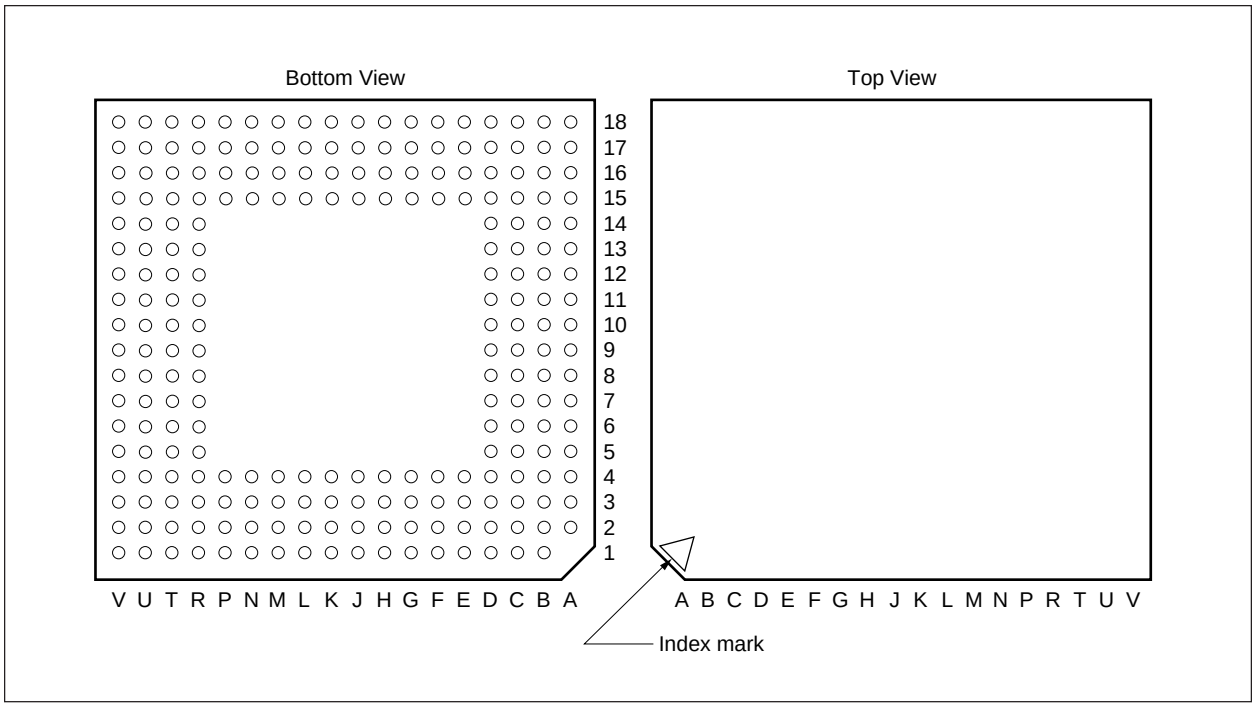
Parameter	VR5000	VR5000A	VR5000B**Note 1**
★ Maximum internal operating frequency	150/180/200 MHz	250 MHz	300 MHz
Internal multiplication ratio for clock interface input	2, 3, 4, 5, 6, 7, 8	2, 2.5**Note 2**, 3, 4, 5, 6, 7, 8	
Supply voltage	3.3 V ±5%	Core: 2.5 V ±5% I/O: 3.3 V ±5%	Core: 1.8 V ±0.1 V I/O: 3.3 V ±5%
Package	• 223-pin ceramic PGA • 272-pin plastic BGA (C/D advanced type)	• 272-pin plastic BGA (C/D advanced type)	

Notes 1. Under development

2. Selectable only when SysClock = 100 MHz

PIN CONFIGURATION

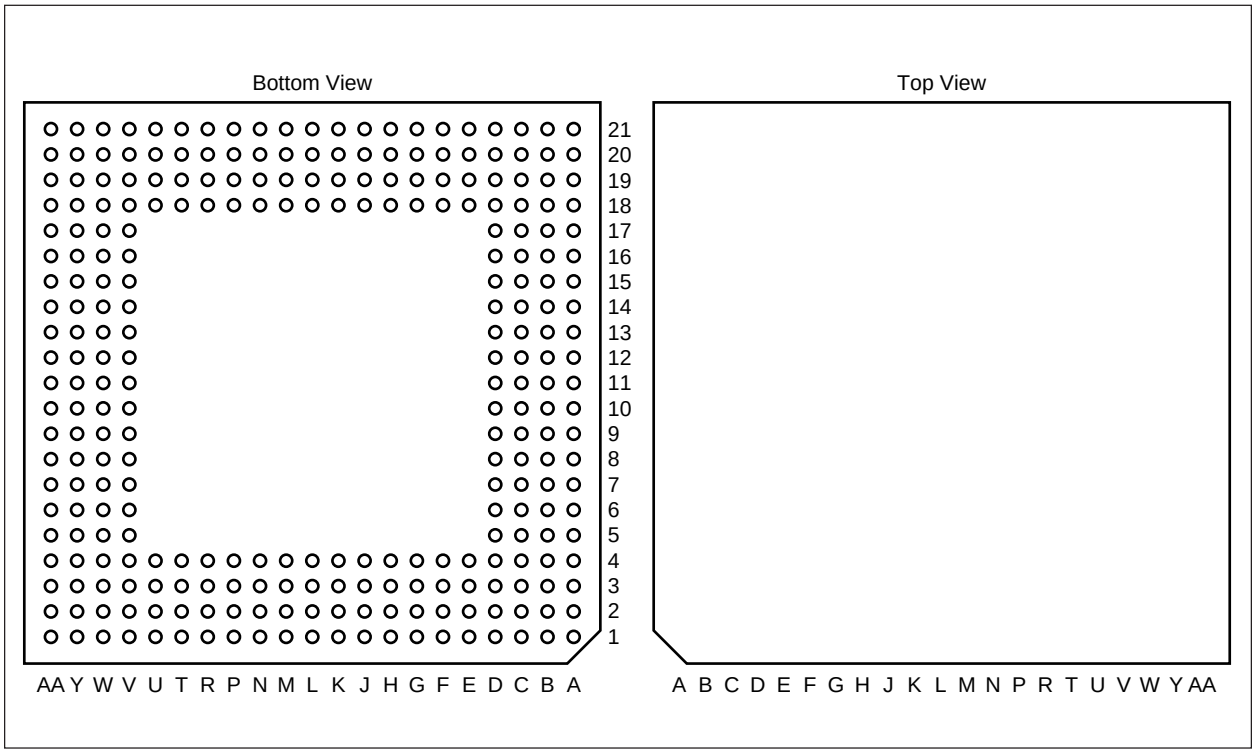
- **223-pin ceramic PGA (48 × 48)**
  μPD30500RJ-150
  μPD30500RJ-180
  μPD30500RJ-200



No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
A2	V_{DD}	C5	SysADC6	E18	V_{DD}	K17	GNDP	R6	SysAD51	U9	SysAD63
A3	GND	C6	SysAD16	F1	V_{DD}	K18	GND	R7	SysAD55	U10	SysAD13
A4	V_{DD}	C7	SysAD50	F2	Reserved	L1	GND	R8	SysAD27	U11	SysAD11
A5	GND	C8	SysAD22	F3	ScValid	L2	SysCmd8	R9	SysAD31	U12	SysAD9
A6	GND	C9	SysAD24	F4	$\overline{Int1}$	L3	SysCmd7	R10	SysAD43	U13	SysAD37
A7	V_{DD}	C10	SysAD28	F15	$\overline{ScDCE0}$	L4	SysCmd5	R11	SysAD39	U14	SysAD3
A8	GND	C11	SysAD62	F16	$\overline{ScCWE0}$	L15	ScLine12	R12	SysAD35	U15	ScWord0
A9	V_{DD}	C12	SysAD44	F17	$\overline{ScTDE}$	L16	ScLine14	R13	SysAD1	U16	V_{DD}
A10	GND	C13	SysAD10	F18	GND	L17	ScLine15	R14	ScWord1	U17	GND
A11	V_{DD}	C14	SysAD38	G1	GND	L18	V_{DD}	R15	ScLine0	U18	GND
A12	GND	C15	SysAD4	G2	Reserved	M1	V_{DD}	R16	ScLine3	V1	GND
A13	V_{DD}	C16	SysAD34	G3	Reserved	M2	SysCmd6	R17	ScLine6	V2	GND
A14	GND	C17	SysAD2	G4	Reserved	M3	SysCmd4	R18	GND	V3	V_{DD}
A15	GND	C18	GND	G15	$\overline{ScCLR}$	M4	SysCmd1	T1	GND	V4	GND
A16	V_{DD}	D1	GND	G16	$\overline{ScTCE}$	M15	ScLine8	T2	SysAD15	V5	GND
A17	GND	D2	$\overline{Int3}$	G17	ModeIn	M16	ScLine10	T3	SysAD47	V6	V_{DD}
A18	GND	D3	$\overline{Int5}$	G18	V_{DD}	M17	ScLine13	T4	SysAD17	V7	GND
B1	GND	D4	$\overline{Release}$	H1	V_{DD}	M18	GND	T5	SysAD19	V8	V_{DD}
B2	GND	D5	V_{DD}	H2	Reserved	N1	GND	T6	SysAD23	V9	GND
B3	V_{DD}	D6	SysADC2	H3	Reserved	N2	SysCmd3	T7	SysAD57	V10	V_{DD}
B4	SysADC4	D7	SysAD48	H4	Reserved	N3	SysCmd2	T8	SysAD29	V11	GND
B5	SysADC0	D8	SysAD52	H15	V_{DD}Ok	N4	SysADC7	T9	V_{DD}	V12	V_{DD}
B6	SysAD18	D9	SysAD56	H16	ModeClock	N15	ScLine5	T10	SysAD45	V13	GND
B7	SysAD20	D10	SysAD60	H17	SysClock	N16	ScLine7	T11	SysAD41	V14	V_{DD}
B8	SysAD54	D11	SysAD14	H18	GND	N17	ScLine11	T12	SysAD7	V15	GND
B9	SysAD26	D12	SysAD42	J1	GND	N18	V_{DD}	T13	SysAD5	V16	GND
B10	SysAD58	D13	SysAD8	J2	$\overline{WrRdy}$	P1	V_{DD}	T14	SysAD33	V17	V_{DD}
B11	SysAD30	D14	SysAD36	J3	$\overline{ValidIn}$	P2	SysCmd0	T15	$\overline{Reset}$	V18	GND
B12	SysAD46	D15	$\overline{ColdReset}$	J4	$\overline{ExtRqst}$	P3	SysCmdP	T16	ScLine1		
B13	SysAD12	D16	SysAD0	J15	Reserved	P4	SysADC1	T17	V_{DD}		
B14	SysAD40	D17	$\overline{ScTOE}$	J16	Reserved	P15	ScLine2	T18	V_{DD}		
B15	SysAD6	D18	V_{DD}	J17	Reserved	P16	ScLine4	U1	V_{DD}		
B16	GND	E1	GND	J18	V_{DD}	P17	ScLine9	U2	V_{DD}		
B17	V_{DD}	E2	$\overline{Int0}$	K1	V_{DD}	P18	GND	U3	GND		
B18	V_{DD}	E3	$\overline{Int2}$	K2	ScMatch	R1	V_{DD}	U4	SysAD21		
C1	V_{DD}	E4	$\overline{Int4}$	K3	$\overline{RdRdy}$	R2	SysADC5	U5	SysAD53		
C2	V_{DD}	E15	SysAD32	K4	$\overline{ScDOE}$	R3	SysADC3	U6	SysAD25		
C3	$\overline{ValidOut}$	E16	$\overline{ScDCE1}$	K15	Reserved	R4	BigEndian	U7	SysAD59		
C4	$\overline{NMI}$	E17	$\overline{ScCWE1}$	K16	V_{DD}P	R5	SysAD49	U8	SysAD61		

- **272-pin plastic BGA (C/D advanced type) (29 × 29)**

  μPD30500S2-150
  μPD30500S2-180
  μPD30500S2-200
★ μPD30500AS2-250
  μPD30500BS2-300[Note]



Note Under development

(1) μPD30500

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
A1	GND	C5	$\overline{\text{ScDCE1}}$	F1	SysAD8	L20	SysAD63	U18	V_{DD}	Y1	V_{DD}
A2	V_{DD}	C6	$\overline{\text{ScDCE0}}$	F2	SysAD38	L21	GND	U19	SysAD17	Y2	V_{DD}
A3	GND	C7	$\overline{\text{ScCWE0}}$	F3	SysAD6	M1	SysAD26	U20	SysAD49	Y3	V_{DD}
A4	SysAD32	C8	$\overline{\text{ScTCE}}$	F4	GND	M2	SysAD56	U21	GND	Y4	$\overline{\text{Release}}$
A5	GND	C9	ModeIn	F18	GND	M3	SysAD24	V1	V_{DD}	Y5	$\overline{\text{Int3}}$
A6	$\overline{\text{ScCWE1}}$	C10	Reserved	F19	SysAD1	M4	V_{DD}	V2	V_{DD}	Y6	$\overline{\text{Int2}}$
A7	GND	C11	GNDP	F20	SysAD33	M18	V_{DD}	V3	V_{DD}	Y7	ScValid
A8	V_{DD}Ok	C12	Reserved	F21	SysAD3	M19	SysAD29	V4	GND	Y8	Reserved
A9	GND	C13	ScLine13	G1	GND	M20	SysAD61	V5	$\overline{\text{NMI}}$	Y9	Reserved
A10	SysClock	C14	ScLine11	G2	SysAD10	M21	SysAD31	V6	GND	Y10	Reserved
A11	GND	C15	ScLine8	G3	SysAD40	N1	GND	V7	V_{DD}	Y11	$\overline{\text{ExtRqst}}$
A12	ScLine15	C16	ScLine5	G4	V_{DD}	N2	SysAD54	V8	V_{DD}	Y12	$\overline{\text{RdRdy}}$
A13	GND	C17	ScLine4	G18	V_{DD}	N3	SysAD22	V9	GND	Y13	SysCmd8
A14	ScLine12	C18	ScLine0	G19	SysAD35	N4	GND	V10	V_{DD}	Y14	SysCmd5
A15	GND	C19	$\overline{\text{Reset}}$	G20	SysAD5	N18	GND	V11	V_{DD}	Y15	SysCmd3
A16	ScLine7	C20	V_{DD}	G21	GND	N19	SysAD27	V12	V_{DD}	Y16	SysCmd0
A17	GND	C21	GND	H1	SysAD42	N20	SysAD59	V13	GND	Y17	SysCmdP
A18	ScLine2	D1	V_{DD}	H2	SysAD44	N21	GND	V14	V_{DD}	Y18	SysADC1
A19	GND	D2	V_{DD}	H3	SysAD12	P1	SysAD50	V15	V_{DD}	Y19	SysAD15
A20	V_{DD}	D3	V_{DD}	H4	V_{DD}	P2	SysAD52	V16	GND	Y20	V_{DD}
A21	GND	D4	GND	H18	V_{DD}	P3	SysAD20	V17	V_{DD}	Y21	V_{DD}
B1	V_{DD}	D5	V_{DD}	H19	SysAD7	P4	V_{DD}	V18	GND	AA1	GND
B2	V_{DD}	D6	GND	H20	SysAD39	P18	V_{DD}	V19	V_{DD}	AA2	V_{DD}
B3	V_{DD}	D7	V_{DD}	H21	SysAD37	P19	SysAD25	V20	V_{DD}	AA3	GND
B4	SysAD2	D8	V_{DD}	J1	GND	P20	SysAD57	V21	V_{DD}	AA4	$\overline{\text{ValidOut}}$
B5	SysAD0	D9	GND	J2	SysAD46	P21	SysAD55	W1	GND	AA5	GND
B6	$\overline{\text{ScTOE}}$	D10	V_{DD}	J3	SysAD14	R1	GND	W2	V_{DD}	AA6	$\overline{\text{Int0}}$
B7	$\overline{\text{ScCLR}}$	D11	V_{DD}P	J4	GND	R2	SysAD18	W3	V_{DD}	AA7	GND
B8	$\overline{\text{ScTDE}}$	D12	V_{DD}	J18	GND	R3	SysAD48	W4	V_{DD}	AA8	Reserved
B9	ModeClock	D13	GND	J19	SysAD9	R4	V_{DD}	W5	$\overline{\text{Int5}}$	AA9	GND
B10	Reserved	D14	V_{DD}	J20	SysAD41	R18	V_{DD}	W6	$\overline{\text{Int4}}$	AA10	$\overline{\text{WrRdy}}$
B11	Reserved	D15	V_{DD}	J21	GND	R19	SysAD53	W7	$\overline{\text{Int1}}$	AA11	GND
B12	NC	D16	GND	K1	SysAD60	R20	SysAD23	W8	Reserved	AA12	ScMatch
B13	ScLine14	D17	V_{DD}	K2	SysAD30	R21	GND	W9	Reserved	AA13	GND
B14	ScLine10	D18	GND	K3	SysAD62	T1	SysAD16	W10	Reserved	AA14	SysCmd6
B15	ScLine9	D19	V_{DD}	K4	V_{DD}	T2	SysADC0	W11	$\overline{\text{ValidIn}}$	AA15	GND
B16	ScLine6	D20	V_{DD}	K18	V_{DD}	T3	SysADC2	W12	$\overline{\text{ScDOE}}$	AA16	SysCmd2
B17	ScLine3	D21	V_{DD}	K19	SysAD11	T4	GND	W13	SysCmd7	AA17	GND
B18	ScLine1	E1	GND	K20	SysAD43	T18	GND	W14	SysCmd4	AA18	SysADC3
B19	V_{DD}	E2	SysAD36	K21	SysAD13	T19	SysAD19	W15	SysCmd1	AA19	GND
B20	V_{DD}	E3	SysAD4	L1	GND	T20	SysAD51	W16	SysADC7	AA20	V_{DD}
B21	V_{DD}	E4	V_{DD}	L2	SysAD58	T21	SysAD21	W17	SysADC5	AA21	GND
C1	GND	E18	V_{DD}	L3	SysAD28	U1	GND	W18	SysAD47		
C2	V_{DD}	E19	ScWord1	L4	V_{DD}	U2	SysADC4	W19	BigEndian		
C3	$\overline{\text{ColdReset}}$	E20	ScWord0	L18	V_{DD}	U3	SysADC6	W20	V_{DD}		
C4	SysAD34	E21	GND	L19	SysAD45	U4	V_{DD}	W21	GND		

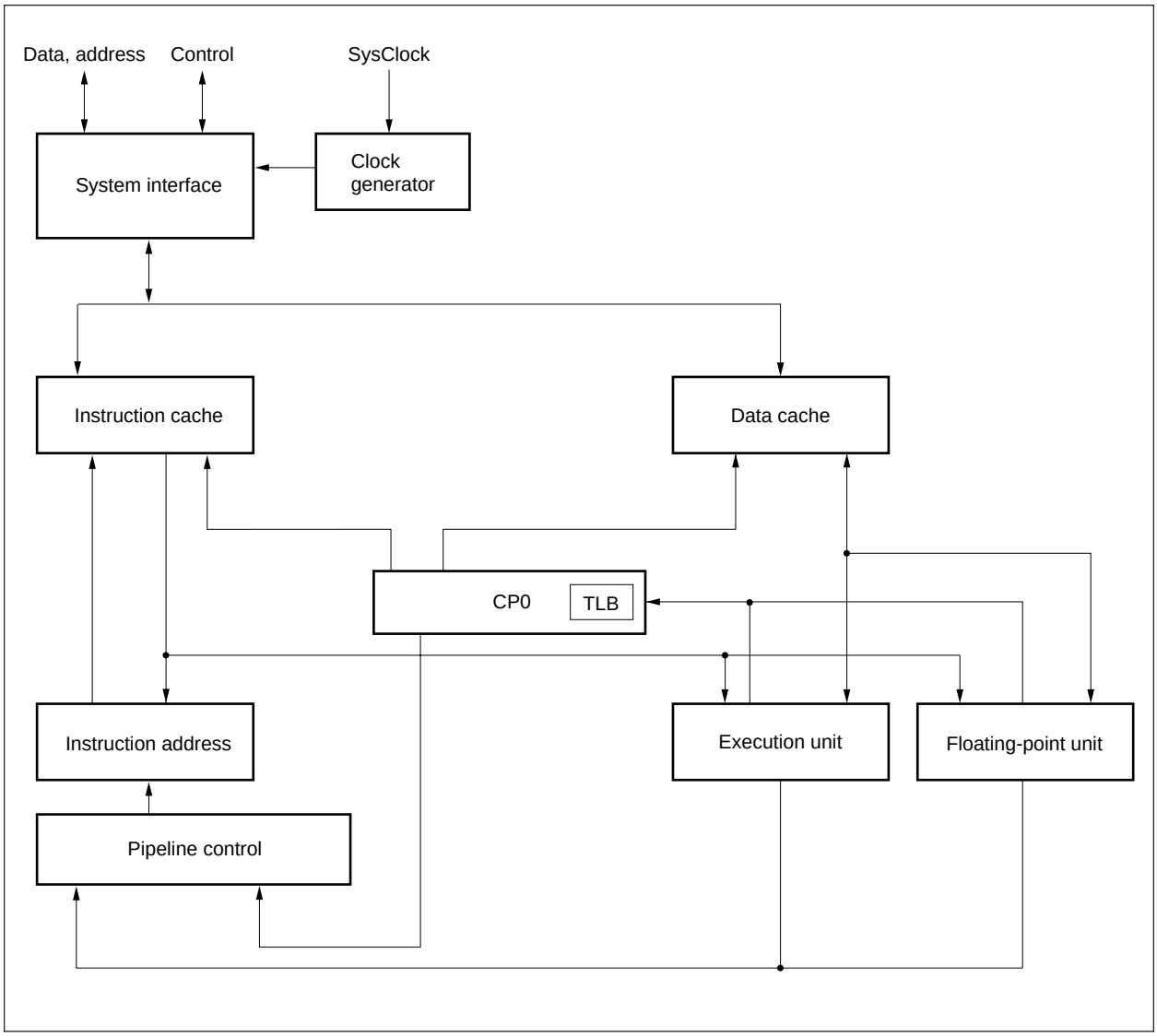
(2) μPD30500A, 30500B

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
A1	GND	C5	$\overline{\text{ScDCE1}}$	F1	SysAD8	L20	SysAD63	U18	V_{DD}	Y1	V_{DD}IO
A2	V_{DD}IO	C6	$\overline{\text{ScDCE0}}$	F2	SysAD38	L21	GND	U19	SysAD17	Y2	V_{DD}IO
A3	GND	C7	$\overline{\text{ScCWE0}}$	F3	SysAD6	M1	SysAD26	U20	SysAD49	Y3	V_{DD}IO
A4	SysAD32	C8	$\overline{\text{ScTCE}}$	F4	GND	M2	SysAD56	U21	GND	Y4	$\overline{\text{Release}}$
A5	GND	C9	ModeIn	F18	GND	M3	SysAD24	V1	V_{DD}	Y5	$\overline{\text{Int3}}$
A6	$\overline{\text{ScCWE1}}$	C10	NC	F19	SysAD1	M4	V_{DD}IO	V2	V_{DD}	Y6	$\overline{\text{Int2}}$
A7	GND	C11	GNDP	F20	SysAD33	M18	V_{DD}IO	V3	V_{DD}	Y7	ScValid
A8	V_{DD}Ok	C12	GND	F21	SysAD3	M19	SysAD29	V4	GND	Y8	GND
A9	GND	C13	ScLine13	G1	GND	M20	SysAD61	V5	$\overline{\text{NMI}}$	Y9	GND
A10	SysClock	C14	ScLine11	G2	SysAD10	M21	SysAD31	V6	GND	Y10	GND
A11	GND	C15	ScLine8	G3	SysAD40	N1	GND	V7	V_{DD}	Y11	$\overline{\text{ExtRqst}}$
A12	ScLine15	C16	ScLine5	G4	V_{DD}IO	N2	SysAD54	V8	V_{DD}IO	Y12	$\overline{\text{RdRdy}}$
A13	GND	C17	ScLine4	G18	V_{DD}IO	N3	SysAD22	V9	GND	Y13	SysCmd8
A14	ScLine12	C18	ScLine0	G19	SysAD35	N4	GND	V10	V_{DD}	Y14	SysCmd5
A15	GND	C19	$\overline{\text{Reset}}$	G20	SysAD5	N18	GND	V11	V_{DD}IO	Y15	SysCmd3
A16	ScLine7	C20	V_{DD}IO	G21	GND	N19	SysAD27	V12	V_{DD}	Y16	SysCmd0
A17	GND	C21	GND	H1	SysAD42	N20	SysAD59	V13	GND	Y17	SysCmdP
A18	ScLine2	D1	V_{DD}	H2	SysAD44	N21	GND	V14	V_{DD}IO	Y18	SysADC1
A19	GND	D2	V_{DD}	H3	SysAD12	P1	SysAD50	V15	V_{DD}	Y19	SysAD15
A20	V_{DD}IO	D3	V_{DD}	H4	V_{DD}	P2	SysAD52	V16	GND	Y20	V_{DD}IO
A21	GND	D4	GND	H18	V_{DD}	P3	SysAD20	V17	V_{DD}IO	Y21	V_{DD}IO
B1	V_{DD}IO	D5	V_{DD}	H19	SysAD7	P4	V_{DD}	V18	GND	AA1	GND
B2	V_{DD}IO	D6	GND	H20	SysAD39	P18	V_{DD}	V19	V_{DD}	AA2	V_{DD}IO
B3	V_{DD}IO	D7	V_{DD}IO	H21	SysAD37	P19	SysAD25	V20	V_{DD}	AA3	GND
B4	SysAD2	D8	V_{DD}	J1	GND	P20	SysAD57	V21	V_{DD}	AA4	$\overline{\text{ValidOut}}$
B5	SysAD0	D9	GND	J2	SysAD46	P21	SysAD55	W1	GND	AA5	GND
B6	$\overline{\text{ScTOE}}$	D10	V_{DD}IO	J3	SysAD14	R1	GND	W2	V_{DD}IO	AA6	$\overline{\text{Int0}}$
B7	$\overline{\text{ScCLR}}$	D11	V_{DD}P	J4	GND	R2	SysAD18	W3	V_{DD}IO	AA7	GND
B8	$\overline{\text{ScTDE}}$	D12	V_{DD}	J18	GND	R3	SysAD48	W4	V_{DD}IO	AA8	GND
B9	ModeClock	D13	GND	J19	SysAD9	R4	V_{DD}IO	W5	$\overline{\text{Int5}}$	AA9	GND
B10	GND	D14	V_{DD}IO	J20	SysAD41	R18	V_{DD}IO	W6	$\overline{\text{Int4}}$	AA10	$\overline{\text{WrRdy}}$
B11	GND	D15	V_{DD}	J21	GND	R19	SysAD53	W7	$\overline{\text{Int1}}$	AA11	GND
B12	GND	D16	GND	K1	SysAD60	R20	SysAD23	W8	GND	AA12	ScMatch
B13	ScLine14	D17	V_{DD}IO	K2	SysAD30	R21	GND	W9	GND	AA13	GND
B14	ScLine10	D18	GND	K3	SysAD62	T1	SysAD16	W10	V_{DD}	AA14	SysCmd6
B15	ScLine9	D19	V_{DD}	K4	V_{DD}IO	T2	SysADC0	W11	$\overline{\text{ValidIn}}$	AA15	GND
B16	ScLine6	D20	V_{DD}	K18	V_{DD}IO	T3	SysADC2	W12	$\overline{\text{ScDOE}}$	AA16	SysCmd2
B17	ScLine3	D21	V_{DD}	K19	SysAD11	T4	GND	W13	SysCmd7	AA17	GND
B18	ScLine1	E1	GND	K20	SysAD43	T18	GND	W14	SysCmd4	AA18	SysADC3
B19	V_{DD}IO	E2	SysAD36	K21	SysAD13	T19	SysAD19	W15	SysCmd1	AA19	GND
B20	V_{DD}IO	E3	SysAD4	L1	GND	T20	SysAD51	W16	SysADC7	AA20	V_{DD}IO
B21	V_{DD}IO	E4	V_{DD}	L2	SysAD58	T21	SysAD21	W17	SysADC5	AA21	GND
C1	GND	E18	V_{DD}	L3	SysAD28	U1	GND	W18	SysAD47		
C2	V_{DD}IO	E19	ScWord1	L4	V_{DD}	U2	SysADC4	W19	BigEndian		
C3	$\overline{\text{ColdReset}}$	E20	ScWord0	L18	V_{DD}	U3	SysADC6	W20	V_{DD}IO		
C4	SysAD34	E21	GND	L19	SysAD45	U4	V_{DD}	W21	GND		

PIN NAMES

BigEndian:	Endian Mode Select
$\overline{\text{ColdReset}}$:	Cold Reset
$\overline{\text{ExtRqst}}$:	External Request
GND:	Ground
GNDP:	Quiet GND for PLL
$\overline{\text{Int}}$ (0:5):	Interrupt Request
ModeClock:	Boot Mode Clock
ModeIn:	Boot Mode Data In
NC:	No Connection
$\overline{\text{NMI}}$:	Non-maskable Interrupt Request
$\overline{\text{RdRdy}}$:	Read Ready
$\overline{\text{Release}}$:	Release Interface
$\overline{\text{Reset}}$:	Reset
$\overline{\text{ScCLR}}$:	Secondary Cache Block Clear
$\overline{\text{ScCWE}}$ (0:1):	Secondary Cache Write Enable
$\overline{\text{ScDCE}}$ (0:1):	Data RAM Chip Enable
$\overline{\text{ScDOE}}$:	Data RAM Output Enable
ScLine (0:15):	Secondary Cache Line Index
ScMatch:	Secondary Cache Tag Match
$\overline{\text{ScTCE}}$:	Secondary Cache Tag RAM Chip Enable
$\overline{\text{ScTDE}}$:	Secondary Cache Tag RAM Data Enable
$\overline{\text{ScTOE}}$:	Secondary Cache Tag RAM Output Enable
ScValid:	Secondary Cache Valid
ScWord (0:1):	Secondary Cache Word Index
SysAD (0:63):	System Address/Data Bus
SysADC (0:7):	System Address/Data Check Bus
SysClock:	System Clock
SysCmd (0:8):	System Command/Data Identifier
SysCmdP:	System Command/Data Identifier Bus Parity
$\overline{\text{ValidIn}}$:	Valid Input
$\overline{\text{ValidOut}}$:	Valid Output
V_{DD}:	Power Supply (μPD30500)
V_{DD}:	Power Supply for Processor Core (μPD30500A, 30500B)
V_{DD}IO:	Power Supply for Processor I/O (μPD30500A, 30500B only)
V_{DD}Ok:	V_{DD} is OK
V_{DD}P:	Quiet V_{DD} for PLL
$\overline{\text{WrRdy}}$:	Write Ready

INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Pin Name	I/O	Function
SysAD (0:63)	I/O	System address/data bus. 64-bit bus for communication between processor, secondary cache and external agent.
SysADC (0:7)	I/O	System address/data check bus. 8-bit bus including check bits for the SysAD bus.
SysCmd (0:8)	I/O	System command/data ID bus. 9-bit bus for communication of commands and data identifiers between processor and external agent.
SysCmdP	I/O	System command/data ID bus parity. 1-bit even number parity bit for the SysCmd bus.
$\overline{\text{ValidIn}}$	Input	Valid in. Signal indicating that external agent has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{ValidOut}}$	Output	Valid out. Signal indicating that processor has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{ExtRqst}}$	Input	External request. Signal used by external agent to request for its use by system interface.
$\overline{\text{Release}}$	Output	Interface release. Signal indicating that the processor has released the system interface to the slave state.
$\overline{\text{WrRdy}}$	Output	Write ready. Signal indicating that the external agent can accept a processor write request.
$\overline{\text{RdRdy}}$	Input	Read ready. Signal indicating that external agent can accept a processor read request.
$\overline{\text{ScCLR}}$	Output	Secondary cache block clear. Clears all the valid bits of the tag RAM.
$\overline{\text{ScCWE (0:1)}}$	Output	Secondary cache write enable. Write enable signal for the secondary cache RAM.
$\overline{\text{ScDCE (0:1)}}$	Output	Data RAM chip select. Chip select signal for secondary cache RAM.
$\overline{\text{ScDOE}}$	Input	Data RAM output enable. Data output enable signal from the external agent.
ScLine (0:15)	Output	Secondary cache line index. Cache line index output of the secondary cache.
ScMatch	Input	Secondary cache tag match. Tag match signal from secondary cache tag RAM.
$\overline{\text{ScTCE}}$	Output	Secondary cache tag RAM chip select. Chip select signal of the secondary cache tag RAM.
$\overline{\text{ScTDE}}$	Output	Secondary cache tag RAM data enable. Data enable signal from the secondary cache tag RAM.
$\overline{\text{ScTOE}}$	Output	Secondary cache tag RAM output enable. Output enable signal from the secondary cache tag RAM.
ScWord (0:1)	I/O	Secondary cache word index. Signal indicating that the double word of the secondary cache index is correct.
ScValid	I/O	Secondary cache valid. Signal indicating that the data of the secondary cache is valid.

Pin Name	I/O	Function
$\overline{\text{Int (0:5)}}$	Input	Interrupt. General-purpose processor interrupt requests whose input statuses can be confirmed by bits 15 through 10 of cause register.
$\overline{\text{NMI}}$	Input	Non-maskable interrupt. Interrupt request that cannot be masked.
$\overline{\text{ColdReset}}$	Input	Cold reset. Signal initializing the internal status of the processor. Inactivate this signal in synchronization with SysClock.
$\overline{\text{Reset}}$	Input	Reset. Signal generating a reset exception, without initializing the internal status of the processor. Inactivate this signal in synchronization with SysClock.
SysClock	Input	System clock. Clock input signal to processor.
BigEndian	Input	Endian mode setting. This signal sets the endian mode of the system interface. When setting the endian mode with this signal, specify little endian with the data from the ModeIn pin that is input at reset. To set the endian mode with the data from the ModeIn pin, fix this signal to 0. BigEndian / Bit 8 of boot mode / Mode 1 / 1 / — 1 / 0 / Big endian 0 / 1 / Big endian 0 / 0 / Little endian
ModeClock	Output	Boot mode clock. Successive boot mode data clock output resulting from dividing SysClock by 256.
ModeIn	Input	Boot mode data input. Input of initialization bit stream.
★ V_{DD}Ok	Input	V_{DD} and V_{DD}IO[Note1] are valid. Signal indicating that the voltage supplied to the V_R5000 is reached to the rated level[Note2] for 100 ms or more, and that that status is stabilized. When V_{DD}Ok is asserted active, the V_R5000 starts an initialization sequence.
V_{DD}P	–	PLL V_{DD}. Power supply for internal PLL.
GNDP	–	PLL GND. Ground for internal PLL.
V_{DD}	–	• V_R5000 Positive power supply pin (3.3 V) • V_R5000A Power supply pin for core (2.5 V) • V_R5000B Power supply pin for core (1.8 V)
V_{DD}IO[Note1]	–	Power supply pin for I/O (3.3 V)
GND	–	Ground pin.

Notes 1. V_{DD}IO is only for V_R5000A and V_R5000B.

2. V_R5000: V_{DD} = 3.135 V
V_R5000A: V_{DD} = 2.375 V, V_{DD}IO = 3.135 V
V_R5000B: V_{DD} = 1.7 V, V_{DD}IO = 3.135 V

2. ELECTRICAL SPECIFICATIONS

2.1 μPD30500

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage[Note]	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Operating case temperature	T_C	PGA package	0 to +70	°C
		BGA package	0 to +85	°C
Storage temperature	T_{stg}	PGA package	–65 to +150	°C
		BGA package	–40 to +125	°C

Note The upper limit of the input voltage (V_{DD} + 0.3) is +4.0 V.

Cautions 1. Do not short circuit two or more outputs at the same time.

2. The quality of the product may be degraded if the absolute maximum rating of even one of the above parameters is exceeded, even momentarily. Absolute maximum ratings, therefore, specify the values which if exceeded may physically damage the product. Use the product never exceeding these ratings.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_C = 0 to +70°C (PGA Package), T_C = 0 to +85°C (BGA Package), V_{DD} = 3.3 V ±5%)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
High-level output voltage	V_{OH}	V_{DD} = MIN., I_{OH} = –4 mA		2.4		V
Low-level output voltage	V_{OL}	V_{DD} = MIN., I_{OL} = 4 mA			0.4	V
High-level input voltage[Note 1]	V_{IH}			2.0	V_{DD} + 0.3	V
Low-level input voltage[Note 1]	V_{IL}			–0.5	+0.8	V
		Pulse of less than 10 ns		–1.5	+0.8	V
High-level input voltage[Note 2]	V_{IHC}			0.8 × V_{DD}	V_{DD} + 0.3	V
Low-level input voltage[Note 2]	V_{ILC}			–0.5	0.2 × V_{DD}	V
		Pulse of less than 10 ns		–1.5	0.2 × V_{DD}	V
Supply current	I_{DD}	Normal operation	150 MHz		2.16	A
			180 MHz		2.54	A
			200 MHz		2.8	A
		Standby			0.25	A
Input leakage current	I_{LI}			–5	+5	μA
Input/output leakage current	I_{LIO}			–5	+5	μA

Notes 1. Not applied to the SysClock pin.

2. Applied to the SysClock pin only.

Remark The operating supply current is almost proportional to the operating clock frequency.

Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{In}			5	pF
Output capacitance	C_{out}			7	pF

AC Characteristics (T_C = 0 to +70°C (PGA Package), T_C = 0 to +85°C (BGA Package), V_{DD} = 3.3 V ±5%)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}		3.0		ns
System clock low-level width	t_{CL}		3.0		ns
System clock frequency[Notes 1, 2]		150 MHz	20	75	MHz
		180 MHz	20	90	MHz
		200 MHz	20	100	MHz
System clock cycle	t_{CP}	150 MHz	13.3	50	ns
		180 MHz	11.1	50	ns
		200 MHz	10	50	ns
System clock jitter	t_{ji}	System clock frequency > 66 MHz		±125	ps
		System clock frequency ≤ 66 MHz		±250	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns
Mode clock cycle	t_{MOC}		256 × t_{CP}		ns

Notes 1. The operation of the V_R5000 is guaranteed only when the PLL is operating

2. The operation is guaranteed if the internal operating frequency 100 MHz or higher.

System Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output hold time	t_{DM}	Modebit (14 : 13) = 10	1.0		ns
		Modebit (14 : 13) = 11	1.1		ns
		Modebit (14 : 13) = 00	1.3		ns
		Modebit (14 : 13) = 01	1.3		ns
Data output delay time	t_{DO}			5.0	ns
Data input setup time	t_{DS}		1.6		ns
Data input hold time	t_{DH}		0.5		ns

Boot Mode Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
More data setup time	t_{MDS}		$t_{CP} \times 0.35$		ns
Mode data hold time	t_{MDH}		$t_{CP} \times 0.35$		ns

Load Coefficient

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Load coefficient	CLD			1.5	ns/25 pF

★ 2.2 μPD30500A

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD}IO$		–0.5 to +4.0	V
	V_{DD}		–0.3 to +3.3	V
Input voltage[Note]	V_I		–0.5 to $V_{DD}IO$ + 0.3	V
		Pulse of less than 10 ns	–1.5 to $V_{DD}IO$ + 0.3	V
Operating case temperature	T_C		0 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

Note The upper limit of the input voltage ($V_{DD}IO$ + 0.3) is +4.0 V.

Cautions 1. Do not short circuit two or more outputs at the same time.

2. The quality of the product may be degraded if the absolute maximum rating of even one of the above parameters is exceeded, even momentarily. Absolute maximum ratings, therefore, specify the values which if exceeded may physically damage the product. Use the product never exceeding these ratings.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_C = 0 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = 2.5 V ±5%)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-level output voltage	V_{OH}	$V_{DD}IO$ = MIN., I_{OH} = –4 mA	2.4		V
Low-level output voltage	V_{OL}	$V_{DD}IO$ = MIN., I_{OL} = 4 mA		0.4	V
High-level input voltage[Note 1]	V_{IH}		2.0	$V_{DD}IO$ + 0.3	V
Low-level input voltage[Note 1]	V_{IL}		–0.5	+0.8	V
		Pulse of less than 10 ns	–1.5	+0.8	V
High-level input voltage[Note 2]	V_{IHC}		0.8 × $V_{DD}IO$	$V_{DD}IO$ + 0.3	V
Low-level input voltage[Note 2]	V_{ILC}		–0.5	0.2 × $V_{DD}IO$	V
		Pulse of less than 10 ns	–1.5	0.2 × $V_{DD}IO$	V
★ Supply current	I_{DD}			1.8	A
	$I_{DD}IO$	System clock frequency = 50 MHz		0.7	A
		System clock frequency = 67 MHz		0.85	A
		System clock frequency = 83 MHz		0.95	A
		System clock frequency = 100 MHz		1.15	A
Input leakage current	I_{LI}		–5	+5	μA
Input/output leakage current	I_{LIO}		–5	+5	μA

Notes 1. Not applied to the SysClock pin.

2. Applied to the SysClock pin only.

Power Application Sequence

Two kinds of power sources are provided with the VR5000A. The sequence of the power application order is not fixed. However, make sure that either of the power supplies does not remain turned on for 1 second or more while the other remains off.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Power application delay	t_{DP}		0	1	sec

Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{in}			5	pF
Output capacitance	C_{out}			7	pF

AC Characteristics (T_C = 0 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = 2.5 V ±5%)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}		3.0		ns
System clock low-level width	t_{CL}		3.0		ns
System clock frequency **Notes 1, 2**			20	100	MHz
System clock cycle	t_{CP}		10	50	ns
System clock jitter	t_{ji}	System clock frequency > 66 MHz		±125	ps
		System clock frequency ≤ 66 MHz		±250	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns
Mode clock cycle	t_{MOC}		256 × t_{CP}		ns

Notes 1. The operation of the VR5000A is guaranteed only when the PLL is operating

2. The operation is guaranteed if the internal operating frequency 100 MHz or higher.

System Interface Parameter

	Parameter	Symbol	Condition	MIN.	MAX.	Unit
	Data output hold time	t_{DM}	Modebit (14 : 13) = 10	1.3		ns
			Modebit (14 : 13) = 11	1.4		ns
			Modebit (14 : 13) = 00	1.5		ns
			Modebit (14 : 13) = 01	1.5		ns
★	Data output delay time	t_{DO}	PClock/SysClock division ratio = 2, 3, 4, 5, 6, 7, 8,		5.0	ns
			PClock/SysClock division ratio = 2.5		7.0	ns
	Data input setup time	t_{DS}		1.6		ns
	Data input hold time	t_{DH}		0.5		ns

Boot Mode Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Mode data setup time	t_{MDS}		$t_{CP} \times 0.35$		ns
Mode data hold time	t_{MDH}		$t_{CP} \times 0.35$		ns

Load Coefficient

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Load coefficient	CLD			1.5	ns/25 pF

2.3 μPD30500B (Preliminary)

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD}IO$		–0.5 to +4.0	V
	V_{DD}		–0.3 to +2.5	V
Input voltage[Note]	V_I		–0.5 to $V_{DD}IO$ + 0.3	V
		Pulse of less than 10 ns	–1.5 to $V_{DD}IO$ + 0.3	V
Operating case temperature	T_C		0 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

Note The upper limit of the input voltage ($V_{DD}IO$ + 0.3) is +4.0 V.

Cautions 1. Do not short circuit two or more outputs at the same time.

2. The quality of the product may be degraded if the absolute maximum rating of even one of the above parameters is exceeded, even momentarily. Absolute maximum ratings, therefore, specify the values which if exceeded may physically damage the product. Use the product never exceeding these ratings.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_C = 0 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = 1.8 V ±0.1 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-level output voltage	V_{OH}	$V_{DD}IO$ = MIN., I_{OH} = –4 mA	2.4		V
Low-level output voltage	V_{OL}	$V_{DD}IO$ = MIN., I_{OL} = 4 mA		0.4	V
High-level input voltage[Note 1]	V_{IH}		2.0	$V_{DD}IO$ + 0.3	V
Low-level input voltage[Note 1]	V_{IL}		–0.5	+0.8	V
		Pulse of less than 10 ns	–1.5	+0.8	V
High-level input voltage[Note 2]	V_{IHC}		0.8 × $V_{DD}IO$	$V_{DD}IO$ + 0.3	V
Low-level input voltage[Note 2]	V_{ILC}		–0.5	0.2 × $V_{DD}IO$	V
		Pulse of less than 10 ns	–1.5	0.2 × $V_{DD}IO$	V
Input leakage current	I_{LI}		–5	+5	μA
Input/output leakage current	I_{LIO}		–5	+5	μA

Notes 1. Not applied to the SysClock pin.

2. Applied to the SysClock pin only.

Power Application Sequence

Two kinds of power sources are provided with the V_R5000B. The sequence of the power application order is not fixed. However, make sure that either of the power supplies does not remain turned on for 1 second or more while the other remains off.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Power application delay	t_{DP}		0	1	se

Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{In}			5	pF
Output capacitance	C_{out}			7	pF

AC Characteristics (T_C = 0 to +85°C, $V_{DD}IO$ = 3.3 V ±5%, V_{DD} = 1.8 V ±0.1 V)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}		3.0		ns
System clock low-level width	t_{CL}		3.0		ns
System clock frequency[Notes 1, 2]			20	100	MHz
System clock cycle	t_{CP}		10	50	ns
System clock jitter	t_{ji}	System clock frequency > 66 MHz		±125	ps
		System clock frequency ≤ 66 MHz		±250	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns
Mode clock cycle	t_{MOC}		256 × t_{CP}		ns

Notes 1. The operation of the V_R5000B is guaranteed only when the PLL is operating

2. The operation is guaranteed if the internal operating frequency 100 MHz or higher.

System Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output hold time	t_{DM}	Modebit (14 : 13) = 10	1.3		ns
		Modebit (14 : 13) = 11	1.4		ns
		Modebit (14 : 13) = 00	1.5		ns
		Modebit (14 : 13) = 01	1.5		ns
Data output delay time	t_{DO}			5.0	ns
Data input setup time	t_{DS}		1.6		ns
Data input hold time	t_{DH}		0.5		ns

Boot Mode Interface Parameter

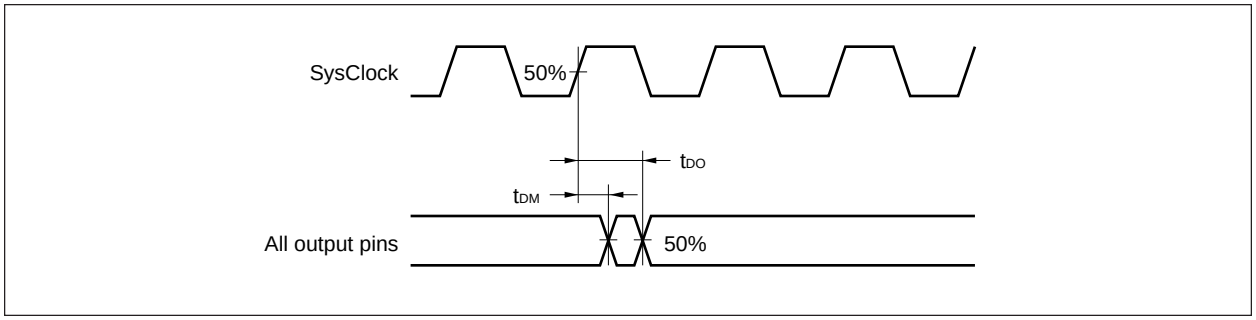
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Mode data setup time	t_{MDS}		$t_{CP} \times 0.35$		ns
Mode data hold time	t_{MDH}		$t_{CP} \times 0.35$		ns

Load Coefficient

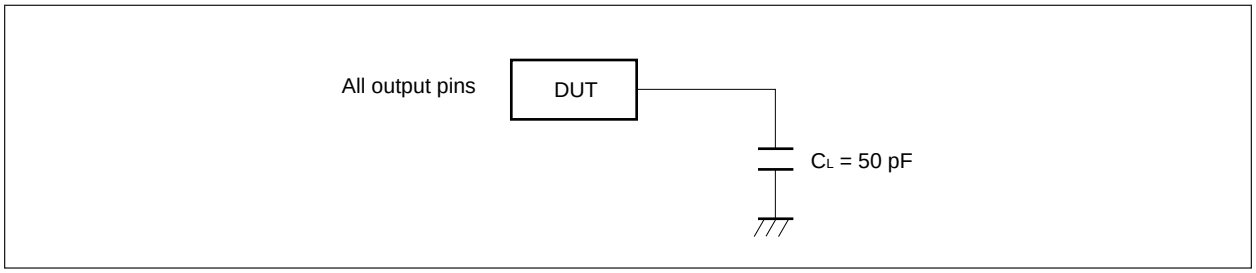
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Load coefficient	CLD			1.5	ns/25 pF

2.4 Test Condition

Test point

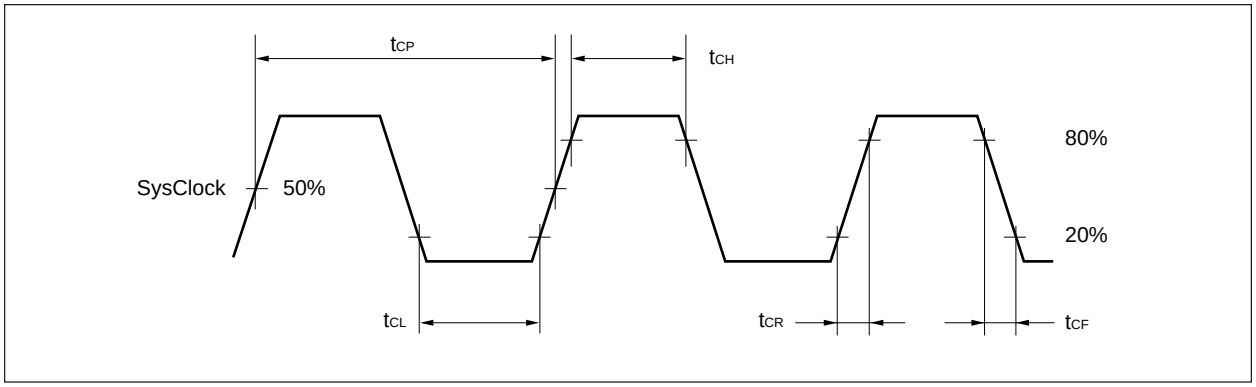


Load Conditions

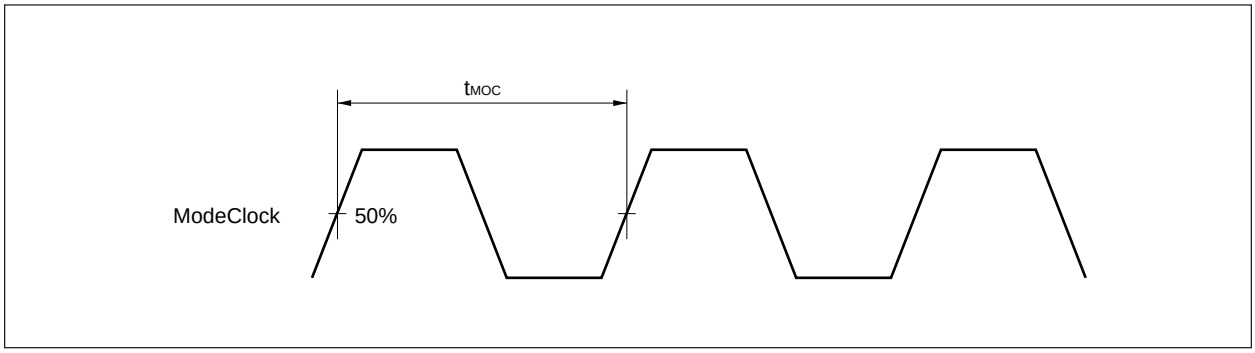


2.5 Timing Chart

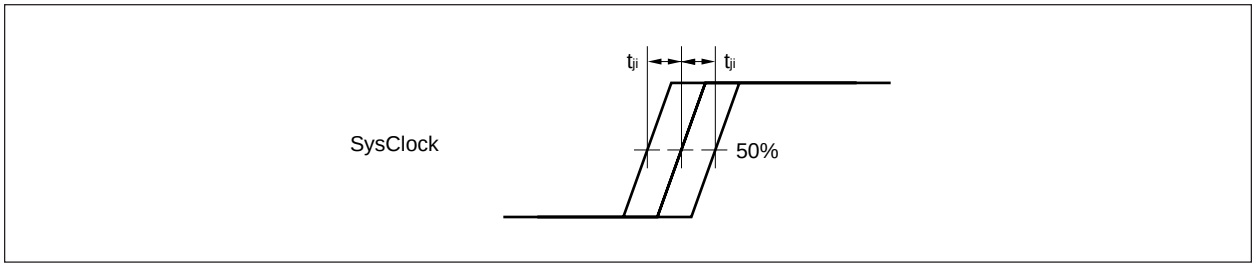
Clock timing



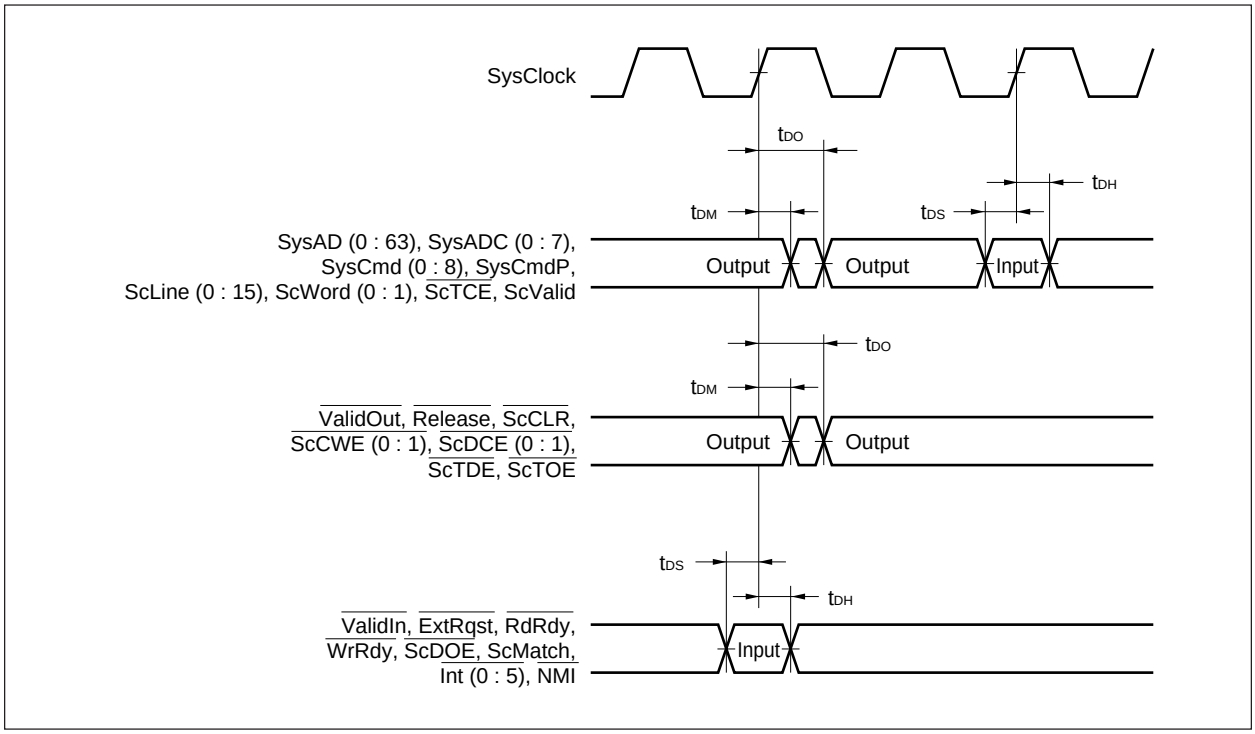
Mode clock timing



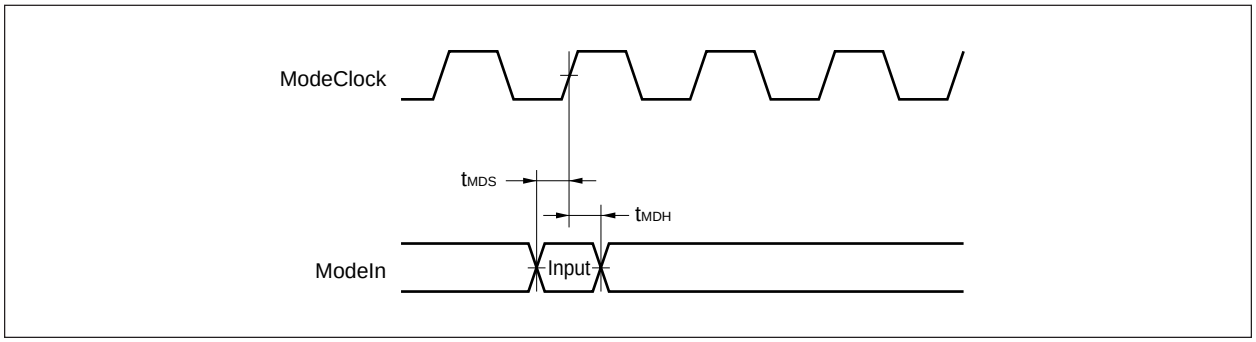
Clock jitter



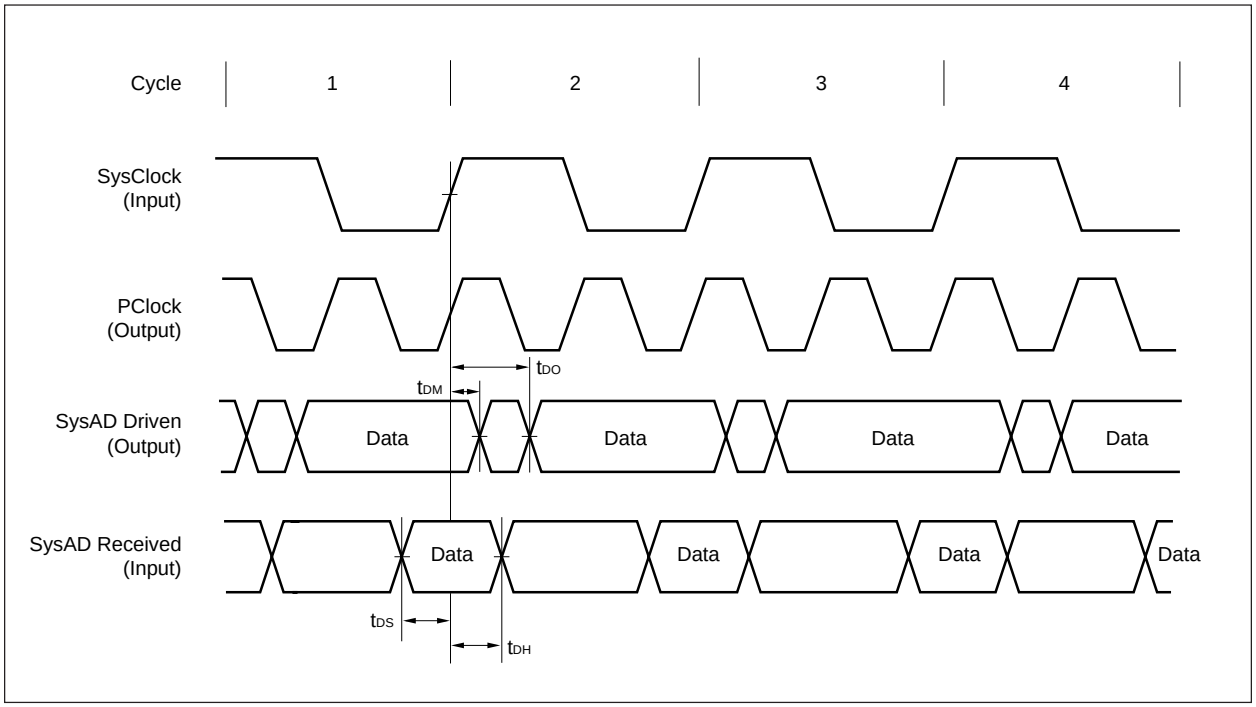
System interface edge timing



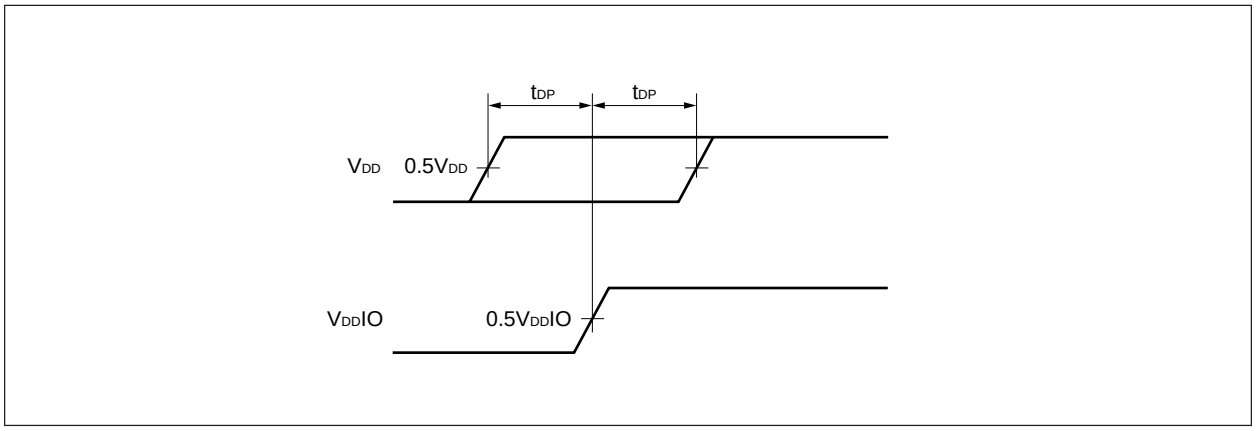
Boot mode interface edge timing



Clocking relations

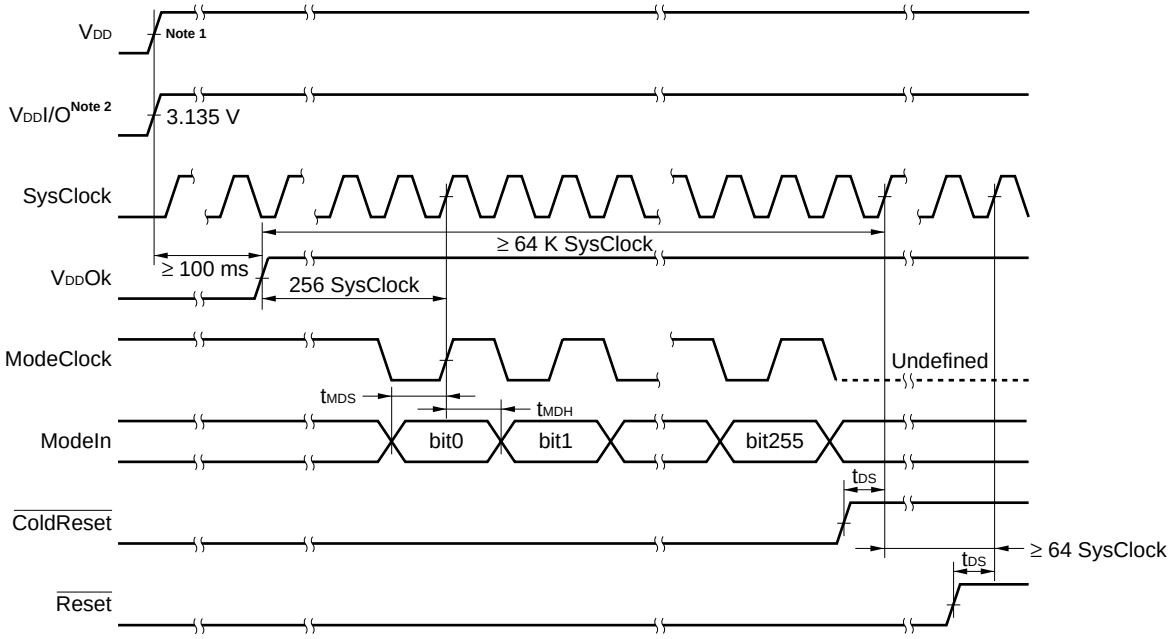


Power application sequence (V_R5000A, V_R5000B only)



Reset Timing

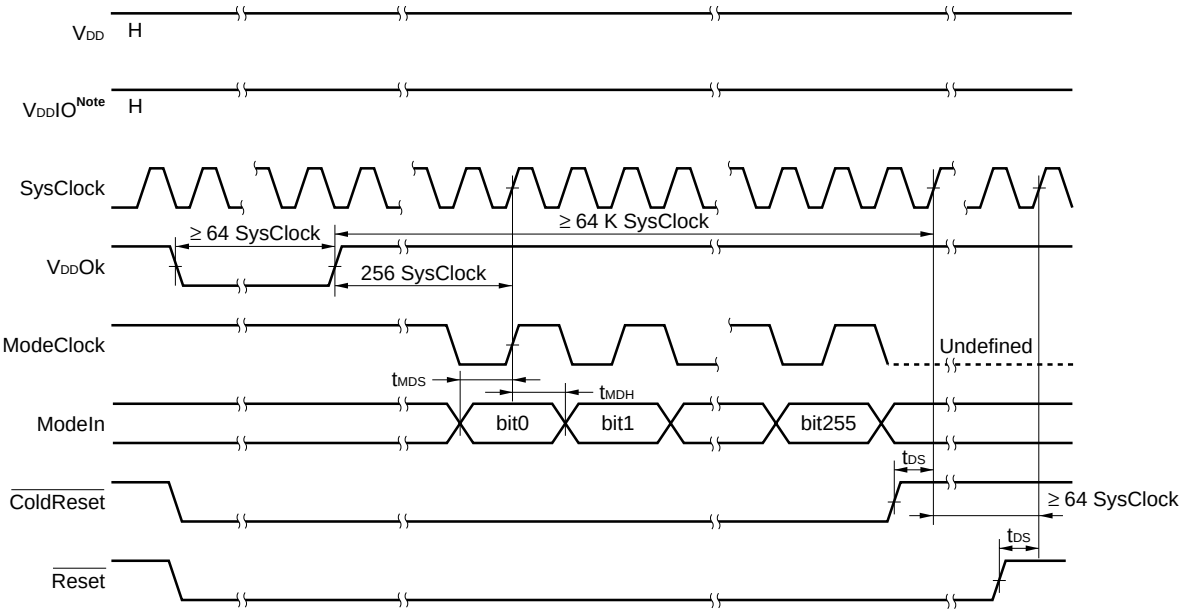
Power-on reset timing



Notes 1. 3.135 V (VR5000), 2.375 V (VR5000A), 1.7 V (VR5000B)

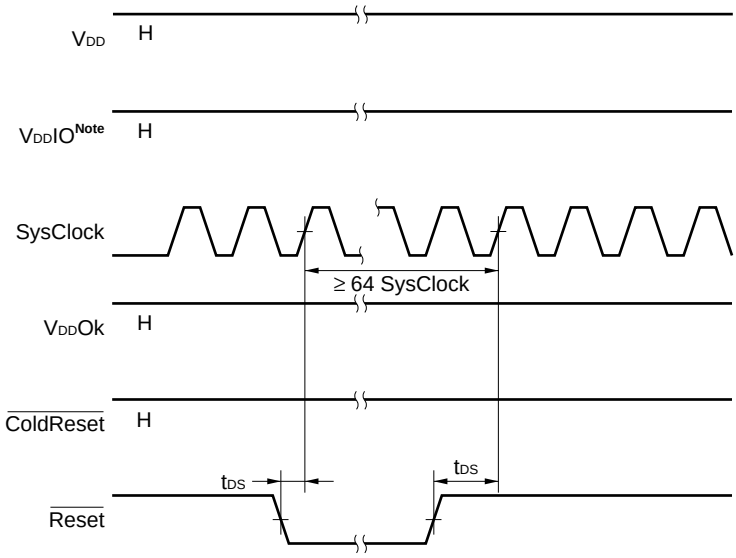
2. VR5000A, VR5000B only

Cold reset timing



Note VR5000A, VR5000B only

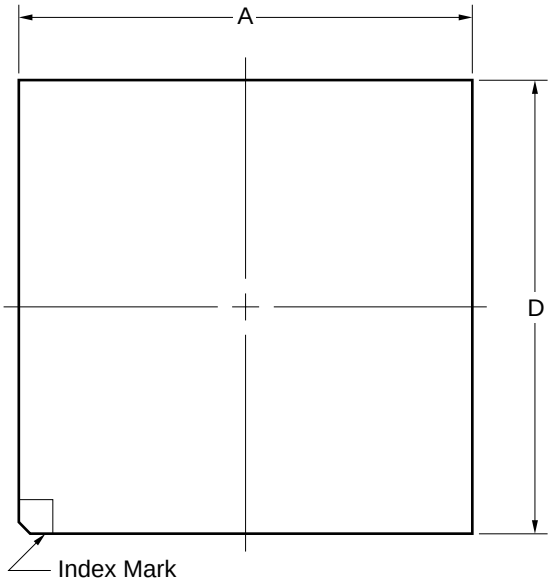
Warm reset timing



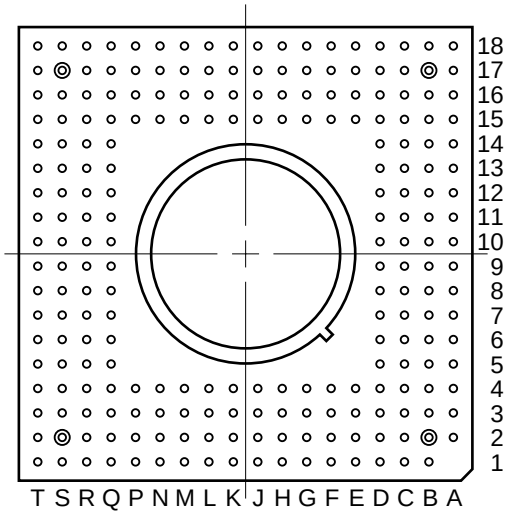
Note VR5000A, VR5000B only

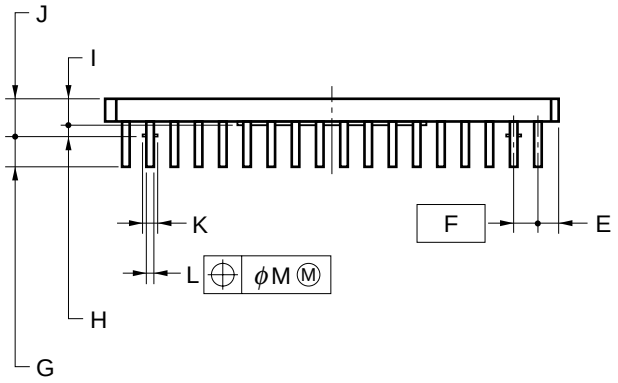
3. PACKAGE DRAWING

223 PIN CERAMIC PGA



< Bottom View >



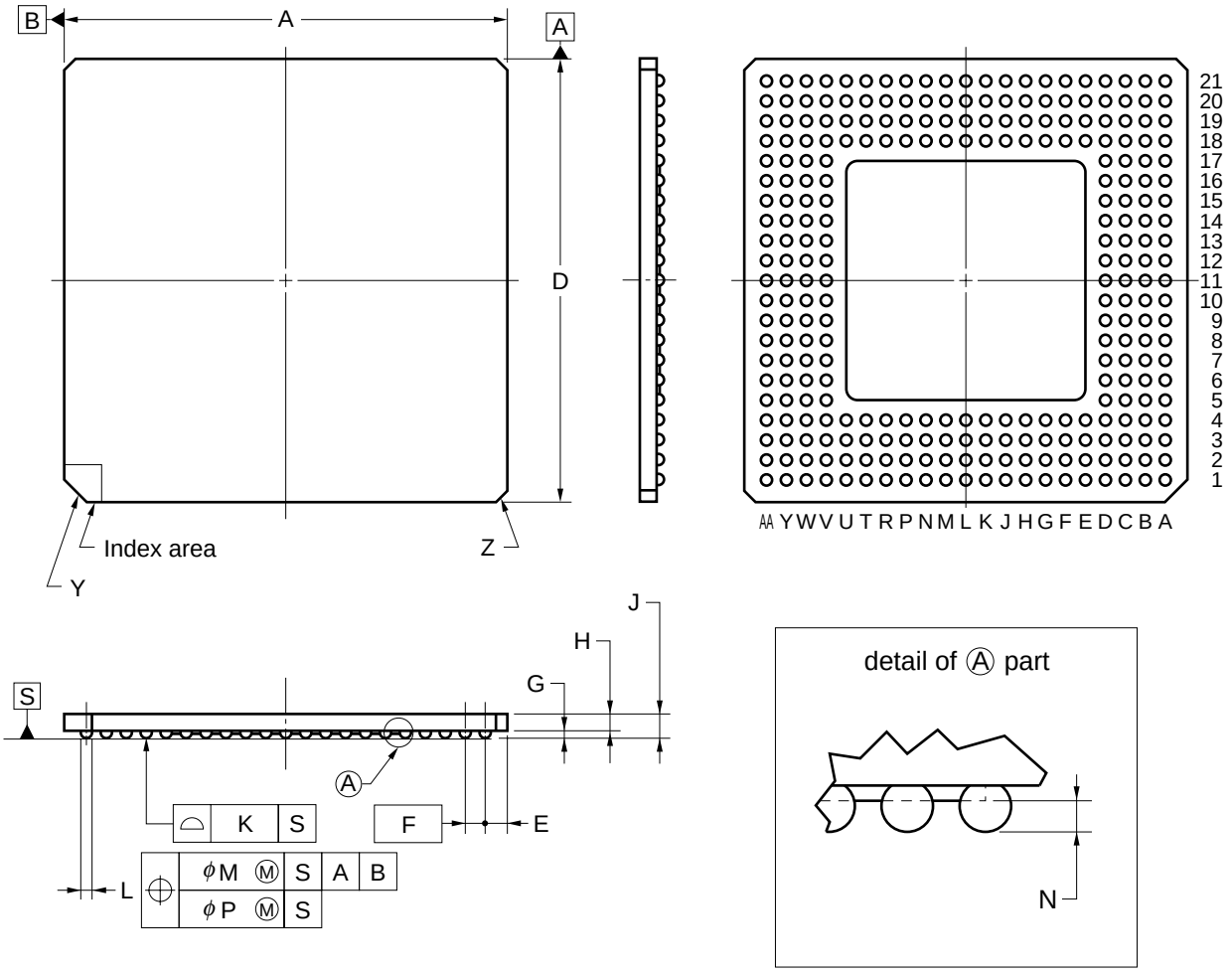


NOTE
Each lead centerline is located within φ0.254(φ0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	47.24±0.25	1.860±0.010
D	47.24±0.25	1.860±0.010
E	2.03	0.080
F	2.54(T.P.)	0.100(T.P.)
G	3.30±0.2	0.130±0.008
H	0.50 MIN.	0.019 MIN.
I	2.82	0.111
J	3.98 MAX.	0.157 MAX.
K	φ1.27±0.2	0.050±0.008
L	φ0.46±0.05	φ0.018±0.002
M	0.254	0.010

X223RJ-100A-1

★ 272-PIN PLASTIC BGA (C/D advanced type) (29x29)



ITEM	MILLIMETERS
A	29.00±0.20
D	29.00±0.20
E	1.80
F	1.27 (T.P.)
G	0.60±0.10
H	0.90
J	1.50±0.20
K	0.15
L	φ0.75±0.15
M	0.30
N	0.25 MIN.
P	0.10
Y	C1.5
Z	C0.5

S272S2-127-C6-3

4. RECOMMENDED SOLDERING CONDITIONS

Soldering this product under the following soldering conditions is recommended.

For the details of the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and recommended other than those recommended, consult NEC.

(1) Soldering Conditions of Surface Mount Type

μPD30500S2-150: 272-pin plastic BGA (C/D advanced type) (29 × 29)
μPD30500S2-180: 272-pin plastic BGA (C/D advanced type) (29 × 29)
μPD30500S2-200: 272-pin plastic BGA (C/D advanced type) (29 × 29)
★ **μPD30500AS2-250: 272-pin plastic BGA (C/D advanced type) (29 × 29)**
μPD30500BS2-300[Note 1]: 272-pin plastic BGA (C/D advanced type) (29 × 29)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec max. (210°C min.), Number of times: 3 times max., Number of days: 3[Note 2] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-103-3
VPS	Package peak temperature: 215°C, Time: 25 to 40 sec max. (200°C min.), Number of times: 3 times max., Number of days: 3[Note 2] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 sec max. (per device side)	—

Notes 1. Under development

2. Number of days in storage after the dry pack has been opened. The storage conditions are at 25°C, 65% RH MAX.

Caution Do not use two or more soldering methods in combination (except partial heating).

(2) Soldering Conditions of Insertion Type

μPD30500RJ-150: 223-pin ceramic PGA (48 × 48)
μPD30500RJ-180: 223-pin ceramic PGA (48 × 48)
μPD30500RJ-200: 223-pin ceramic PGA (48 × 48)

Soldering Method	Soldering Conditions
Wave soldering (Pin only)	Solder bath temperature: 260°C max., Time: 10 sec max.
Partial heating	Pin temperature: 300°C max., Time: 3 sec max. (per pin)

Caution Wave soldering is only for the lead part in order that jet solder cannot contact with the chip directly.

APPENDIX DIFFERENCES BETWEEN THE VR5000 AND VR4310™

	Item		VR5000	VR4310
	Operating frequency	Internal	200 MHz MAX.	167 MHz MAX.
		External	100 MHz MAX.	83.3 MHz MAX.
	Pipeline		2-way super scalar 5-stage pipeline	5-stage pipeline
	Cache	Primary instruction cache	32 Kbytes	16 Kbytes
		Primary data cache	32 Kbytes	8 Kbytes
		Secondary cache interface	Provided	None
		Data protection	Byte parity	None
	System bus	Write data transfer rate	9 types (DDDD/DDxDDx/ DDxxDDxx/DxDxDxDx/ DDxxxDDxxx/DDxxxxDDxxxx/ DxxDxxDxxDxx/ DDxxxxxxDDxxxxxx/DxxxDxxx)	2 types (D/Dxx)
		Initialization pin at reset	ModeIn (dedicated serial pin)	DivMode (0:2)
		Status after last data write	Access ends	Last data retained when transfer rate is set
	Integer operation unit	Corresponding instruction	MIPS I, II, III, IV instruction sets	MIPS I, II, III instruction sets
	JTAG interface		None	Provided
	SyncOut-SyncIn bus		None	Provided
	Clock interface	Multiplication ratio of input to internal	2, 3, 4, 5, 6, 7, 8	1.5, 2, 2.5, 3, 4, 5, 6
		Division ratio of internal to bus	2, 3, 4, 5, 6, 7, 8	1.5, 2, 2.5, 3, 4, 5, 6
		Clock output	None	TClock
★	Power management mode		Standby mode (pipline does not operate)	Not provided
	PRId register		Imp = 0x23	Imp = 0x0B

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Note that this document is not designated as 'preliminary', while some of the related documents are preliminary versions.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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