NEC

MOS INTEGRATED CIRCUIT

μPD4216805

16 M-BIT DYNAMIC RAM
2 M-WORD BY 8-BIT, HYPER PAGE MODE

DESCRIPTION

The μPD4216805 is a 2 097 152 words by 8 bits dynamic CMOS RAM with optional hyper page mode.
Hyper page mode is a kind of the page mode and is useful for the read operation.
The μPD4216805 is packed in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.

FEATURES

- Hyper page mode
- 2 097 152 words by 8 bits organization
- Single +5.0 V±10 % power supply
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 4 096 refresh cycles /64 ms

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD4216805-50	50 ns	84 ns	20 ns
μPD4216805-60	60 ns	104 ns	25 ns
μPD4216805-70	70 ns	124 ns	30 ns

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD4216805G5-50	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4216805G5-60	60 ns		
μPD4216805G5-70	70 ns		
~~μPD4216805G5-50-7KD~~	50 ns	~~28-pin Plastic TSOP (II)~~ (400 mil) ~~Reverse bent~~	
μPD4216805G5-60-7KD	~~60 ns~~		
~~μPD4216805G5-70-7KD~~	70 ns		
μPD4216805LE-50	50 ns	28-pin Plastic SOJ (400 mil)	
μPD4216805LE-60	60 ns		
μPD4216805LE-70	70 ns		

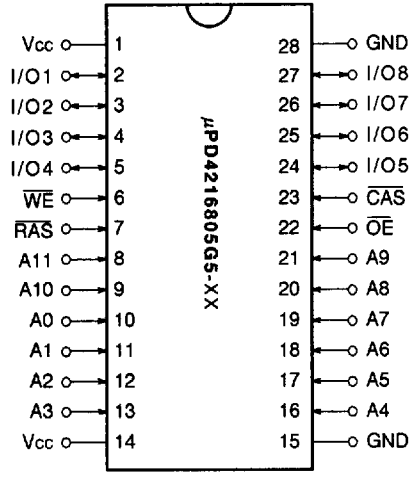
QUALITY GRADE

Standard

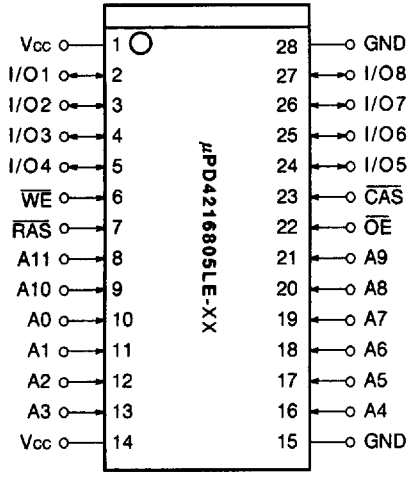
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking side)

28-pin Plastic TSOP (II) (400 mil)

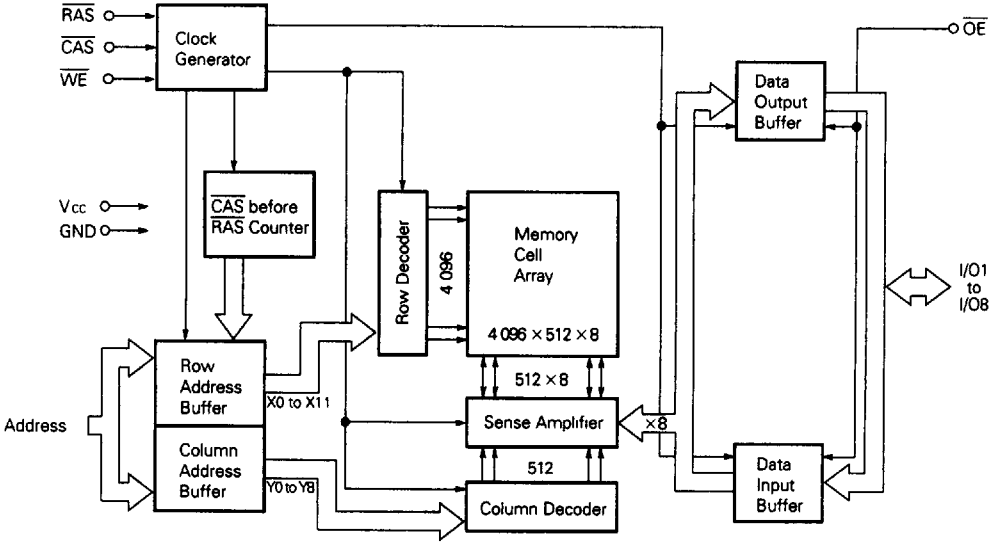


28-pin Plastic SOJ (400 mil)



A0 to A11	: Address Inputs
I/O1 to I/O8	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply
GND	: Ground

BLOCK DIAGRAM



INPUT/OUTPUT PIN FUNCTIONS

The μPD4216805 has input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 21-bit of address signal, upper 12-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC}+1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O8			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 50 ns		100	mA	3,4,7
			t_{RAC} = 60 ns		90		
			t_{RAC} = 70 ns		80		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH}$ (MIN.)	I_O = 0 mA		2	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$–0.2 V	I_O = 0 mA		1		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH}$ (MIN.) $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 50 ns		100	mA	3,4,5,7
			t_{RAC} = 60 ns		90		
			t_{RAC} = 70 ns		80		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL}$ (MAX.) $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC}$(MIN.) I_O = 0 mA	t_{RAC} = 50 ns		100	mA	3,4,6
			t_{RAC} = 60 ns		90		
			t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC}$(MIN.) I_O = 0 mA	t_{RAC} = 50 ns		100	mA	3,4
			t_{RAC} = 60 ns		90		
			t_{RAC} = 70 ns		80		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) Notes 8, 9 (1/2)

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	84		104		124		ns	
Read Modify Write Cycle Time	t_{RWC}	107		133		157		ns	
Access Time from $\overline{RAS}$	t_{RAC}		50		60		70	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		13		15		18	ns	10, 11
Access Time from Column Address	t_{AA}		25		30		35	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		27		35		40	ns	11
Access Time from $\overline{OE}$	t_{OEA}		13		15		18	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	9	25	12	30	12	35	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Delay Time	t_{OED}	10		13		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	12,18
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	30		40		50		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	50	10 000	60	10 000	70	10 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	7		10		12		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	35		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	11	37	14	45	14	52	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	7		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	27		35		40		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	7		10		10		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	7		10		12		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25		30		35		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7		10		10		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	7		10		10		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	7		10		10		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27		32		37		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64		77		89		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39		47		54		ns	17

(2/2)

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	7		10		12		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7		10		12		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		64		64		64	ms	

HYPER PAGE MODE

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20		25		30		ns	
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7		10		10		ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41		52		59		ns	17
Read Modify Write Cycle Time	t_{HPRWC}	52		66		75		ns	
Data Output Hold Time	t_{DHC}	5		5		5		ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	t_{WPZ}	7		10		10		ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	12, 18

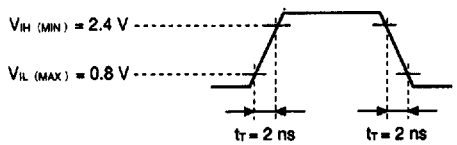
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.

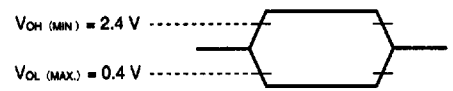
Notes 8. AC measurements assume t_T = 2 ns.

9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD (MAX.)}$ and $t_{RCD} \leqq t_{RCD (MAX.)}$	$t_{RAC (MAX.)}$	$t_{RAC (MAX.)}$
$t_{RAD} > t_{RAD (MAX.)}$ and $t_{RCD} \leqq t_{RCD (MAX.)}$	$t_{AA (MAX.)}$	$t_{RAD} + t_{AA (MAX.)}$
$t_{RCD} > t_{RCD (MAX.)}$	$t_{CAC (MAX.)}$	$t_{RCD} + t_{CAC (MAX.)}$

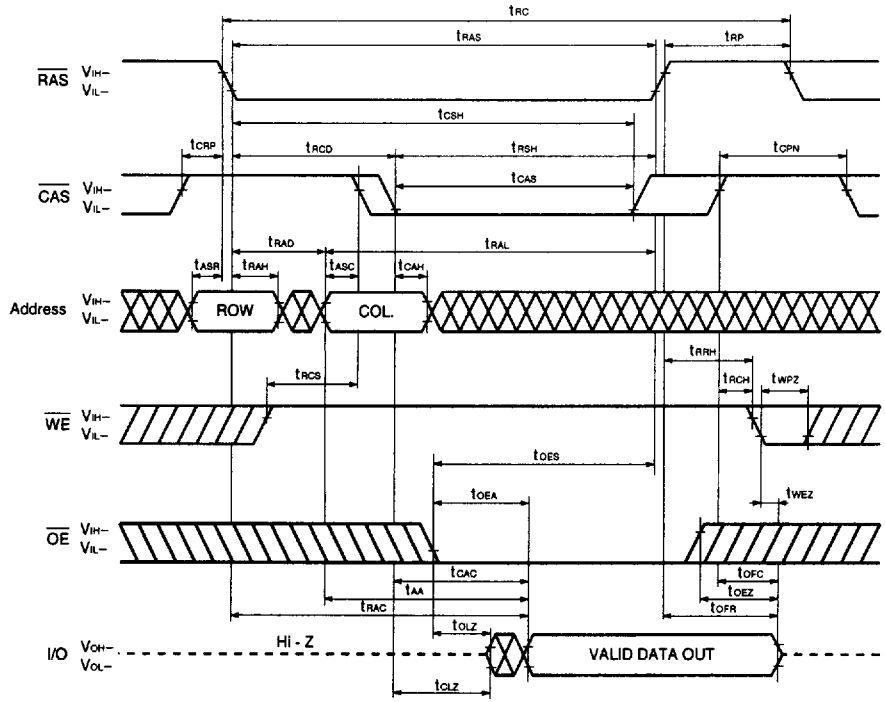
$t_{RAD (MAX.)}$ and $t_{RCD (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD (MAX.)}$ and $t_{RCD} \geqq t_{RCD (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFC (MAX.)}$, $t_{OFR (MAX.)}$, $t_{WEZ (MAX.)}$, and $t_{OEZ (MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
13. $t_{CRP (MIN.)}$ requirement is applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycles.
14. Either $t_{RCH (MIN.)}$ or $t_{RRH (MIN.)}$ should be met in read cycles.
15. $t_{WP (MIN.)}$ is applied for late write cycles or read modify write cycles. In early write cycles, $t_{WCH (MIN.)}$ should be met.
16. $t_{DS (MIN.)}$ and $t_{DH (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geqq t_{WCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD (MIN.)}$, $t_{CWD} \geqq t_{CWD (MIN.)}$, $t_{AWD} \geqq t_{AWD (MIN.)}$ and $t_{CPWD} \geqq t_{CPWD (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

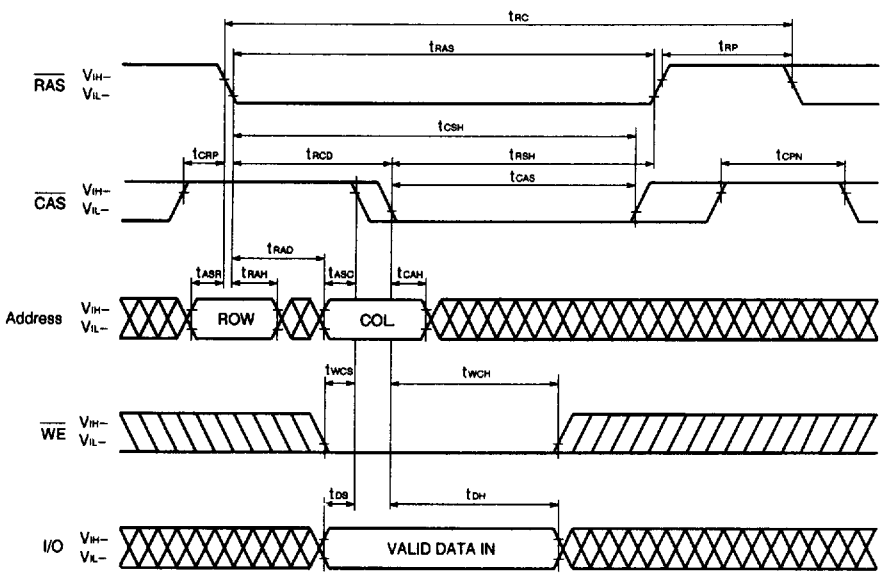
(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active···t_{WEZ}, t_{WPZ} are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive···t_{OEZ} is effective.

READ CYCLE

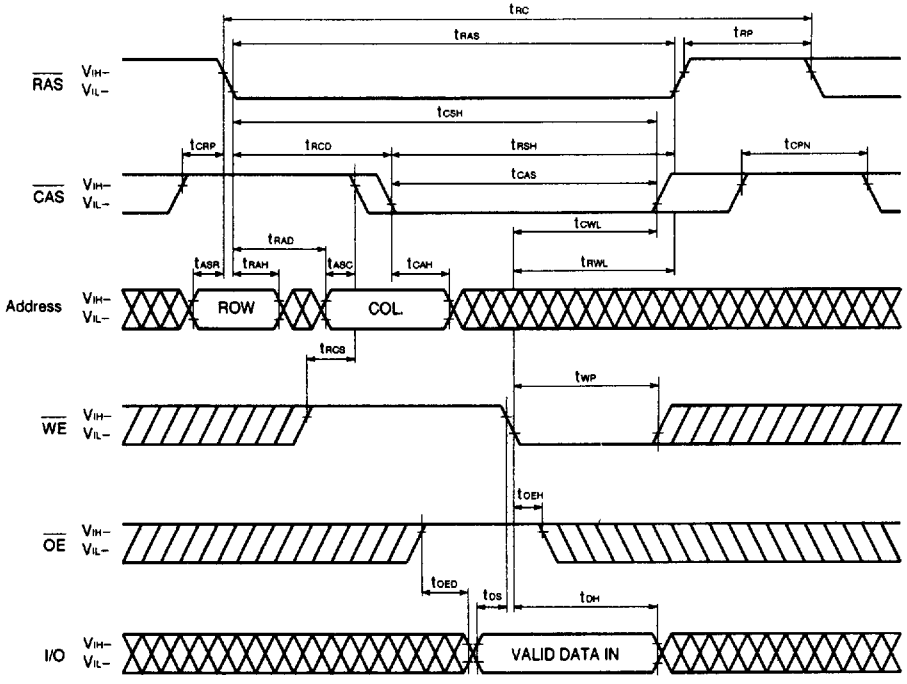


EARLY WRITE CYCLE

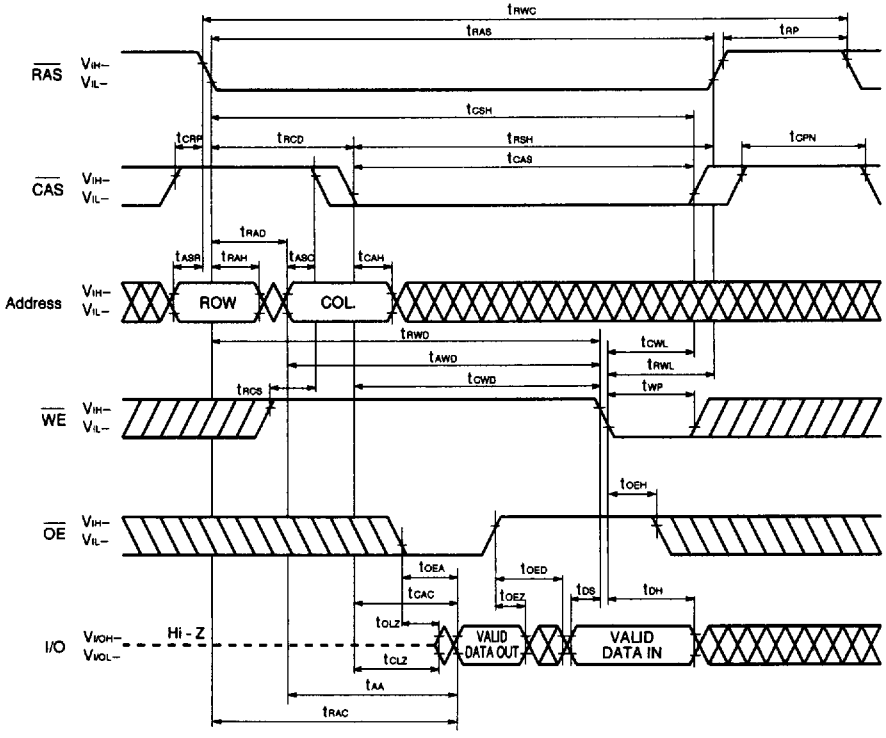


Remark $\overline{OE}$ = Don't Care

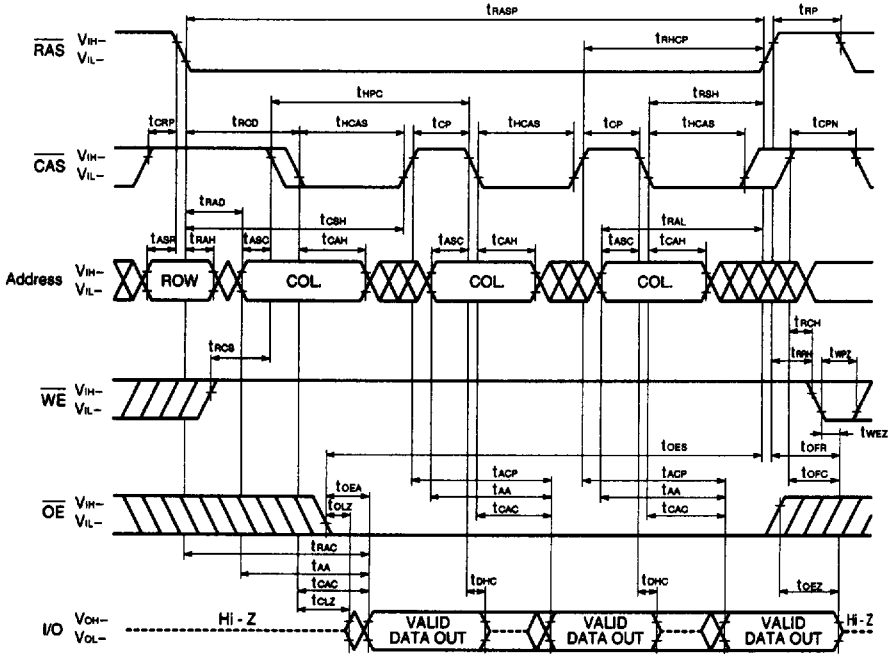
LATE WRITE CYCLE



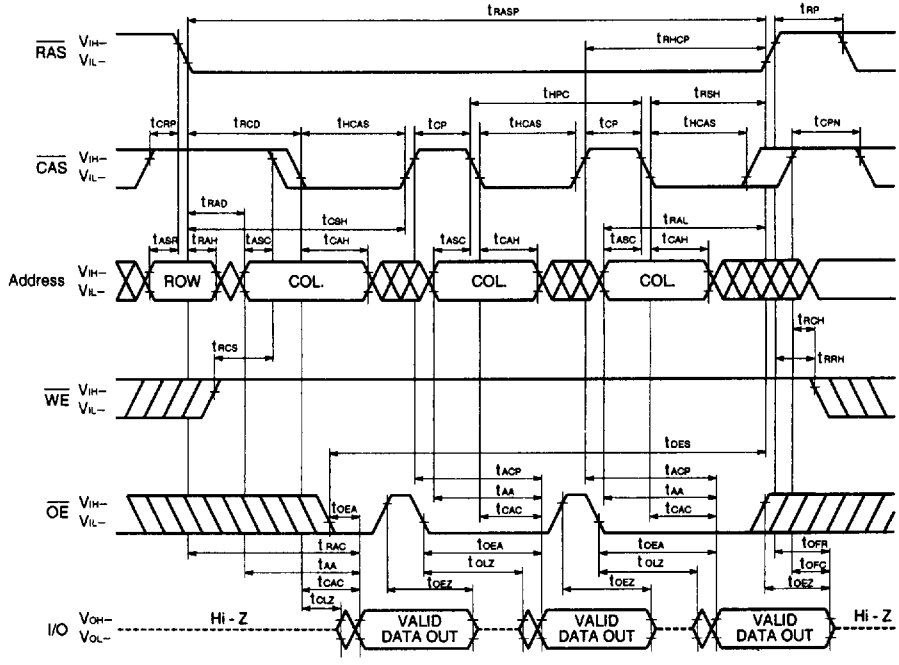
READ MODIFY WRITE CYCLE



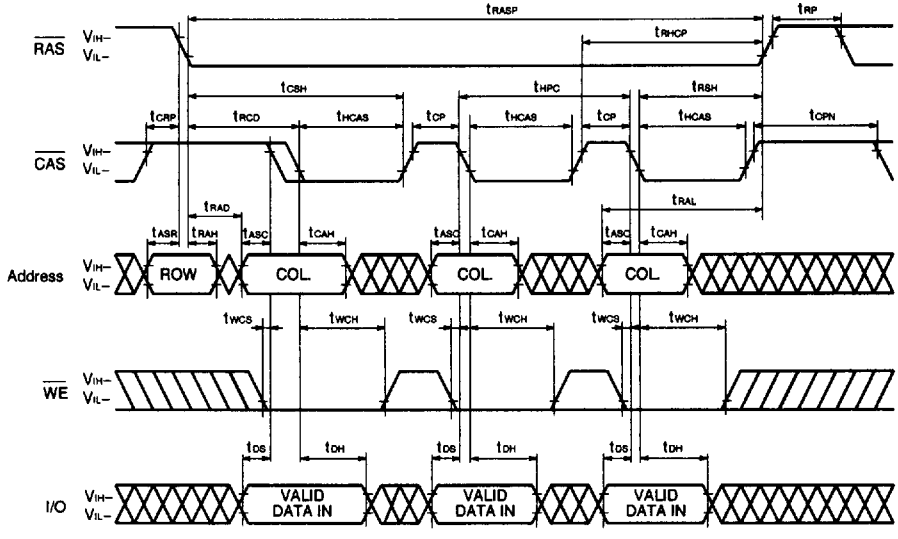
HYPER PAGE MODE READ CYCLE



HYPER PAGE MODE READ CYCLE ($\overline{OE}$ CONTROL)

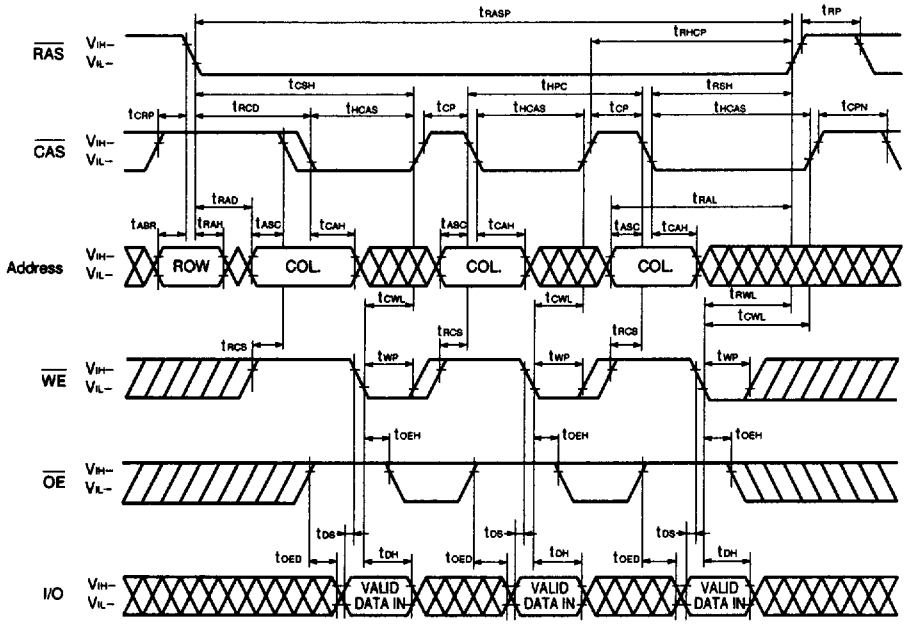


HYPER PAGE MODE EARLY WRITE CYCLE

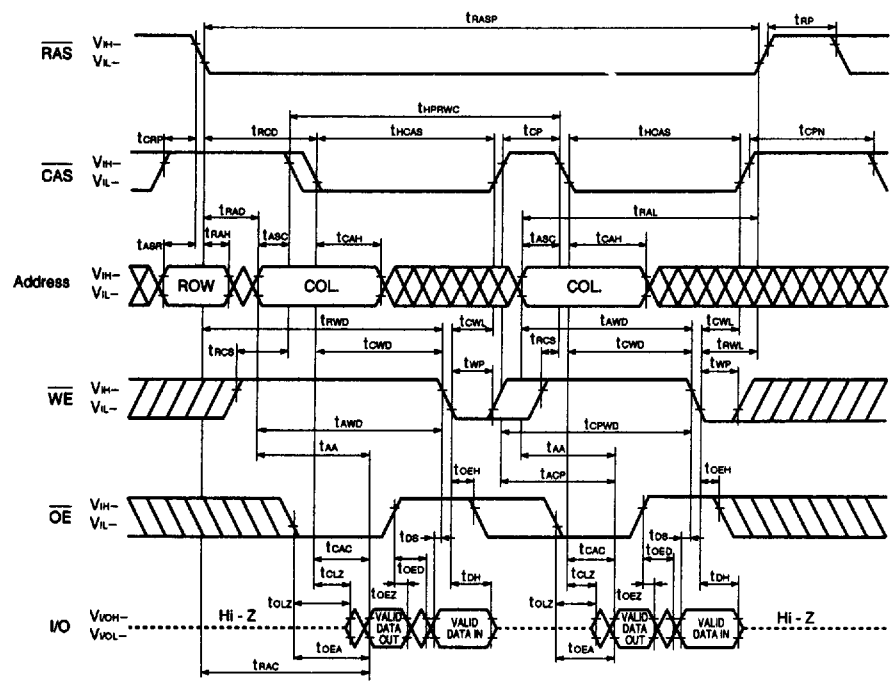


Remark $\overline{OE}$ = Don't Care

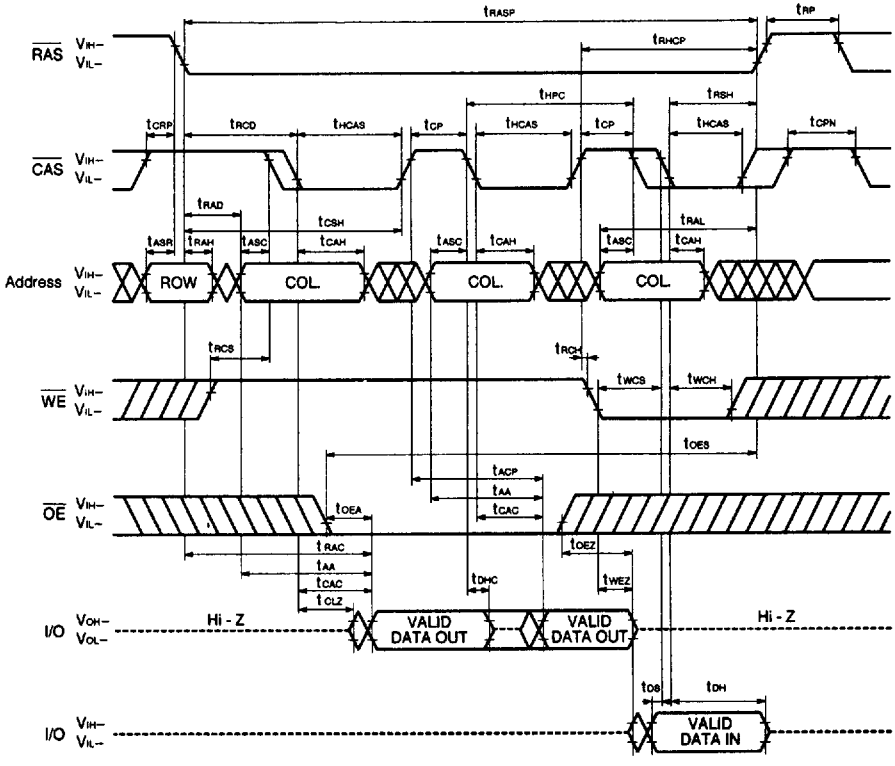
HYPER PAGE MODE LATE WRITE CYCLE



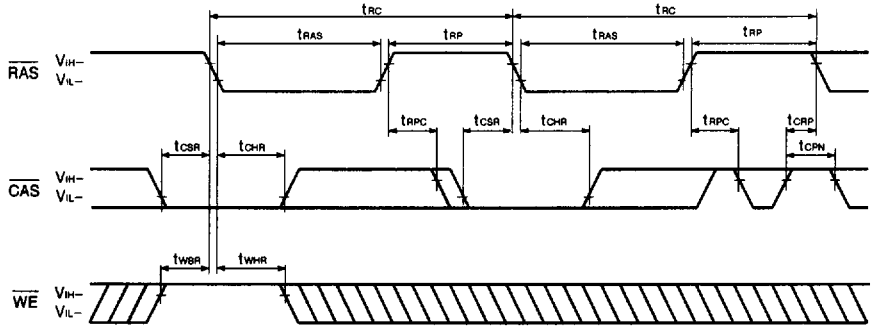
HYPER PAGE MODE READ MODIFY WRITE CYCLE



HYPER PAGE MODE READ AND WRITE CYCLE

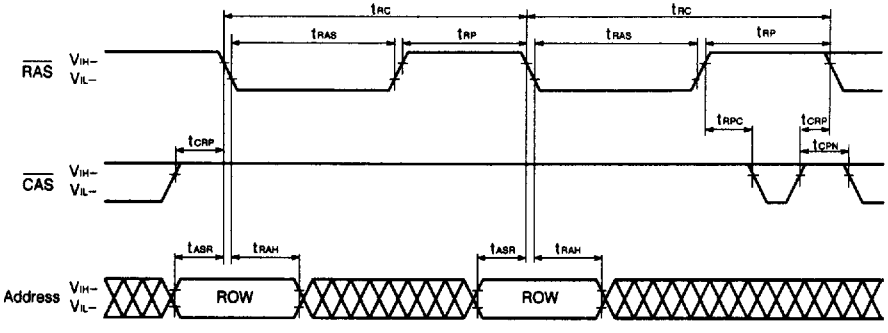


$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



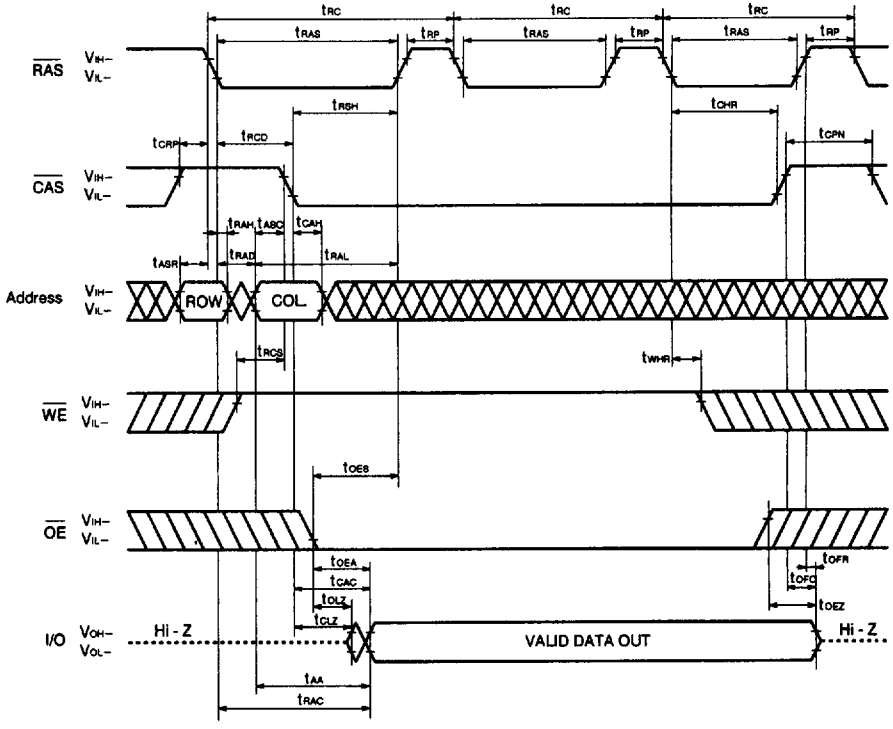
Remark Address, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

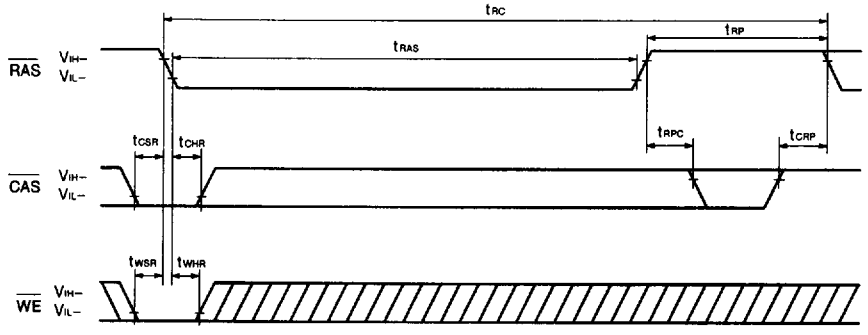


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O = Hi - Z

HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, $\overline{OE}$ = Don't care I/O = HI - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the column address input A0.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O8 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O8 to check written data. In case of writing each 2 bits rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

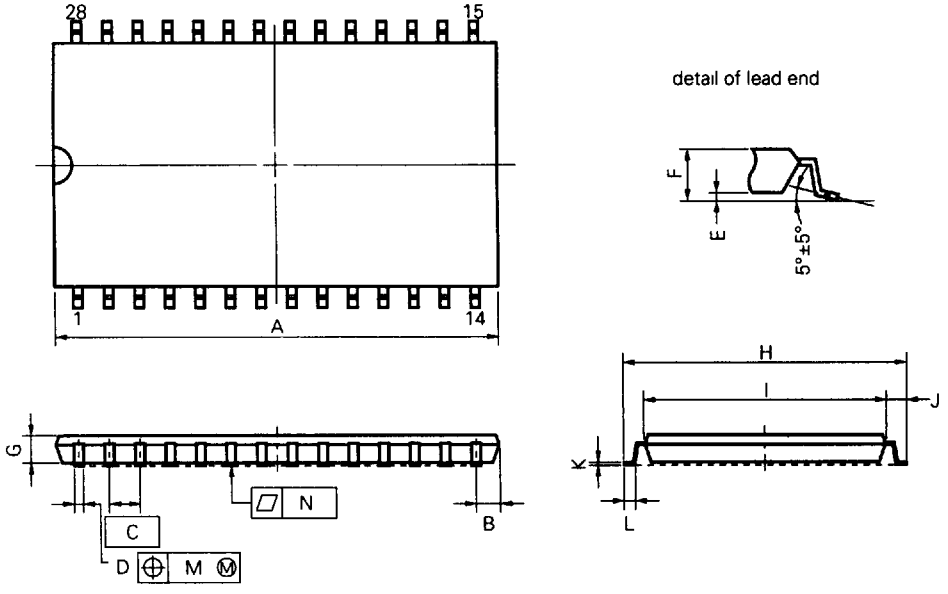
Use normal read cycle or $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

28 PIN PLASTIC TSOP(II) (400 mil)



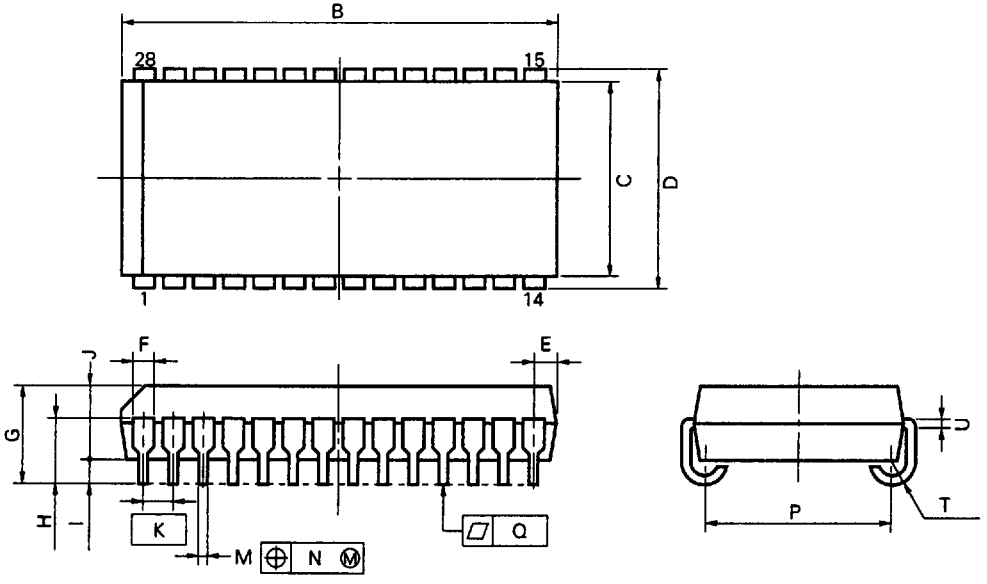
S28G5-50-7JD2-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	$0.016^{+0.004}_{-0.005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD4216805.

TYPE OF SURFACE MOUNT DEVICE

μPD4216805G5 : 28-pin Plastic TSOP(II) (400 mil)
μPD4216805LE : 28-pin Plastic SOJ (400 mil)