PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT
μPD703201, 703201Y, 703204, 703204Y, 70F3201, 70F3201Y, 70F3204, 70F3204Y

V850ES/SA2™, V850ES/SA3™
32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD703201, 703201Y, 70F3201, and 70F3201Y (V850ES/SA2), μPD703204, 703204Y, 70F3204, and 70F3204Y (V850ES/SA3) are products in the V850 Family™ of 32-bit single-chip microcontrollers, and include peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a D/A converter, and a DMA controller.

In addition to their high real-time responsiveness and one-clock-pitch execution of instructions, the V850ES/SA2 and V850ES/SA3 include instructions suited to digital servo control applications such as multiplication instructions executed via a hardware multiplier, saturation instructions, and bit manipulation instructions. As a real-time control system, this device provides a high-level cost performance ideal for ultra-low-power DVC and portable audio applications.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850ES/SA2, V850ES/SA3 User's Manual Hardware: To be prepared
V850ES User's Manual Architecture: To be prepared

FEATURES

- Number of instructions: 83
- Minimum instruction execution time:
  59 ns (@ 17 MHz operation with main system clock (fxx))
  74 ns (@ 13.5 MHz operation with main system clock (fxx))
- General-purpose registers: 32 bits × 32 registers
- Instruction set:
  Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space:
  64 MB linear address space
  Memory block division function:
  2 MB, 2 MB, 4 MB, 8 MB = Total four blocks
- External bus interface: 16-bit data bus
  Address bus: Separate output enabled
- Internal memory
  Mask ROM: 256 KB (μPD703201, 703201Y, 703204, 703204Y)
  Flash memory: 256 KB (μPD70F3201, 70F3201Y, 70F3204, 70F3204Y)
  RAM: 16 KB
- Interrupts and exceptions
  Non-maskable interrupts: 2 sources
  Maskable interrupts:
  38 sources (μPD703201, 70F3201)
  39 sources (μPD703201Y, 70F3201Y)
  39 sources (μPD703204, 70F3204)
  40 sources (μPD703204Y, 70F3204Y)
  Software exceptions: 32 sources
  Exception trap: 1 source
- I/O lines Total: 82 (V850ES/SA2)
  102 (V850ES/SA3)
- Timer/counters
  16-bit timer: 2 channels
  8-bit timer: 4 channels
- Real-time counter (for watch): 1 channel
- Watchdog timer: 1 channel

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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Date Published June 2001 N CP(K)
Printed in Japan

- Serial interface (SIO)
  - Asynchronous serial interface (UART): 2 channels
  - Clocked serial interface (CSI):
    - 4 channels (V850ES/SA2),
    - 5 channels (V850ES/SA3)
  - I^2C bus interface: 1 channel
  - (μPD703201Y, 703204Y, 70F3201Y, 70F3204Y)
- A/D converter:
  - 10-bit resolution × 12 channels (V850ES/SA2)
  - 10-bit resolution × 16 channels (V850ES/SA3)
- D/A converter: 8-bit resolution × 2 channels
- DMA controller: 4 channels
- Power save functions: HALT/IDLE/STOP/Backup modes
- ROM correction: Four points can be corrected
- Packages: 100-pin plastic LQFP (14 × 14) (V850ES/SA2)
  - 121-pin plastic FBGA (12 × 12) (V850ES/SA3)

APPLICATIONS

- Low-power portable devices
  - DVCs, portable audios

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD703201GC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB (mask ROM)
μPD703201YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB (mask ROM)
μPD703204F1-×××-EA6	121-pin plastic FBGA (12 × 12)	256 KB (mask ROM)
μPD703204YF1-×××-EA6	121-pin plastic FBGA (12 × 12)	256 KB (mask ROM)
μPD70F3201GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB (flash memory)
μPD70F3201YGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB (flash memory)
μPD70F3204F1-EA6	121-pin plastic FBGA (12 × 12)	256 KB (flash memory)
μPD70F3204YF1-EA6	121-pin plastic FBGA (12 × 12)	256 KB (flash memory)

Remark ××× indicates ROM code suffix.

PIN CONFIGURATION

- **V850ES/SA2**

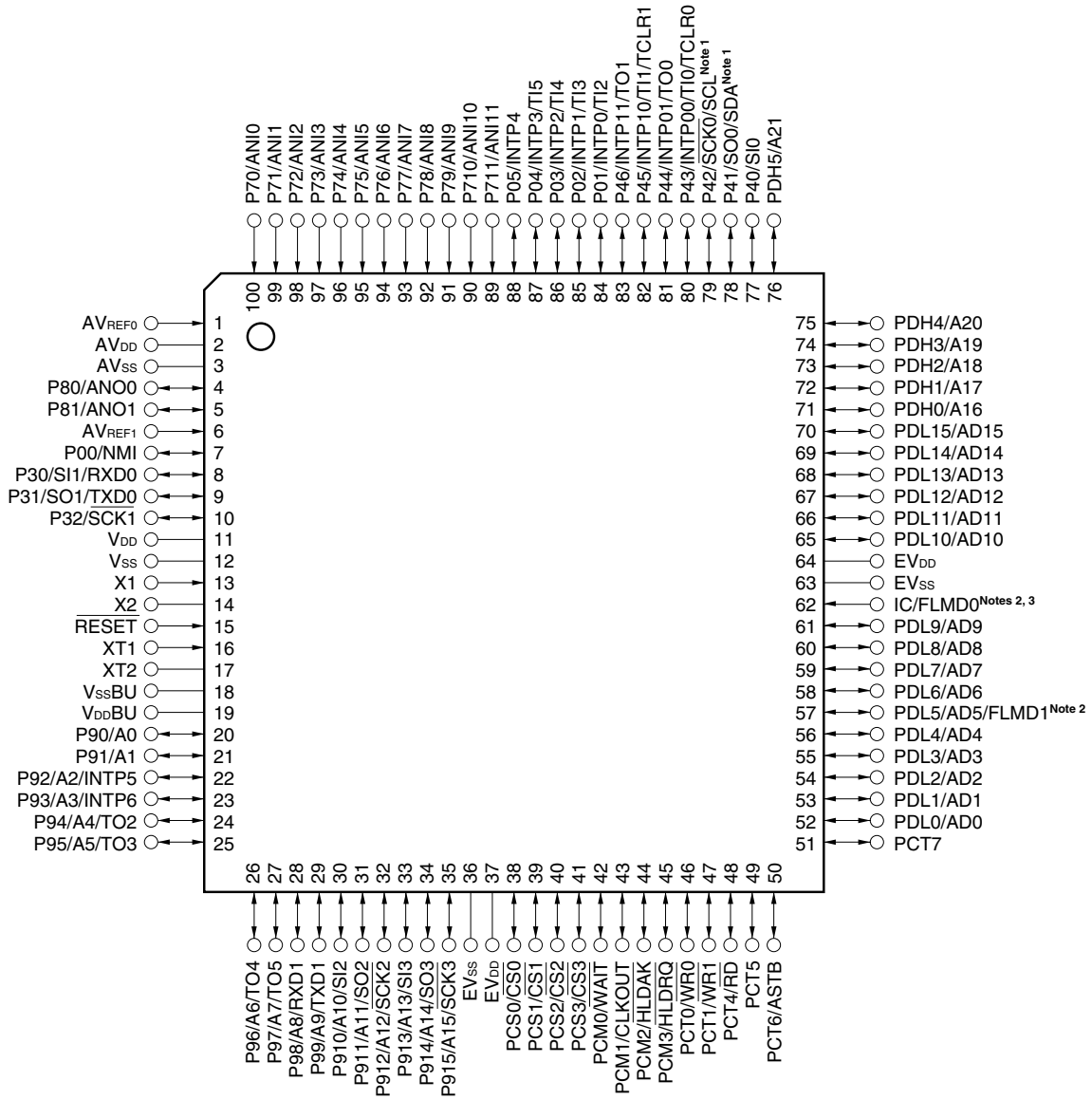
  100-pin plastic LQFP (fine-pitch) (14 × 14)

  μPD703201GC-×××-8EU

  μPD703201YGC-×××-8EU

  μPD70F3201GC-8EU

  μPD70F3201YGC-8EU



Notes 1. SCL and SDA are valid only for the μPD703201Y and 70F3201Y.

2. FLMD0 and FLMD1 are valid only for the μPD70F3201 and 70F3201Y.

3. IC: Connect directly to VSS (μPD703201, 703201Y).

FLMD0: Connect to VSS in normal mode (μPD70F3201, 70F3201Y).

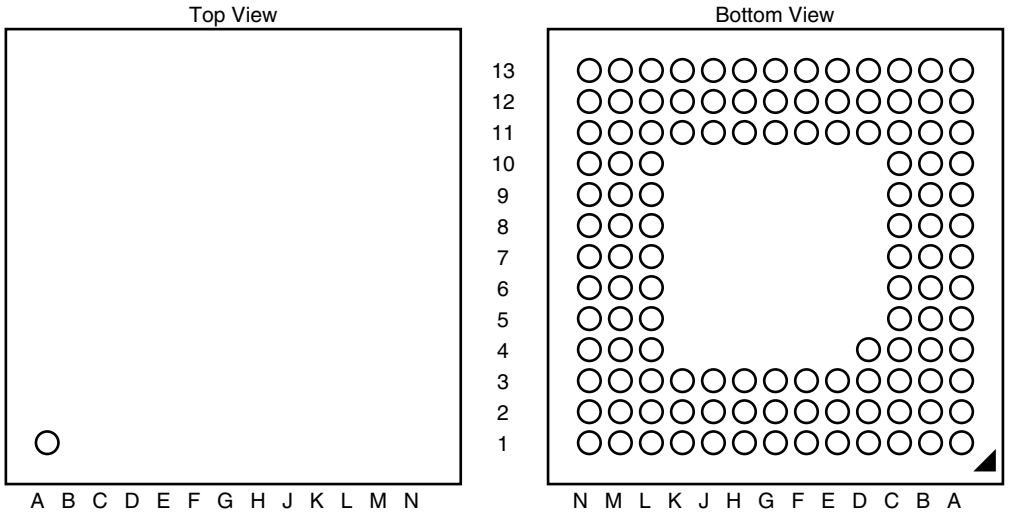
- **V850ES/SA3**

  121-pin plastic FBGA (12 × 12)

  μPD703204F1-×××-EA6 μPD70F3204F1-EA6

  μPD703204YF1-×××-EA6 μPD70F3204YF1-EA6

(1/2)



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	P70/ANI0	B8	PCD3	D2	AV_{REF1}
A2	P71/ANI1	B9	P02/INTP1/TI3	D3	P00/NMI
A3	P73/ANI3	B10	P46/INTP11/TO1	D11	PDH0/A16
A4	P713/ANI13	B11	P42/$\overline{SCK0}$/SCL[Note]	D12	PDH2/A18
A5	P76/ANI6	B12	P40/SI0	D13	PDH1/A17
A6	P78/ANI8	B13	PDH4/A20	E1	P30/SI1/RXD0
A7	P711/ANI11	C1	P80/ANO0	E2	P31/SO1/TXD0
A8	P04/INTP3/TI5	C2	AV_{SS}	E3	P32/$\overline{SCK1}$
A9	PCD2	C3	P74/ANI4	E11	PDL14/AD14
A10	P45/INTP10/TI1/TCLR1	C4	P714/ANI14	E12	PDH6/A22
A11	P43/INTP00/TI0/TCLR0	C5	P715/ANI15	E13	PDL15/AD15
A12	P41/SO0/SDA[Note]	C6	P79/ANI9	F1	V_{SS}
A13	PDH5/A21	C7	P05/INTP4	F2	X1
B1	AV_{DD}	C8	P03/INTP2/TI4	F3	V_{DD}
B2	AV_{REF0}	C9	PCD1	F11	PDL11/AD11
B3	P72/ANI2	C10	P01/INTP0/TI2	F12	PDL13/AD13
B4	P712/ANI12	C11	P44/INTP01/TO0	F13	PDL12/AD12
B5	P75/ANI5	C12	PDH3/A19	G1	$\overline{RESET}$
B6	P77/ANI7	C13	PDH7/A23	G2	XT1
B7	P710/ANI10	D1	P81/ANO1	G3	X2

Note SCL and SDA are valid only for μPD703204Y and 70F3204Y.

Remark Connect the D4 pin directly to V_{SS}.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
G11	EV_{SS}	K13	PDL3/AD3	M7	PCS4
G12	PDL10/AD10	L1	P93/A3/INTP6	M8	PCM0/$\overline{WAIT}$
G13	EV_{DD}	L2	P94/A4/TO2	M9	PCM2/$\overline{HLDAK}$
H1	V_{SS}BU	L3	P911/A11/SO2	M10	PCT3
H2	V_{DD}BU	L4	P914/A14/SO3	M11	PCT4/$\overline{RD}$
H3	XT2	L5	P915/A15/$\overline{SCK3}$	M12	PCT7
H11	PDL8/AD8	L6	EV_{DD}	M13	PDL0/AD0
H12	IC/FLMD0[Notes 1, 2]	L7	PCS0/$\overline{CS0}$	N1	P96/A6/TO4
H13	PDL9/AD9	L8	PCS2/$\overline{CS2}$	N2	P98/A8/RXD1
J1	P20/SI4	L9	PCM4	N3	P910/A10/SI2
J2	P91/A1	L10	PCT2	N4	P912/A12/$\overline{SCK2}$
J3	P90/A0	L11	PCT0/$\overline{WR0}$	N5	PCS7
J11	PDL5/AD5/FLMD1[Note 1]	L12	PDL1/AD1	N6	PCS6
J12	PDL7/AD7	L13	PDL2/AD2	N7	PCS1/$\overline{CS1}$
J13	PDL6/AD6	M1	P95/A5/TO3	N8	PCS3/$\overline{CS3}$
K1	P22/$\overline{SCK4}$	M2	P97/A7/TO5	N9	PCM5
K2	P92/A2/INTP5	M3	P99/A9/TXD1	N10	PCM3/$\overline{HLDRQ}$
K3	P21/SO4	M4	P913/A13/SI3	N11	PCT1/$\overline{WR1}$
K11	PCM1/CLKOUT	M5	EV_{SS}	N12	PCT5
K12	PDL4/AD4	M6	PCS5	N13	PCT6/ASTB

Notes 1. FLMD0 and FLMD1 are valid only for μPD70F3204Y and 70F3204Y.

2. IC: Connect directly to V_{SS} (μPD703204, 703204Y).

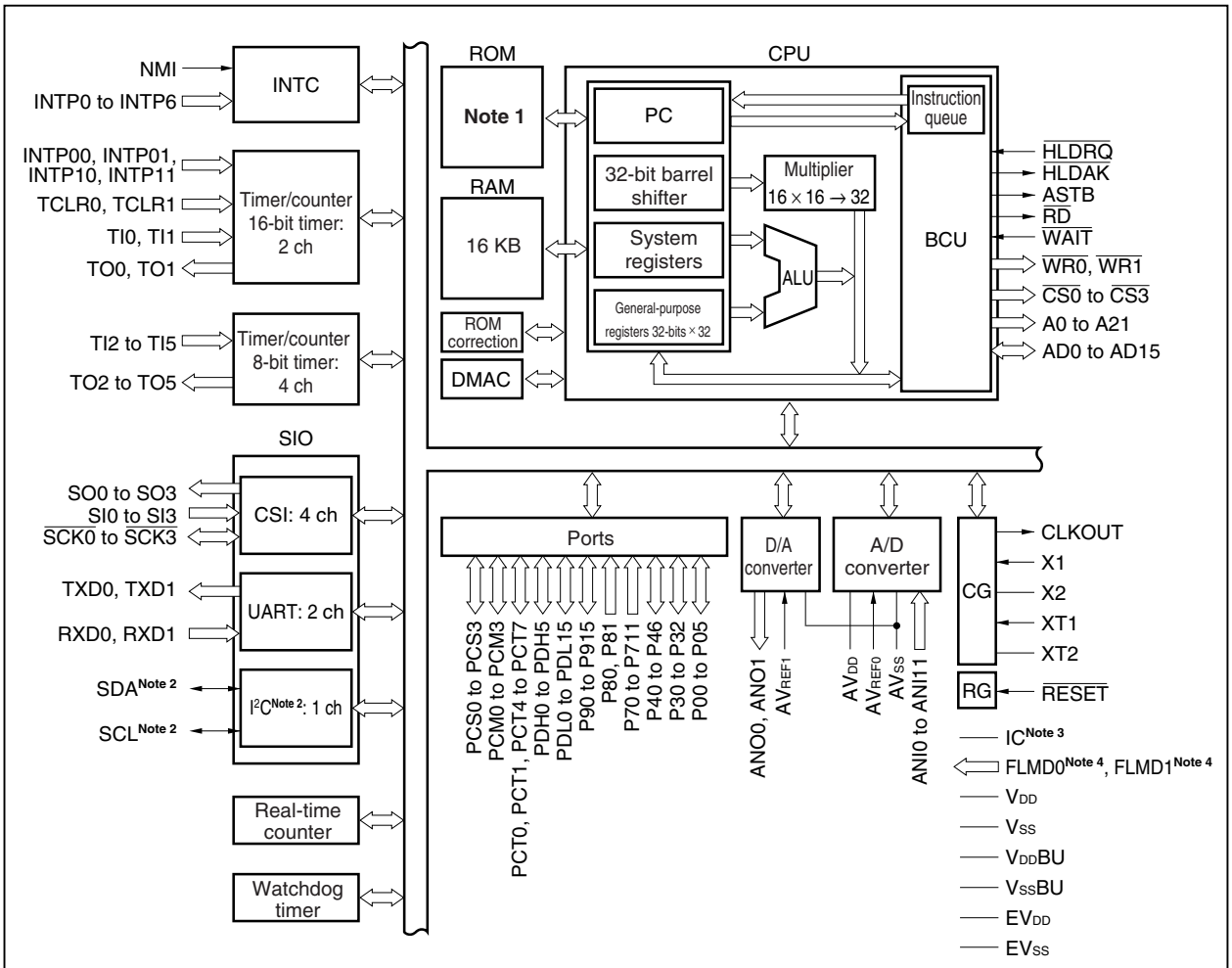
FLMD0: Connect to V_{SS} in normal mode (μPD70F3204, 70F3204Y).

PIN IDENTIFICATION

A0 to A23: Address bus
AD0 to AD15: Address/data bus
ADTRG: AD trigger input
ANI0 to ANI15: Analog input
ANO0, ANO1: Analog output
ASTB: Address strobe
AV_{DD}: Analog V_{DD}
AV_{REF0}, AV_{REF1}: Analog reference voltage
AV_{SS}: Analog V_{SS}
CLKOUT: Clock output
$\overline{CS0}$ to $\overline{CS3}$: Chip select
EV_{DD}: Power supply for port
EV_{SS}: Ground for port
FLMD0, FLMD1: Flash programming mode
$\overline{HLDAK}$: Hold acknowledge
$\overline{HLDRQ}$: Hold request
IC: Internally connected
INTP0 to INTP6: Interrupt request from peripherals
INTP00, INTP01,: Interrupt request to timer
INTP10, INTP11
NMI: Non-maskable interrupt request
P00 to P05: Port 0
P20 to P22: Port 2
P30 to P32: Port 3
P40 to P46: Port 4
P70 to P715: Port 7
P80, P81: Port 8
P90 to P915: Port 9
PCD1 to PCD3: Port CD
PCM0 to PCM5: Port CM
PCS0 to PCS7: Port CS
PCT0 to PCT7: Port CT
PDH0 to PDH7: Port DH
PDL0 to PDL15: Port DL
$\overline{RD}$: Read
$\overline{RESET}$: Reset
RXD0, RXD1: Receive data
$\overline{SCK0}$ to $\overline{SCK4}$: Serial clock
SCL: Serial clock
SDA: Serial data
SI0 to SI4: Serial input
SO0 to SO4: Serial output
TCLR0, TCLR1: Timer clear input
TI0 to TI5: Timer input
TO0 to TO5: Timer output
TXD0, TXD1: Transmit data
V_{DD}: Power supply
$V_{DD}BU$: Power supply for backup
V_{SS}: Ground
$V_{SS}BU$: Ground for backup
$\overline{WAIT}$: Wait
$\overline{WR0}$: Write strobe low level data
$\overline{WR1}$: Write strobe high level data
X1, X2: Crystal for main clock
XT1, XT2: Crystal for subclock

INTERNAL BLOCK DIAGRAM

- **V850ES/SA2**



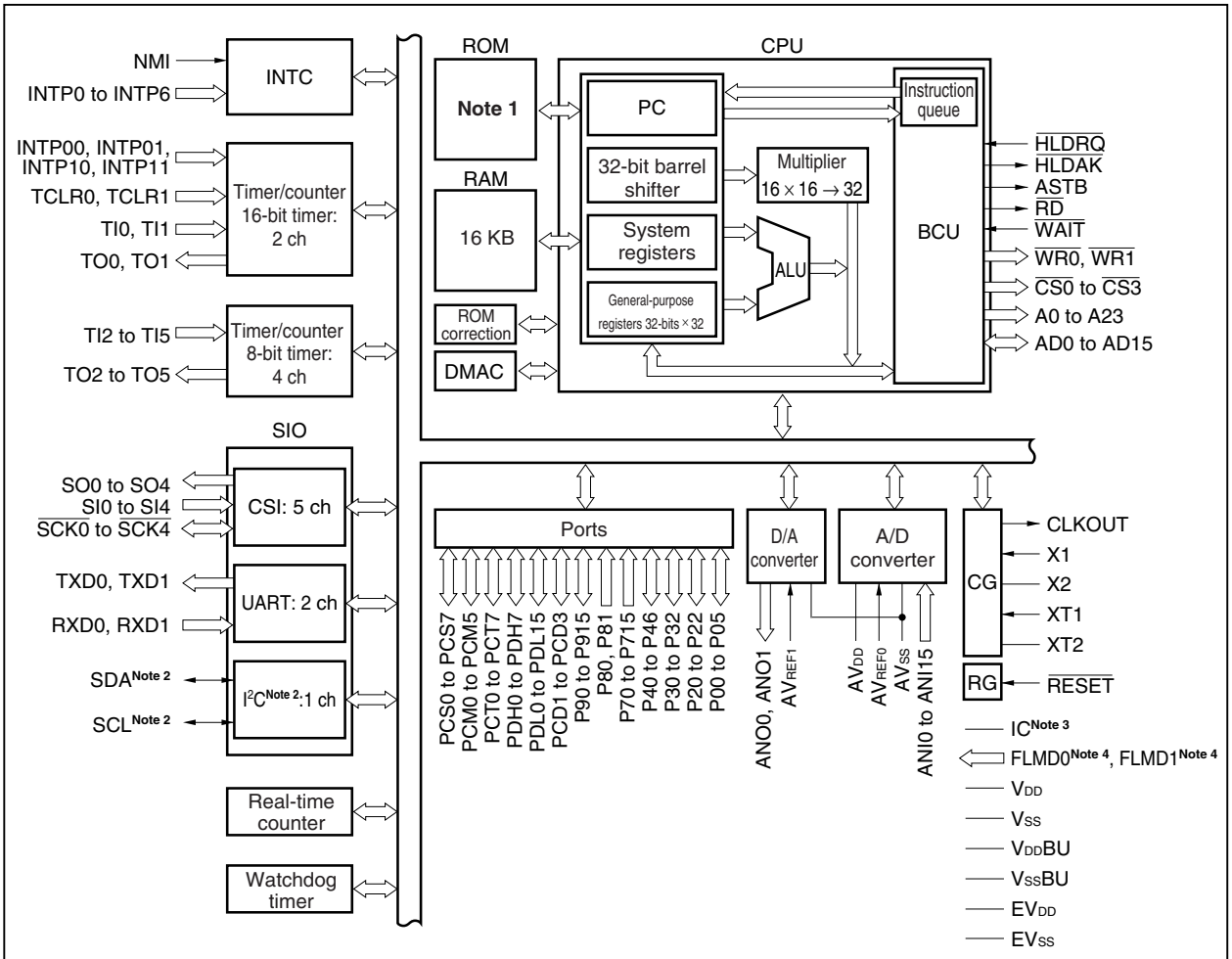
Notes 1. μPD703201, 703201Y: 256 KB (mask ROM)
μPD70F3201, 70F3201Y: 256 KB (flash memory)

2. Applies to the μPD703201Y and 70F3201Y only.

3. Applies to the μPD703201 and 703201Y only.

4. Applies to the μPD70F3201 and 70F3201Y only.

- **V850ES/SA3**



Notes 1. μPD703204, 703204Y: 256 KB (mask ROM)
μPD70F3204, 70F3204Y: 256 KB (flash memory)

2. Applies to the μPD703204Y and 70F3204Y only.

3. Applies to the μPD703204 and 703204Y only.

4. Applies to the μPD70F3204 and 70F3204Y only.

CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 6-bit I/O port Input/output can be specified in 1-bit units.	NMI
P01				INTP0/TI2
P02				INTP1/TI3
P03				INTP2/TI4
P04				INTP3/TI5
P05				INTP4
[P20]	I/O	Yes	Port 2 3-bit I/O port Input/output can be specified in 1-bit units. N-ch open drain can be specified in 1-bit units (P21, P22 only).	[SI4]
[P21]				[SO4]
[P22]				[$\overline{\text{SCK4}}$]
P30	I/O	Yes	Port 3 3-bit I/O port Input/output can be specified in 1-bit units. N-ch open drain can be specified in 1-bit units (P31, P32 only).	SI1/RXD0
P31				SO1/TXD0
P32				$\overline{\text{SCK1}}$
P40	I/O	Yes	Port 4 7-bit I/O port Input/output can be specified in 1-bit units. N-ch open drain can be specified in 1-bit units (P41, P42 only).	SI0
P41				SO0/SDA[Note]
P42				$\overline{\text{SCK0}}$/SCL[Note]
P43				INTP00/TI0/TCLR0
P44				INTP01/TO0
P45				INTP10/TI1/TCLR1
P46				INTP11/TO1
P70	Input	No	Port 7 12-bit input port (V850ES/SA2) 16-bit input port (V850ES/SA3)	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P78				ANI8
P79				ANI9
P710				ANI10
P711				ANI11
[P712]				[ANI12]
[P713]				[ANI13]
[P714]				[ANI14]
[P715]				[ANI15]

Note Applies to the μPD703201Y, 703204Y, 70F3201Y, and 70F3204Y only.

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

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Pin Name	I/O	PULL	Function	Alternate Function
P80	Input	No	Port 8 2-bit input port	ANO0
P81				ANO1
P90	I/O	Yes	Port 9 16-bit I/O port Input/output can be specified in 1-bit units. N-ch open drain can be specified in 1-bit units (P911, P912, P914, P915 only).	A0
P91				A1
P92				A2/INTP5
P93				A3/INTP6
P94				A4/TO2
P95				A5/TO3
P96				A6/TO4
P97				A7/TO5
P98				A8/RXD1
P99				A9/TXD1
P910				A10/SI2
P911				A11/SO2
P912				A12/$\overline{\text{SCK2}}$
P913				A13/SI3
P914				A14/SO3
P915				A15/$\overline{\text{SCK3}}$
[PCD1]	I/O	No	Port CD 3-bit I/O port Input/output can be specified in 1-bit units.	–
[PCD2]				–
[PCD3]				–
PCM0	I/O	No	4-bit I/O port (V850ES/SA2) 6-bit I/O port (V850ES/SA3) Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1				CLKOUT
PCM2				$\overline{\text{HLDAK}}$
PCM3				$\overline{\text{HLDRQ}}$
[PCM4]				–
[PCM5]				–
PCS0	I/O	No	Port 10 4-bit I/O port (V850ES/SA2) 8-bit I/O port (V850ES/SA3) Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$
PCS1				$\overline{\text{CS1}}$
PCS2				$\overline{\text{CS2}}$
PCS3				$\overline{\text{CS3}}$
[PCS4]				–
[PCS5]				–
[PCS6]				–
[PCS7]				–

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

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Pin Name	I/O	PULL	Function	Alternate Function
PCT0	I/O	No	Port CT 6-bit I/O port (V850ES/SA2) 8-bit I/O port (V850ES/SA3) Input/output can be specified in 1-bit units.	$\overline{WR0}$
PCT1				$\overline{WR1}$
[PCT2]				–
[PCT3]				–
PCT4				$\overline{RD}$
PCT5				–
PCT6				ASTB
PCT7				–
PDH0	I/O	No	Port DH 6-bit I/O port (V850ES/SA2) 8-bit I/O port (V850ES/SA3) Input/output can be specified in 1-bit units.	A16
PDH1				A17
PDH2				A18
PDH3				A19
PDH4				A20
PDH5				A21
[PDH6]				[A22]
[PDH7]				[A23]
PDL0	I/O	No	Port DL 16-bit I/O port Input/output can be specified in 1-bit units.	AD0
PDL1				AD1
PDL2				AD2
PDL3				AD3
PDL4				AD4
PDL5				AD5/FLMD1[Note]
PDL6				AD6
PDL7				AD7
PDL8				AD8
PDL9				AD9
PDL10				AD10
PDL11				AD11
PDL12				AD12
PDL13				AD13
PDL14				AD14
PDL15				AD15

Note Applies to the μPD70F3201, 70F3201Y, 70F3204, and 70F3204Y only.

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

1.2 Non-Port Pins

(1/4)

Pin Name	I/O	PULL	Function	Alternate Function
A0	Output	Yes	Address bus for external memory (when using separate bus)	P90
A1				P91
A2				P92/INTP5
A3				P93/INTP6
A4				P94/TO2
A5				P95/TO3
A6				P96/TO4
A7				P97/TO5
A8				P98/RXD1
A9				P99/TXD1
A10				P910/SI2
A11				P911/SO2
A12				P912/$\overline{\text{SCK2}}$
A13				P913/SI3
A14				P914/SO3
A15				P915/$\overline{\text{SCK3}}$
A16 to A21, [A22, A23]	Output	No	Address bus for external memory	PDH0 to PDH5, [PDH6, PDH7]
AD0 to AD4	I/O	No	Address/data bus for external memory	PDL0 to PDL4
AD5				PDL5/FLMD1[Note]
AD6 to AD15				PDL6 to PDL15
ANI0	Input	No	Analog voltage input for A/D converter	P70
ANI1				P71
ANI2				P72
ANI3				P73
ANI4				P74
ANI5				P75
ANI6				P76
ANI7				P77
ANI8				P78
ANI9				P79
ANI10				P710
ANI11				P711
[ANI12]				[P712]
[ANI13]				[P713]
[ANI14]				[P714]
[ANI15]				[P715]

Note Applies to the μPD70F3201, 70F3201Y, 70F3204, and 70F3204Y only.

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

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Pin Name	I/O	PULL	Function	Alternate Function
ANO0	Output	No	Analog voltage output for D/A converter	P80
ANO1				P81
ASTB	Output	No	Address strobe signal output for external memory	PCT6
AV_{DD}	–	–	Positive power supply for A/D converter (same potential as V_{DD})	–
AV_{REF0}	Input	–	Reference voltage input for A/D converter	–
AV_{REF1}			Reference voltage input for D/A converter	–
AV_{SS}	–	–	Ground potential for A/D, D/A converters (same potential as V_{SS})	–
CLKOUT	Output	No	Internal system clock output	PCM1
$\overline{CS0}$ to $\overline{CS3}$	Output	No	Chip select output	PCS0 to PCS3
EV_{DD}	–	–	Positive power supply for external devices (same potential as V_{DD})	–
EV_{SS}	–	–	Ground potential for external devices (same potential as V_{SS})	–
FLMD0[Note 1]	Input	No	Flash programming mode lead-in pins	–
FLMD1[Note 1]				PDL5/AD5
$\overline{HLDAK}$	Output	No	Bus hold acknowledge output	PCM2
$\overline{HLDRQ}$	Input	No	Bus hold request input	PCM3
IC	–	–	Internally connected (directly connect to V_{SS}). (μPD703201, 703201Y, 703204, and 703204Y only)	–
INTP0 to INTP3	Input	Yes	External interrupt request input (maskable, analog noise elimination)	P01/TI2 to P04/TI5
INTP4				P05
INTP5				P92/A2
INTP6				P93/A3
INTP00	Input	Yes	Capture trigger input (TM0)	P43/TI0/TCLR0
INTP01				P44/TO0
INTP10			Capture trigger input (TM1)	P45/TI1/TCLR1
INTP11				P46/TO1
NMI	Input	Yes	External interrupt input (non-maskable, analog noise elimination)	P00
$\overline{RD}$	Output	No	Read strobe signal output for external memory	PCT4
$\overline{RESET}$	Input	–	System reset input	–
RXD0	Input	Yes	Serial receive data input (UART0)	P30/SI1
RXD1			Serial receive data input (UART1)	P98/A8
$\overline{SCK0}$	I/O	Yes	Serial clock I/O (CSI0)	P42/SCL[Note 2]
$\overline{SCK1}$			Serial clock I/O (CSI1)	P32
$\overline{SCK2}$			Serial clock I/O (CSI2)	P912/A12
$\overline{SCK3}$			Serial clock I/O (CSI3)	P915/A15
[$\overline{SCK4}$]			Serial clock I/O (CSI4)	[P22]
SCL[Note 2]	I/O	Yes	Serial clock I/O (I^2C)	P42/$\overline{SCK0}$
SDA[Note 2]	I/O	Yes	Serial transmit/receive data I/O (I^2C)	P41/SO0

Notes 1. Applies to the μPD70F3201, 70F3201Y, 70F3204, and 70F3204Y only.

2. Applies to the μPD703201Y, 703204Y, 70F3201Y, and 70F3204Y only.

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

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Pin Name	I/O	PULL	Function	Alternate Function
SI0	Input	Yes	Serial receive data input (CSI0)	P40
SI1			Serial receive data input (CSI1)	P30/RXD0
SI2			Serial receive data input (CSI2)	P910/A10
SI3			Serial receive data input (CSI3)	P913/A13
[SI4]			Serial receive data input (CSI4)	[P20]
SO0	Output	Yes	Serial transmit data output (CSI0)	P41/SDA[Note]
SO1			Serial transmit data output (CSI1)	P31/TXD0
SO2			Serial transmit data output (CSI2)	P911/A11
SO3			Serial transmit data output (CSI3)	P914/A14
[SO4]			Serial transmit data output (CSI4)	[P21]
TCLR0	Input	Yes	Timer clear input (TM0)	P43/INTP00/TI0
TCLR1			Timer clear input (TM1)	P45/INTP10/TI1
TI0	Input	Yes	External event/clock input (TM0)	P43/INTP00/TCLR0
TI1			External event/clock input (TM1)	P45/INTP10/TCLR1
TI2			External event/clock input (TM2)	P01/INTP0
TI3			External event/clock input (TM3)	P02/INTP1
TI4			External event/clock input (TM4)	P03/INTP2
TI5			External event/clock input (TM5)	P04/INTP3
TO0	Output	Yes	Timer output (TM0)	P44/INTP01
TO1			Timer output (TM1)	P46/INTP11
TO2			Timer output (TM2)	P94/A4
TO3			Timer output (TM3)	P95/A5
TO4			Timer output (TM4)	P96/A6
TO5			Timer output (TM5)	P97/A7
TXD0	Output	Yes	Serial transmit data output (UART0)	P31/SO1
TXD1			Serial transmit data output (UART1)	P99/A9
V_{DD}	–	–	Positive power supply pin for internal functions (except for subclock oscillator, RTC, and internal RAM)	–
V_{DD}BU	–	–	Positive power supply pin for backup (for subclock oscillator, RTC and internal RAM)	–
V_{SS}	–	–	Ground potential for internal functions (except for subclock oscillator, RTC, and internal RAM)	–
V_{SS}BU	–	–	Ground potential for backup (for subclock oscillator, RTC and internal RAM)	–
$\overline{WAIT}$	Input	No	External wait input	PCM0
$\overline{WR0}$	Output	No	Write strobe for external memory (lower 8 bits)	PCT0
$\overline{WR1}$			Write strobe for external memory (higher 8 bits)	PCT1

Note Applies to the μPD703201Y, 703204Y, 70F3201Y, and 70F3204Y only.

Remarks 1. PULL: On-chip pull-up resistor

2. Pins in brackets ([ ]) are only for the V850ES/SA3.

(4/4)

Pin Name	I/O	PULL	Function	Alternate Function
X1	Input	No	Connecting resonator for main clock	–
X2	–			–
XT1	Input	No	Connecting resonator for subclock	–
XT2	–			–

Remark PULL: On-chip pull-up resistor

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are show in Table 1-1. For the schematic circuit diagram of each type, refer to Figure 1-1.

Table 1-1. Types of Pin I/O Circuits (1/2)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins
P00	NMI	5-W	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P01 to P04	INTP0/TI2 to INTP3/TI5		
P05	INTP4		
[P20]	[SI4]	5-W	
[P21]	[SO4]	10-E	
[P22]	[$\overline{SCK4}$]	10-F	
P30	SI1/RXD0	5-W	
P31	SO1/TXD0	10-E	
P32	$\overline{SCK1}$	10-F	
P40	SI0	5-W	
P41	SO0/SDA[Note]	10-F	
P42	$\overline{SCK0}$/SCL[Note]	10-F	
P43	INTP00/TI0/TCLR0	5-W	
P44	INTP01/TO0		
P45	INTP10/TI1/TCLR1		
P46	INTP11/TO1		
P70 to P711, [P712 to P715]	ANI0 to ANI15	9	Independently connect to AV_{DD} or AV_{SS} via a resistor.
P80, P81	ANO0, ANO1	34	
P90, P91	A0, A1	5-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P92, P93	A2/INTP5, A3/INTP6	5-W	
P94 to P97	A4/TO2 to A7/TO5	5-A	
P98	A8/RXD1	5-W	
P99	A9/TXD1	5-A	
P910	A10/SI2	5-W	
P911	A11/SO2	10-E	
P912	A12/$\overline{SCK2}$	10-F	
P913	A13/SI3	5-W	
P914	A14/SO3	10-E	
P915	A15/$\overline{SCK3}$	10-F	
[PCD1 to PCD3]	–	5	
PCM0	$\overline{WAIT}$		
PCM1	CLKOUT		
PCM2	$\overline{HLDAK}$		

Note Applies to the μPD703201Y, 703204Y, 70F3201Y, and 70F3204Y only.

Remark Pins in brackets ([ ]) are only for the V850ES/SA3.

Table 1-1. Types of Pin I/O Circuits (2/2)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins
PCM3	$\overline{\text{HLDRQ}}$	5	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
[PCM4]	–		
[PCM5]	–		
PCS0 to PCS3	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$		
[PCS4 to PCS7]	–		
PCT0, PCT1	$\overline{\text{WR0}}$, $\overline{\text{WR1}}$		
[PCT2, PCT3]	–		
PCT4	$\overline{\text{RD}}$		
PCT5	–		
PCT6	ASTB		
PCT7	–		
PDH0 to PDH5, [PDH6, PDH7]	A16 to A21, [A22, A23]		
PDL0 to PDL4	AD0 to AD4		
PDL5	AD5/FLMD1[Note 1]		
PDL6 to PDL15	AD6 to AD15		
AV_{DD}	–	–	–
AV_{REF0}	–	–	Connect to AV_{SS} via a resistor.
AV_{REF1}	–	–	Connect to AV_{SS} via a resistor.
AV_{SS}	–	–	–
EV_{DD}	–	–	–
EV_{SS}	–	–	–
FLMD0[Note 1]	–	–	–
IC[Note 2]	–	–	–
$\overline{\text{RESET}}$	–	2	–
V_{DD}	–	–	–
$V_{DD}BU$	–	–	–
V_{SS}	–	–	–
$V_{SS}BU$	–	–	–
X1	–	–	–
X2	–	–	–
XT1	–	16	Connect to $V_{SS}BU$ via a resistor.
XT2	–	16	Leave open.

Notes 1. Applies to the μPD70F3201, 70F3201Y, 70F3204, and 70F3204Y only.

2. Applies to the μPD703201, 703201Y, 703204, and 703204Y only.

Remark Pins in brackets ([ ]) are only for the V850ES/SA3.

Figure 1-1. Pin I/O Circuits (1/2)

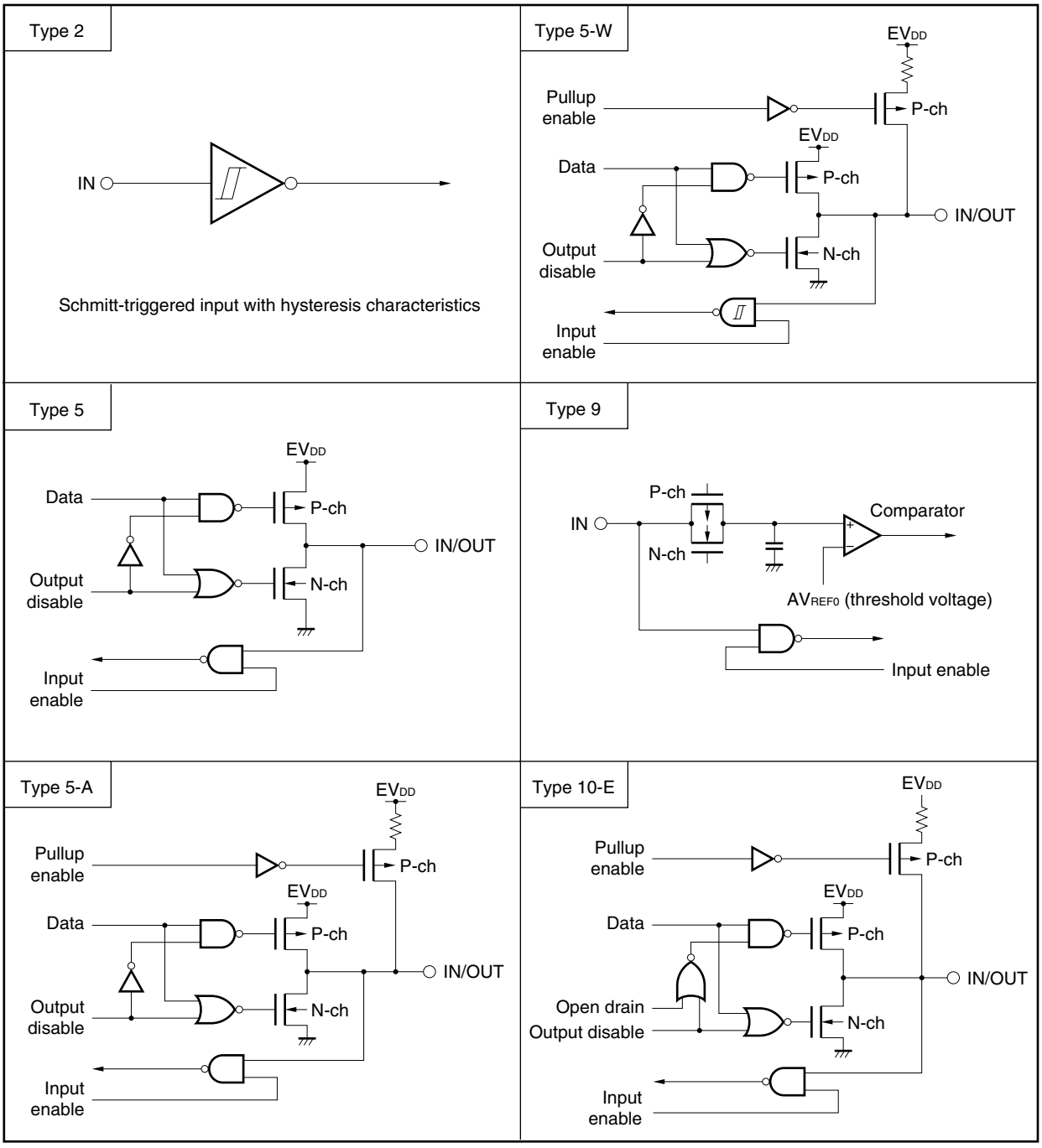
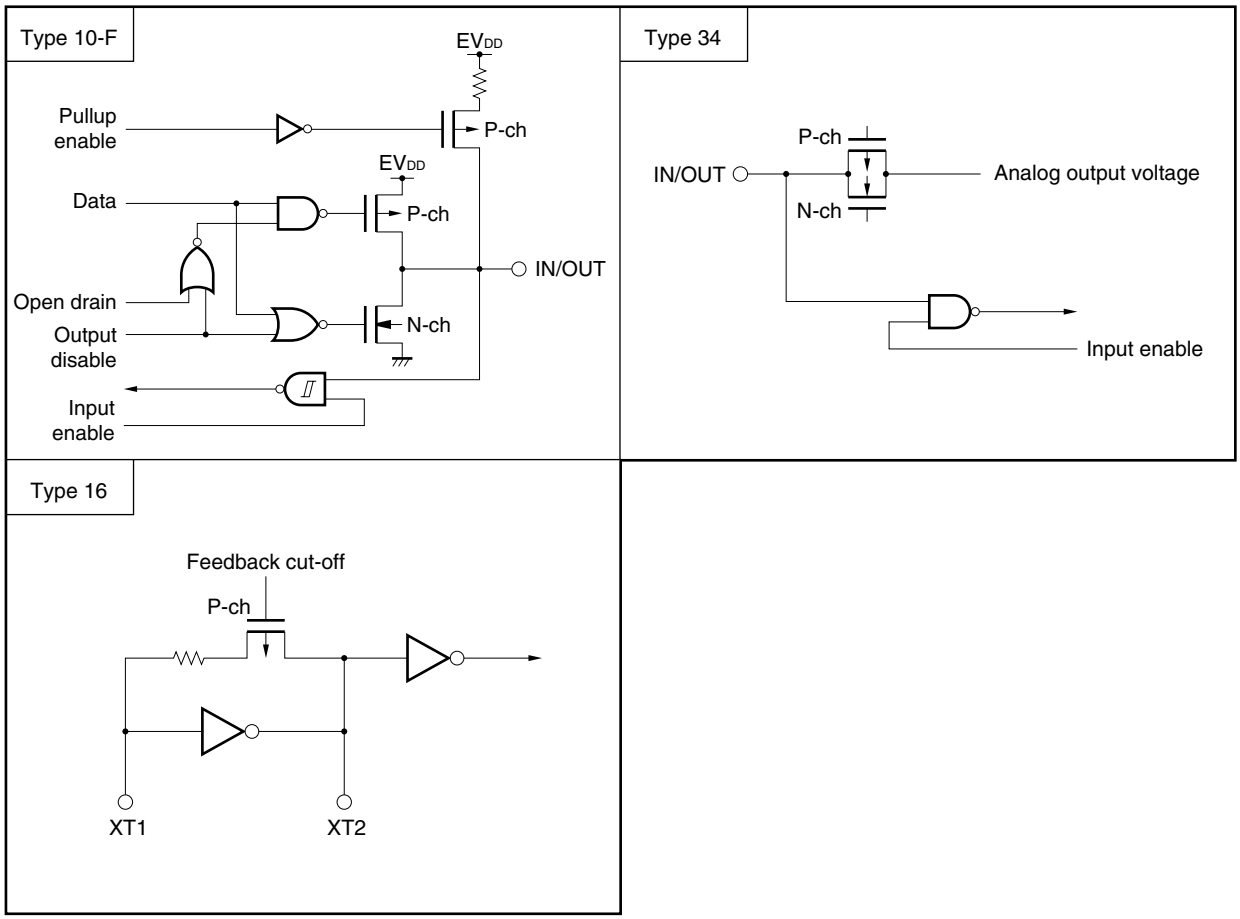


Figure 1-1. Pin I/O Circuits (2/2)



2. FUNCTION BLOCKS

2.1 Internal Units

Each internal unit of the V850ES/SA2 and V850ES/SA3 is described below.

(1) CPU

The CPU uses five-stage pipeline control to enable 1-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as the multiplier (16 bits × 16 bits → 32 bits) and the barrel shifter (32 bits), helps accelerate processing of complex instructions.

(2) Bus control unit (BCU)

The BCU starts the required external bus cycle based on the physical address obtained by the CPU. When an instruction is fetched from external memory area and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an internal instruction queue.

(3) ROM

This consists of a 256 KB mask ROM or flash memory mapped to the address space 0000000H to 003FFFFH. This area can be accessed by the CPU in 1-clock cycle when an instruction is fetched.

(4) RAM

This consists of a 16 KB RAM mapped to the address space 3FFB000H to 3FFEFFFH. This area can be accessed by the CPU in 1-clock cycle.

(5) Interrupt controller (INTC)

This controller services hardware interrupt requests (NMI, INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiple servicing control can be performed for interrupt sources.

(6) Clock generator (CG)

The clock generator includes two types of oscillators, one for the main clock (f_{XX}) and one for the subclock (f_{XT}), generates five types of clocks (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, and $f_{XX}/32$), and supplies one of them as the operating clock for the CPU (f_{CPU}). The subclock can only be selected as the operation clock of the real-time counter.

(7) Timer/counter

A two-channel 16-bit timer/event counter and a four-channel 8-bit timer/event counter are incorporated, which enables measurement of pulse intervals and frequency as well as programmable pulse output.

Two channels of the 8-bit timer/event counter can be connected via a cascade connection to enable use as a 16-bit timer.

(8) Real-time counter (for watch)

This counter counts the reference time period (1 second) for watch counting by using the 32.768 kHz subclock or the main clock. At the same time, the real-time counter can also be used as an interval timer that uses the main clock as a source clock. This counter includes week, date, hour, minute, and second counters, and is capable of counting up to 4,095 weeks.

(9) Watchdog timer

This timer detects inadvertent program loops, system abnormalities, etc.

It can also be used as an interval timer.

When used as a watchdog timer, it generates a non-maskable interrupt request (INTWDT) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request (INTWDTM) after an overflow occurs.

(10) Serial interface (SIO)

The V850ES/SA2 and V850ES/SA3 incorporate three kinds of serial interfaces: asynchronous serial interfaces (UART0 and UART1), clocked serial interfaces (V850E/SA2: CSI0 to CSI3, V850ES/SA3: CSI0 to CSI4), and an I^2C bus interface (I^2C). The V850ES/SA2 is capable of using up to 4 channels and the V850ES/SA3 is capable of using up to 5 channels simultaneously. Among these channels, one channel can be switched between UART and CSI, and other one channel can be switched between CSI and I^2C.

For UART0 and UART1, data is transferred via the TXDO, TXD1, RXD0, and RXD1 pins.

For CSI0 to CSI3, data is transferred via the SO0 to SO3, SI0 to SI3, and $\overline{SCK0}$ to $\overline{SCK3}$ pins.

For CSI4, data is transferred via the SO4, SI4, and $\overline{SCK4}$ pins (V850ES/SA3 only).

For I^2C, data is transferred via the SDA and SCL pins.

I^2C is incorporated in the μPD703201Y, 703204Y, 70F3201Y and 70F3204Y only.

UART includes an on-chip dedicated baud rate generator.

(11) A/D converter

This high-speed, high-resolution 10-bit A/D converter includes 12 analog input pins for the V850ES/SA2 and 16 for the V850ES/SA3. Conversion is performed using the successive approximation method.

(12) D/A converter

A two-channel 8-bit resolution D/A converter is incorporated. This D/A converter uses the R string method.

(13) DMA controller

A 4-channel DMA controller is incorporated. Data is transferred between internal RAM, on-chip peripheral I/O, and external memory based on interrupt requests by the on-chip peripheral I/O.

(14) ROM correction

This is a function that replaces a part of the program in the mask ROM with a program in the internal RAM for execution. Four points can be corrected.

(15) Ports

The ports function as both general-purpose ports and control pins, as shown below.

Port	I/O	Port Function	Control Function
P0	6-bit I/O	General-purpose port	NMI, external interrupt, timer input
P2[Note]	3-bit I/O		Serial interface
P3	3-bit I/O		Serial interface
P4	7-bit I/O		Serial interface, timer I/O, timer trigger
P7	12-bit input (V850ES/SA2) 16-bit input (V850ES/SA3)		A/D converter analog input
P8	2-bit input		D/A converter analog output
P9	16-bit I/O		External address bus, serial interface, timer output, external interrupt
PCD[Note]	3-bit I/O		–
PCM	4-bit I/O (V850ES/SA2) 6-bit I/O (V850ES/SA3)		External bus interface
PCS	4-bit I/O (V850ES/SA2) 8-bit I/O (V850ES/SA3)		Chip select output
PCT	6-bit I/O (V850ES/SA2) 8-bit I/O (V850ES/SA3)		External bus interface
PDH	6-bit I/O (V850ES/SA2) 8-bit I/O (V850ES/SA3)		External address bus
PDL	16-bit I/O		External address/data bus

Note V850ES/SA3 only

3. CPU FUNCTIONS

The CPU of the V850ES/SA2 and V850ES/SA3 is based on RISC architecture and executes most instructions in a 1-clock cycle by using a 5-stage pipeline.

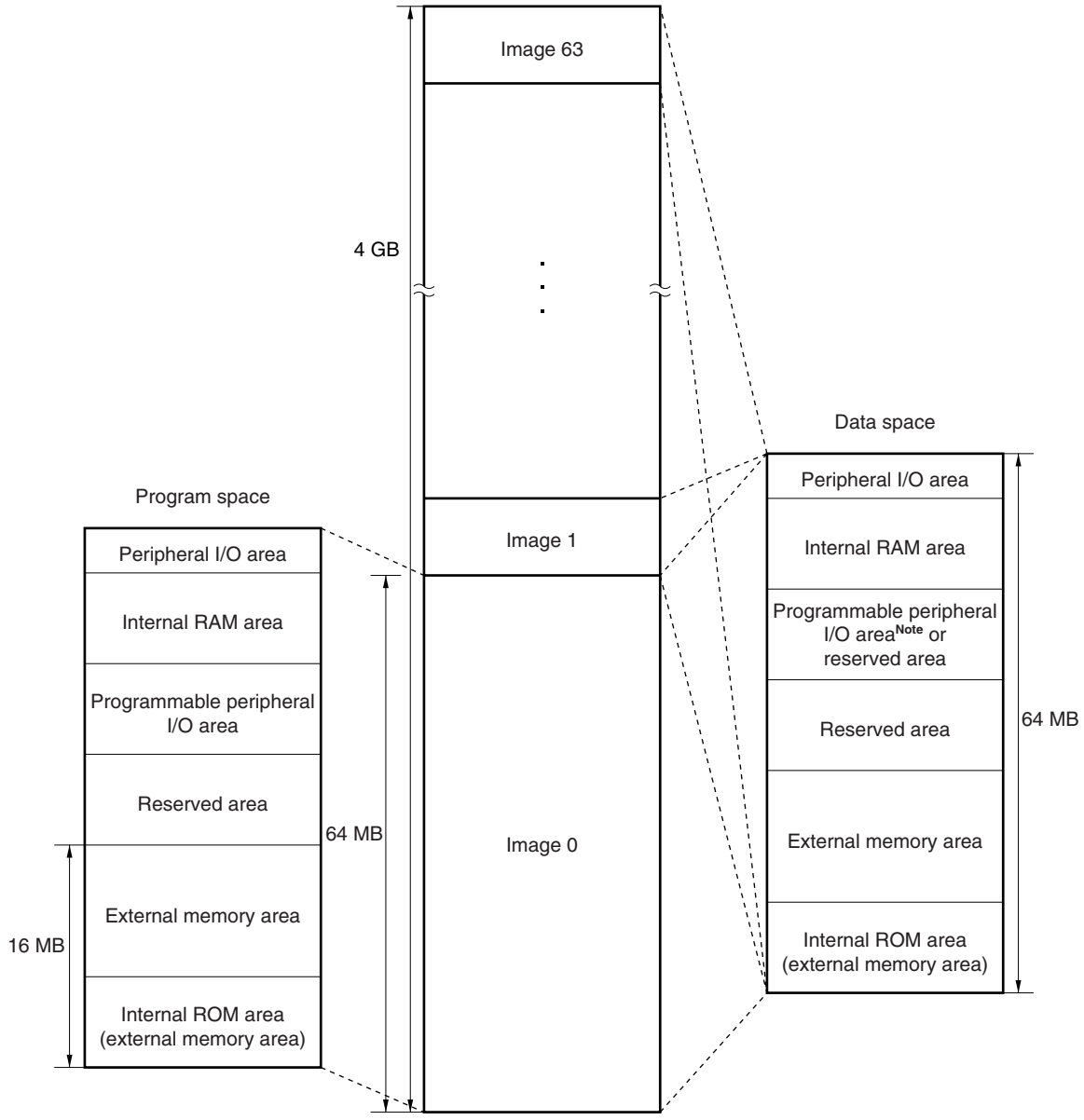
The features of the CPU are as follows.

- Minimum instruction execution time: 59 ns (@ 17 MHz operation with main system clock (fxx))
  74 ns (@ 13.5 MHz operation with main system clock (fxx))
- Address space: 64 MB linear
  - Memory block division function: 2 MB, 2 MB, 4 MB, 8 MB = Total four blocks
- General-purpose registers: 32 bits × 32
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiplication/division instructions
- Saturation operation instructions
- 1-clock 32-bit shift instruction
- Load/store instructions with long/short format
- Internal memory
  - Mask ROM: 256 KB (μPD703201, 703201Y, 703204, 703204Y)
    Flash memory: 256 KB (μPD70F3201, 70F3201Y, 70F3204, 70F3204Y)
  - RAM: 16 KB
- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

4. MEMORY MAP

The memory maps of the V850ES/SA2 and V850ES/SA3 are shown below.

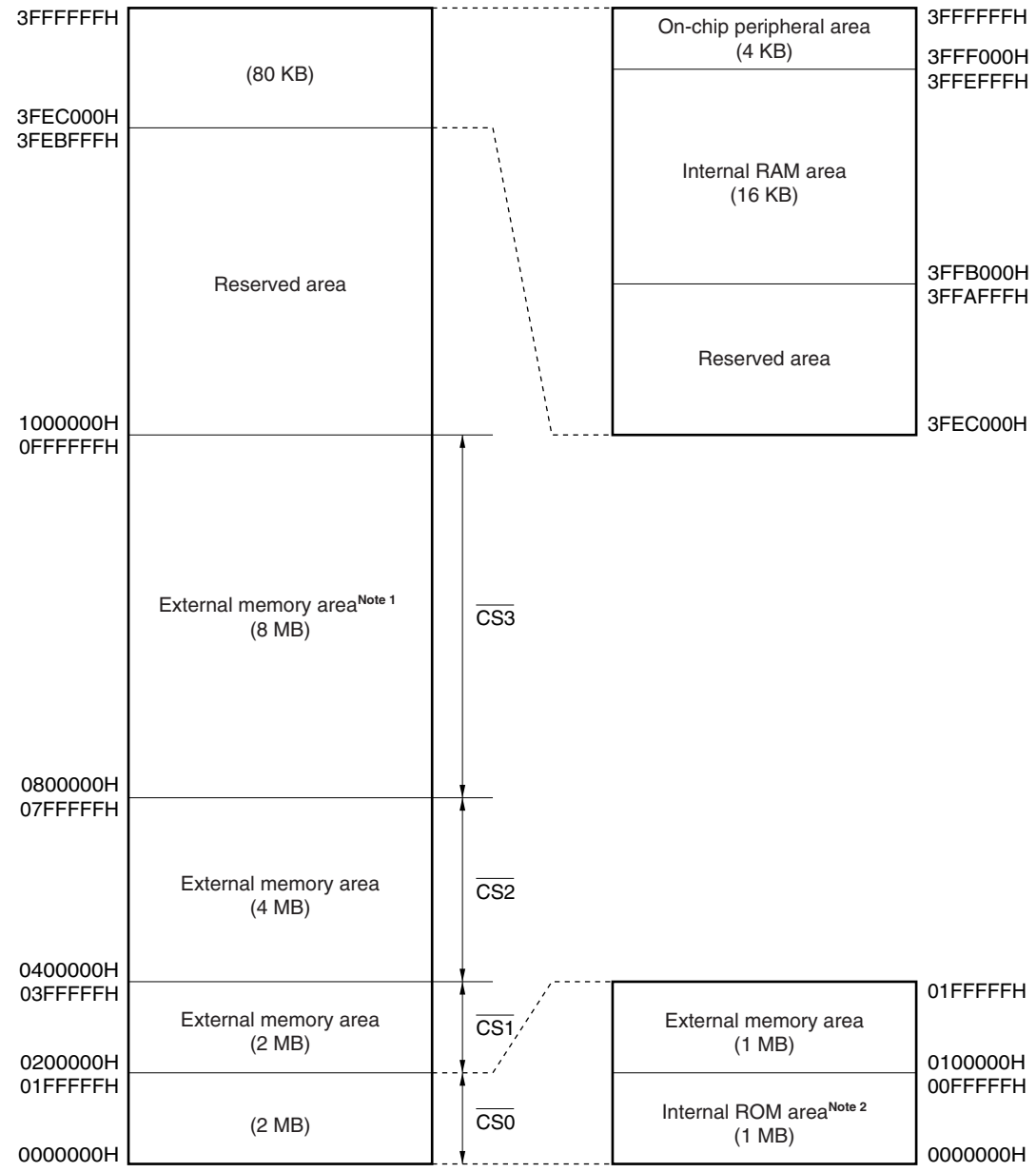
O Address Space



Note The programmable peripheral I/O area in the data space can only be used for image 4n (n = 0 to 15). It cannot be used for other images (reserved area).

Remark Internal ROM: 256 KB (0000000H to 003FFFFH)
Internal RAM: 16 KB (3FFB000H to 3FFEFFFH)

○ **Data Memory Map**



Notes 1. In the V850ES/SA2, this area is the 4 MB space of 0800000H to 0BFFFFFH (0C00000H to 0FFFFFFH is an image of 0800000H to 0BFFFFFH).

2. This area is used as an external memory area during data write access.

5. EXTERNAL BUS INTERFACE FUNCTION

The V850ES/SA2 and V850ES/SA3 incorporate an external bus interface function that can be used to connect memories, such as ROM or RAM, and peripheral I/O externally.

The external bus interface function has the following features.

- Separate bus/multiplexed bus output selectable
- 8-bit/16-bit data bus sizing function
- Chip select function for four spaces
- Wait function
  - Programmable wait function
  - External wait function
- Idle state function
- Bus hold function

The following pins are used for the external bus interface.

Table 5-1. List of Bus Control Pins (When Multiplexed Bus Is Selected)

Bus Control Pin	Alternate Function	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
A16 to A23[Note]	PDH0 to PDH7	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	PCS0 to PCS3	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
ASTB	PCT6	Output	Address strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

Note A16 to A21 in the V850ES/SA2.

Table 5-2. List of Bus Control Pins (When Separate Bus Is Selected)

Bus Control Pin	Alternate Function	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Data bus
A0 to A15	P90 to P915	Output	Address bus
A16 to A23[Note]	PDH0 to PDH7	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	PCS0 to PCS3	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

Note A16 to A21 in the V850ES/SA2.

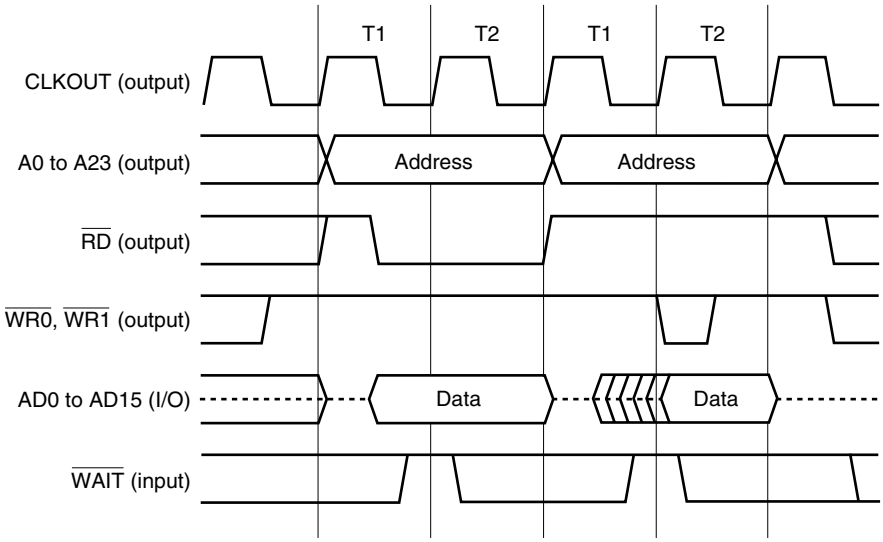
The number of basic clocks required for accessing each area in the address space is as follows.

Table 5-3. Number of Access Clocks

Bus Cycle Type \ Area (Bus Width)	Internal ROM (32 Bits)	Internal RAM (32 Bits)	External Memory (16 Bits)
Instruction fetch (normal access)	1	1 or 2	3 + n[Note]
Instruction fetch (branch)	2	1 or 2	3 + n[Note]
Operand data access	3	1	3 + n[Note]

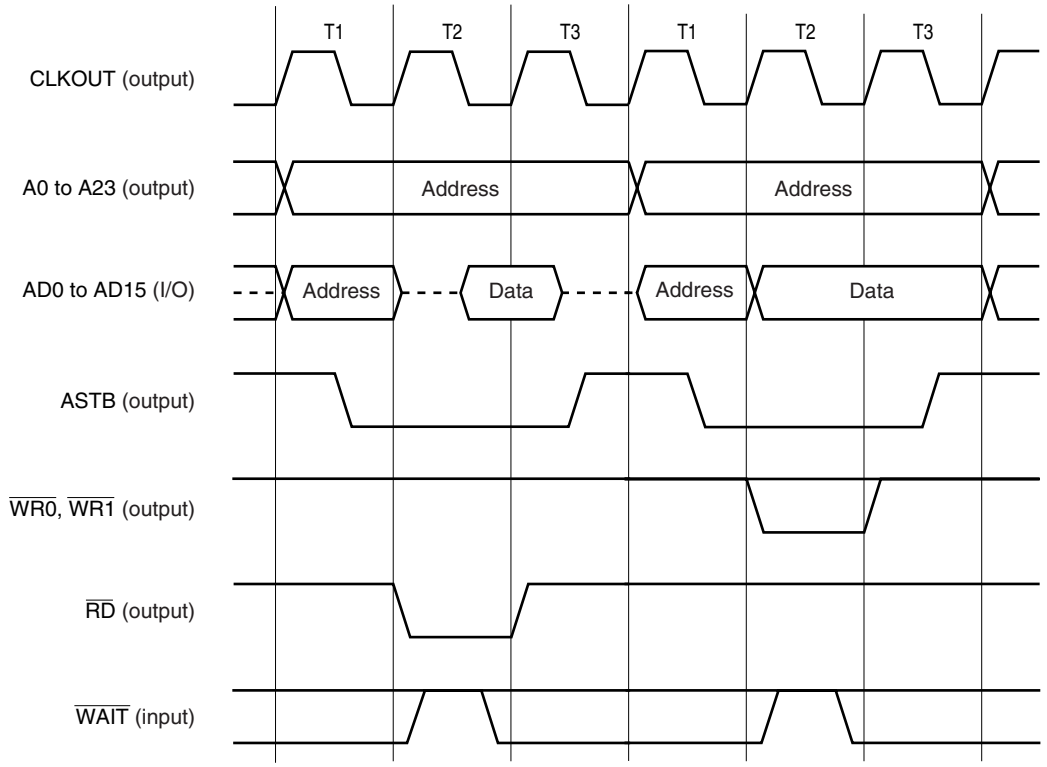
Note 2 + n clocks when the separate bus is selected. n is the number of waits.

Figure 5-1. Example of Timing In Separate Bus Mode (Read → Write)



Remark The broken lines indicates the high-impedance state

Figure 5-2. Example of Timing In Multiplexed Bus Mode (Read → Write)



Remark The broken lines indicate the high-impedance state.

6. INTERRUPT SERVICING/EXCEPTION PROCESSING FUNCTION

The features of the interrupt servicing/exception processing function are as follows.

- Interrupt
  - Non-maskable interrupt: 2 sources
  - Maskable interrupt
    μPD703201, 70F3201: External 8, internal 30 sources
    μPD703201Y, 70F3201Y: External 8, internal 31 sources
    μPD703204, 70F3204: External 8, internal 31 sources
    μPD703204Y, 70F3204Y: External 8, internal 32 sources
  - 8-level programmable priority control
  - Mask specification for the interrupt request according to priority
  - Mask specification for each maskable interrupt request
  - Noise elimination, edge detection, and valid edge specification of an external interrupt request
- Exceptions
  - Software exception: 32 sources
  - Exception trap: 2 sources (illegal op code exception, debug trap)

Table 6-1 shows the interrupt/exception sources.

Table 6-1. Interrupt Source List (1/2)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				WDT overflow (WDTRES)	WDT				
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	–	0010H	00000010H	nextPC	–
		–	INTWDT	WDT overflow	WDT	0020H	00000020H	nextPC	–
Software exception	Exception	–	TRAP0n[Note]	TRAP instruction	–	004nH[Note]	00000040H	nextPC	–
		–	TRAP1n[Note]	TRAP instruction	–	005nH[Note]	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Illegal op code/ DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM	Internal timer overflow	WDT	0080H	00000080H	nextPC	WDTIC
		1	INTP0	INTP0 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin valid edge input	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTRTC	RTC interrupt	RTC	0100H	00000100H	nextPC	RTCIC
		9	INTCC00	CC00 capture trigger input/match between TM0 and CC00	TM0	0110H	00000110H	nextPC	CCIC00
		10	INTCC01	CC01 capture trigger input/match between TM0 and CC01	TM0	0120H	00000120H	nextPC	CCIC01
		11	INTOVF0	TM0 overflow	TM0	0130H	00000130H	nextPC	OVFIC0
		12	INTCC10	CC10 capture trigger input/match between TM1 and CC10	TM1	0140H	00000140H	nextPC	CCIC10
		13	INTCC11	CC11 capture trigger input/match between TM1 and CC11	TM1	0150H	00000150H	nextPC	CCIC11
		14	INTOVF1	TM1 overflow	TM1	0160H	00000160H	nextPC	OVFIC1
		15	INTTM2	Match between TM2 and CR2/TM2 overflow	TM2	0170H	00000170H	nextPC	TMIC2
		16	INTTM3	Match between TM3 and CR3/TM3 overflow	TM3	0180H	00000180H	nextPC	TMIC3

Note n: Value of 0 to FH

Table 6-1. Interrupt Source List (2/2)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	17	INTTM4	Match between TM4 and CR4/TM4 overflow	TM4	0190H	00000190H	nextPC	TMIC4
		18	INTTM5	Match between TM5 and CR5/TM5 overflow	TM5	01A0H	000001A0H	nextPC	TMIC5
		19	INTCSI0	CSI0 transfer end	CSI0	01B0H	000001B0H	nextPC	CSIIC0
		20	INTIIC[Note 1]	I^2C transfer end	I^2C	01C0H	000001C0H	nextPC	IICIC0
		21	INTCSI1	CSI1 transfer end	CSI1	01D0H	000001D0H	nextPC	CSIIC1
		22	INTSRE0	UART0 receive error	UART0	01E0H	000001E0H	nextPC	SREIC0
		23	INTSR0	UART0 receive end	UART0	01F0H	000001F0H	nextPC	SRIC0
		24	INTST0	UART0 transfer end	UART0	0200H	00000200H	nextPC	STIC0
		25	INTCSI2	CSI2 transfer end	CSI2	0210H	00000210H	nextPC	CSIIC2
		26	INTSRE1	UART1 receive error	UART1	0220H	00000220H	nextPC	SREIC1
		27	INTSR1	UART1 receive end	UART1	0230H	00000230H	nextPC	SRIC1
		28	INTST1	UART1 transmit end	UART1	0240H	00000240H	nextPC	STIC1
		29	INTCSI3	CSI3 transfer end	CSI3	0250H	00000250H	nextPC	CSIIC3
		30	INTCSI4[Note 2]	CSI4 transfer end	CSI4	0260H	00000260H	nextPC	CSIIC4
		31	INTAD	A/D conversion end	ADC	0270H	00000270H	nextPC	ADIC
		32	INTDMA0	DMA0 transfer end	DMA	0280H	00000280H	nextPC	DMAIC0
		33	INTDMA1	DMA1 transfer end	DMA	0290H	00000290H	nextPC	DMAIC1
		34	INTDMA2	DMA2 transfer end	DMA	02A0H	000002A0H	nextPC	DMAIC2
		35	INTDMA3	DMA3 transfer end	DMA	02B0H	000002B0H	nextPC	DMAIC3
		36	INTROV	RTC overflow	RTC	02C0H	000002C0H	nextPC	ROVIC
		37	INTBRG	BRG match	BRG	02D0H	000002D0H	nextPC	BRGIC

Note 1. Valid for the μPD703201Y, 70F3201Y, 703204Y and 70F3204Y only.

2. Valid for the V850E/SA3 only.

Remarks 1. Default Priority: Priority that applies when two or more maskable interrupt requests occur at the same time. The highest priority is 0.

Restored PC: The value of the PC saved to EIPC or FEPC when interrupt servicing/exception processing is started. However, the value of the restored PC saved when an interrupt is acknowledged during division instruction (DIV, DIVH, DIVU, DIVHU) execution is the value of the PC of the current instruction (DIV, DIVH, DIVU, DIVHU).

nextPC: The value of the PC to be processed after an interrupt/exception.

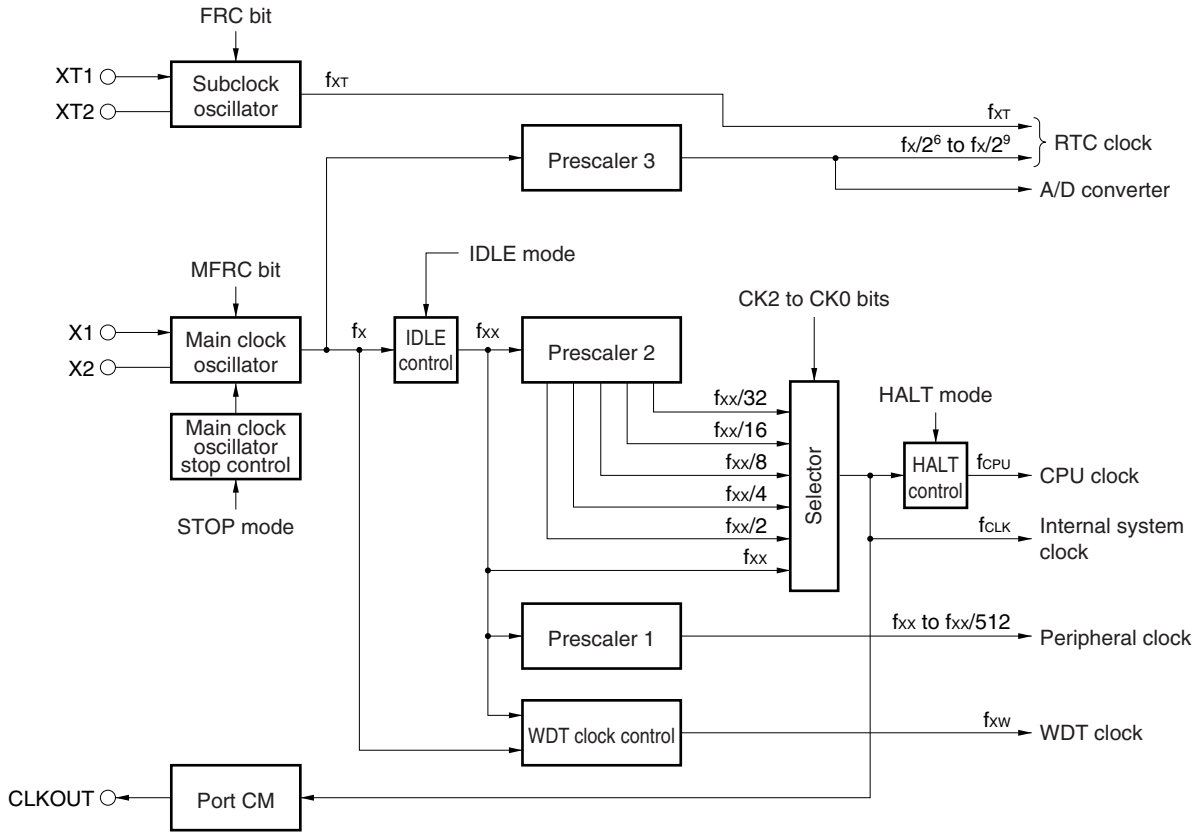
2. The execution address of the illegal instruction when an illegal op code exception occurs is calculated with (Restored PC – 4).

7. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- Main clock oscillator
  - 2 to 17 MHz (@ V_{DD} = 2.3 to 2.7 V operation)
  - 2 to 13.5 MHz (@ V_{DD} = 2.2 to 2.7 V operation)
- Subclock oscillator
  - 32.768 kHz (@ V_{DD} = 2.2 to 2.7 V operation)
- Internal system clock generation
  - 6 levels (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$)
- Peripheral clock generation
- Clock output function

The following figure shows the configuration of the clock generation function.



Remark f_X, f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_{CLK}: Internal system clock frequency
f_{XW}: Watchdog timer clock frequency

8. POWER SAVE FUNCTION

The V850ES/SA2 and V850ES/SA3 have the following power save functions to realize an effective low-power-consuming system.

- HALT mode: Only the clock of the CPU is stopped in this mode.
- IDLE mode: All operations on the chip other than oscillator operation are stopped in this mode.
- STOP mode: All operations on the chip other than subclock oscillator operation are stopped in this mode.
- Backup mode: The power supply other than for the subclock oscillator, real-time counter, and internal RAM can be disconnected.

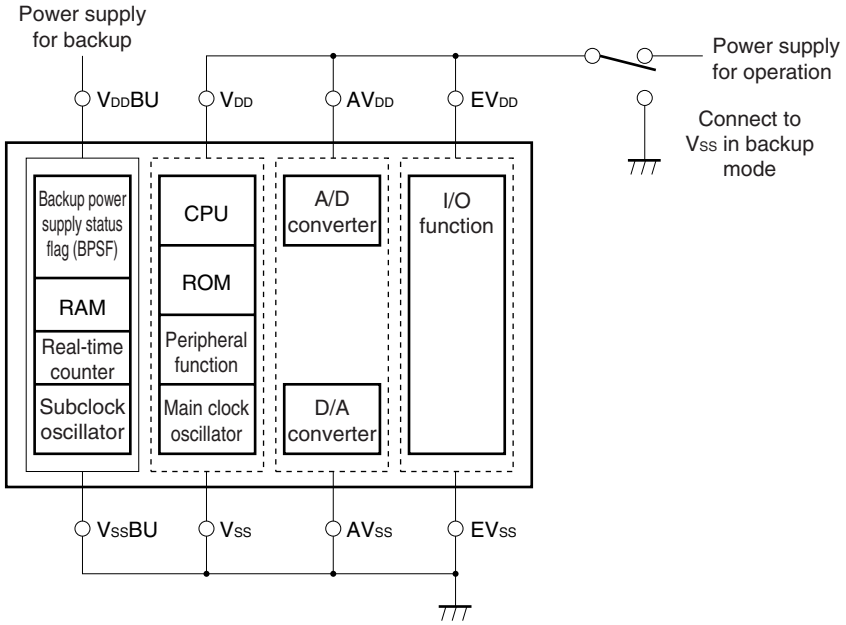
The following table shows the operating states of the on-chip peripheral functions in each mode.

Parameter	HALT Mode	IDLE Mode	STOP Mode	Backup Mode
V_{DD}, EV_{DD}, AV_{DD}	Power supplied			Power OFF possible
$V_{DD}BU$	Power supplied			
CPU operation	Stopped			
On-chip peripheral function operation	Enabled	Stopped		
Main clock oscillator operation	Enabled		Stopped	
Subclock oscillator operation	Enabled			
Real-time counter function, RAM retention	Enabled			
Release condition	• Non-maskable interrupt request • Unmasked maskable interrupt request • $\overline{\text{RESET}}$ pin input			$\overline{\text{RESET}}$ pin input after power is supplied

- **Backup mode overview**

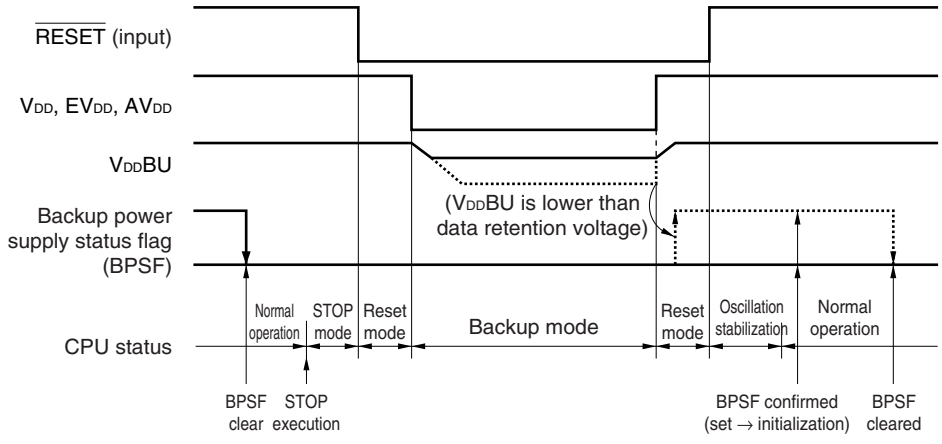
The V850ES/SA2 and V850ES/SA3 are put in backup mode by stopping supplying power other than the backup power supply (V_{DD}BU) in STOP mode.

The backup power supply supplies power only to the subclock oscillator, real-time counter, and internal RAM, as shown in the figure below. Other on-chip functions including the CPU cannot operate since the power supply is stopped.



In backup mode, subclock oscillator operation, real-time counter count operation, and internal RAM data retention are enabled.

If the voltage is lower than the data retention voltage in backup mode, a backup power supply status flag (BPSF) is set and that internal RAM retention data can be detected as invalid. When this flag is set, the real-time counter and the RAM should be initialized at reset start.



9. TIMER/COUNTER FUNCTION

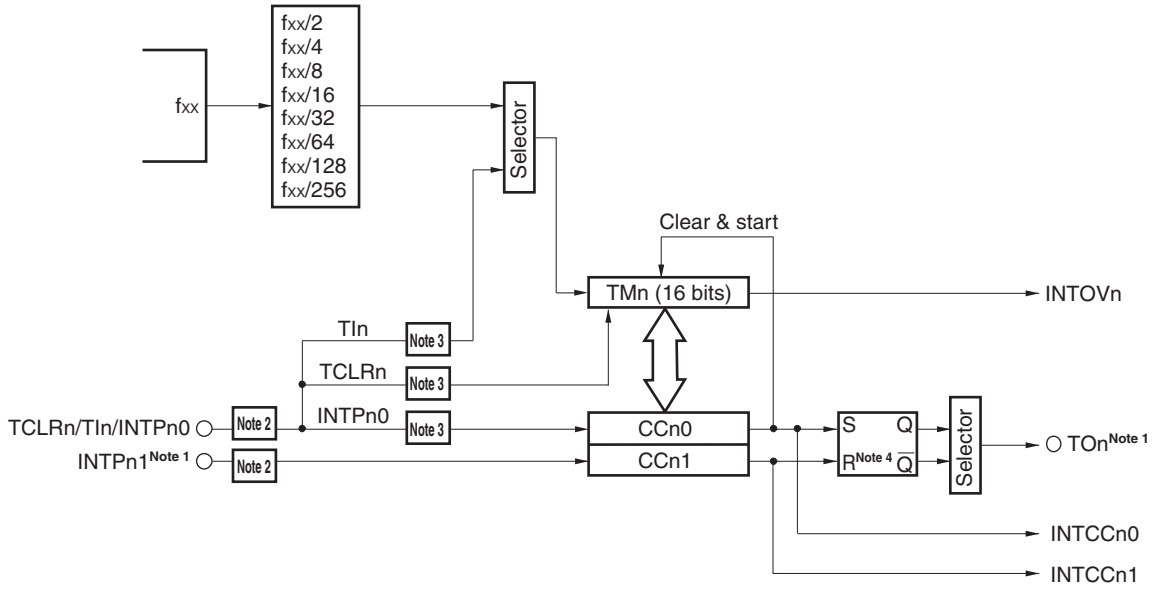
The timer/counter function has the following features.

- 16-bit timer/counter (TM0, TM1)
  - Capture/compare common registers: 2 for each
  - Interrupt request sources
    - Capture/match interrupt requests: 2 sources for each
    - Overflow interrupt requests: 1 source for each
  - Timer/counter count clock sources: 2 types
    (Selection of external pulse input or internal system clock division)
  - Either free-running mode or overflow stop mode can be selected as the operation mode when the timer/counter overflows
  - Timer/counter can be cleared by a match of the timer/counter and a compare register
  - External pulse outputs: 1 for each

- 8-bit timers (TM2 to TM5)
  - Stand-alone mode (mode in which a single timer is used)
    - Interval timer
    - External event counter
    - Square-wave output
    - PWM output
  - Cascade connection mode (mode in which two timers are used connected in cascade: 16-bit resolution)
    - 16-bit resolution interval timer
    - 16-bit resolution external event counter
    - 16-bit resolution square-wave output

The following figure shows the configuration of the timer/counter function.

(1) TM0, TM1



Notes 1. The INTPn1 pin is used as the TOn pin.

2. Noise eliminator

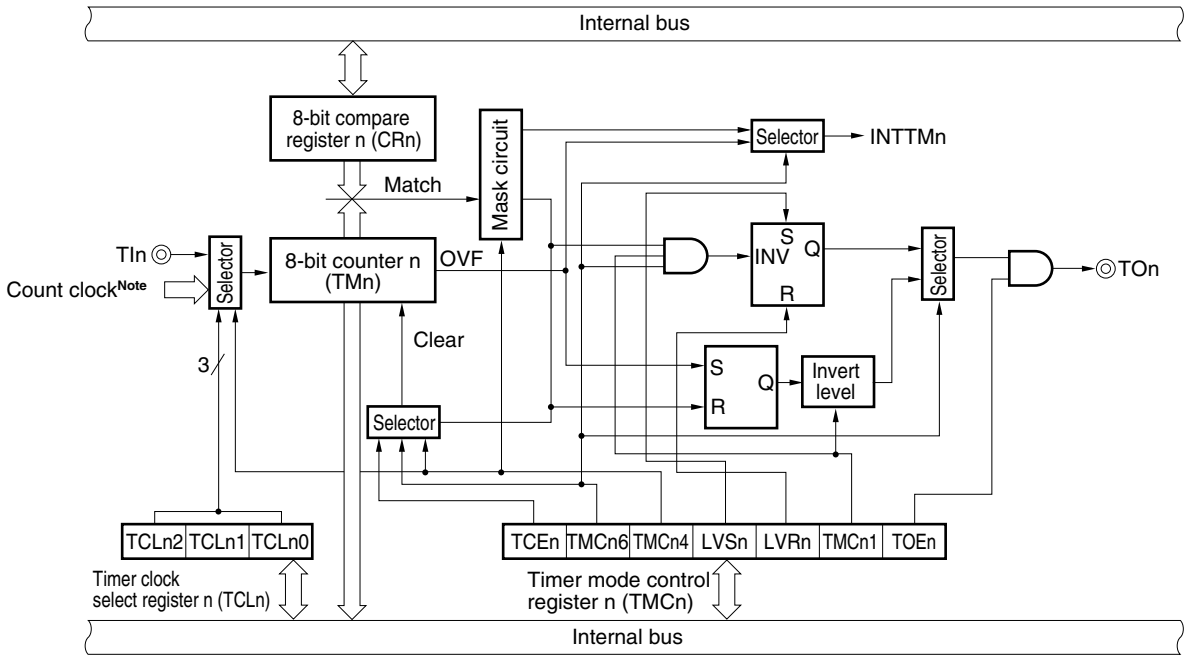
3. Edge detector

4. Reset priority

Remarks 1. n = 0, 1

2. f_{XX}: Main clock frequency

(2) TM2 to TM5



Note The count clock is set by the TCLn register.

- When n = 2, 3
  - fxx/4
  - fxx/8
  - fxx/16
  - fxx/32
  - fxx/128
  - fxx/512
- When n = 4, 5
  - fxx/4
  - fxx/8
  - fxx/16
  - fxx/32
  - fxx/128
  - fxx/256

Remarks 1. "——◎" is a signal that can be directly connected to a port.

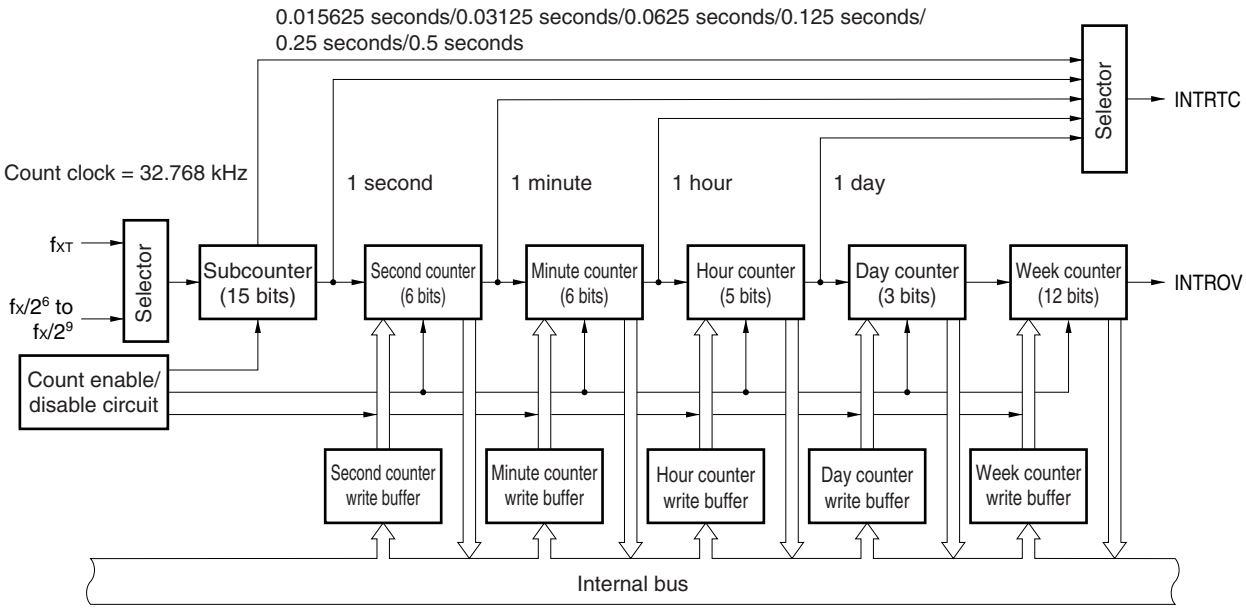
2. n = 2 to 5

10. REAL-TIME COUNTER FUNCTION

The real-time counter function has the following features.

- Includes counters of weeks, days, hours, minutes, and seconds, and can count up to 4,095 weeks.
- Counters of weeks, days, hours, minutes, and seconds can be read during operation and while operation is stopped.
- Week counter overflow interrupt request occurrence (INTROV)
- Interval interrupt request occurrence (INTRTC) at a fixed interval (can be selected from the following)
  0.015625 seconds, 0.03125 seconds, 0.0625 seconds, 0.125 seconds, 0.25 seconds, 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day
- When subclock (f_{XT}) is selected, operable only with power supply to $V_{DD}BU$.

The following figure shows the configuration of the real-time counter function.



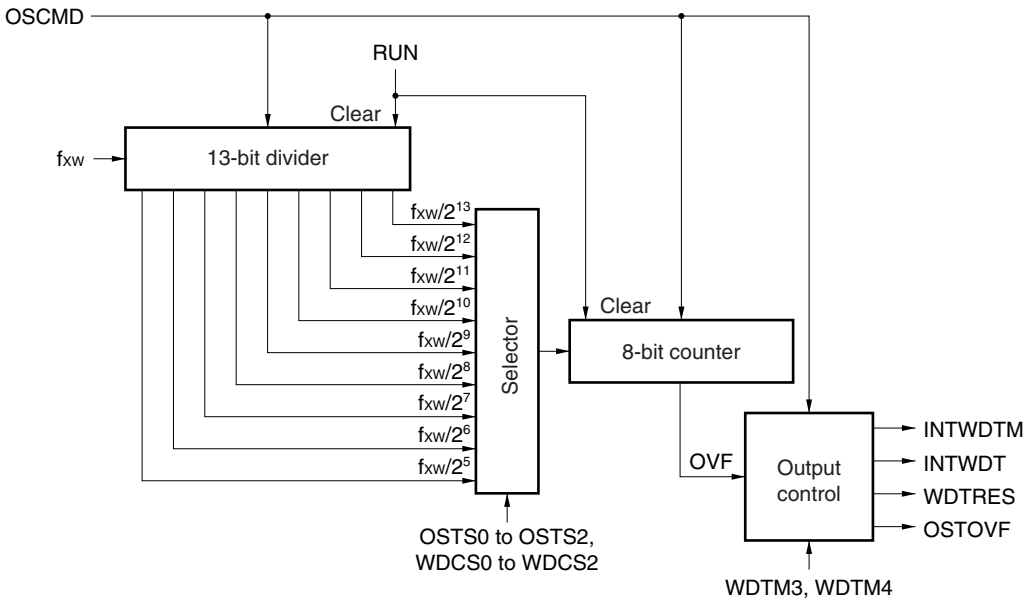
Remark f_X: Main clock frequency
f_{XT}: Subclock frequency

11. WATCHDOG TIMER FUNCTION

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer
- Timer for oscillation stabilization

The following figure shows the configuration of the watchdog timer function.



Remarks 1. WDTRES: Reset signal triggered by WDT overflow
OSTOVF: Overflow signal for oscillation stabilization
OSCMD: Timer mode signal for oscillation stabilization
fxw: Watchdog timer clock frequency

2. During counting of oscillation stabilization time: fxw = fx/2
Other than above: fxw = fxx/2

12. SERIAL INTERFACE FUNCTION

The V850ES/SA2 and V850ES/SA3 include the following three types of serial interfaces.

Type	V850ES/SA2	V850ES/SA3
3-wire serial I/O	4 channels (CSI0 to CSI3)	5 channels (CSI0 to CSI4)
Asynchronous serial interface	2 channels (UART0, UART1)	
I^2C bus[Note]	1 channel (I^2C)[Note]	

Note Available only in the μPD703201Y, 703204Y, 70F3201Y, and 70F3204Y.

Some functions are used alternately as follows.

- CSI0/I^2C
- CSI1/UART0
- CSI2
- UART1
- CSI3
- CSI4 (V850ES/SA3 only)

12.1 3-Wire Serial I/O (CSIn)

Remark In this section, the value of n is as follows.
n = 0 to 3 (V850ES/SA2)
n = 0 to 4 (V850ES/SA3)

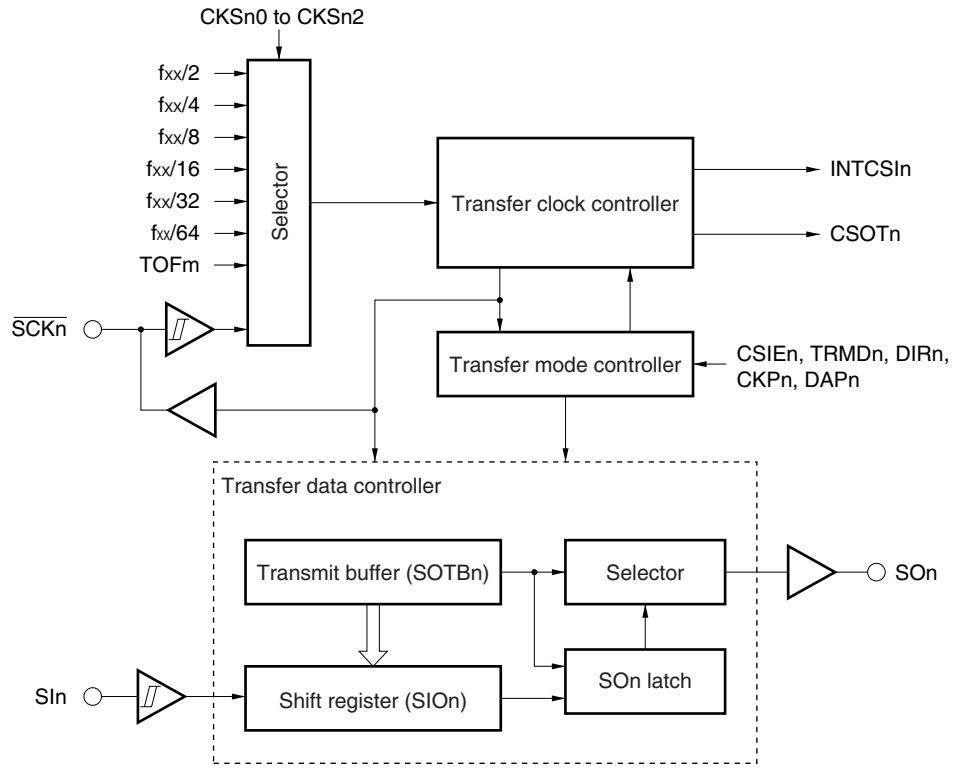
The 3-wire serial I/O (CSIn) transfers data using following three lines.

- $\overline{SCKn}$ (serial clock)
- SOn (serial data output)
- SIn (serial data input)

The 3-wire serial I/O (CSIn) has the following features.

- Transfer data length: Fixed to 8 bits
- Transfer data MSB/LSB first can be switched
- Transfer clock can be selected from eight clocks (seven master clocks, one slave clock)
- Transmit/receive mode or receive-only mode can be specified
- On-chip 8-bit transmit buffer
- Transfer data transmit/receive timing with respect to the transfer clock can be changed

The following figure shows the configuration of the 3-wire serial I/O (CSIn).



Remarks 1. When n = 0: m = 2
When n = 1: m = 3
When n = 2: m = 4
When n = 3: m = 5
When n = 4: m = 5 (V850ES/SA3 only)

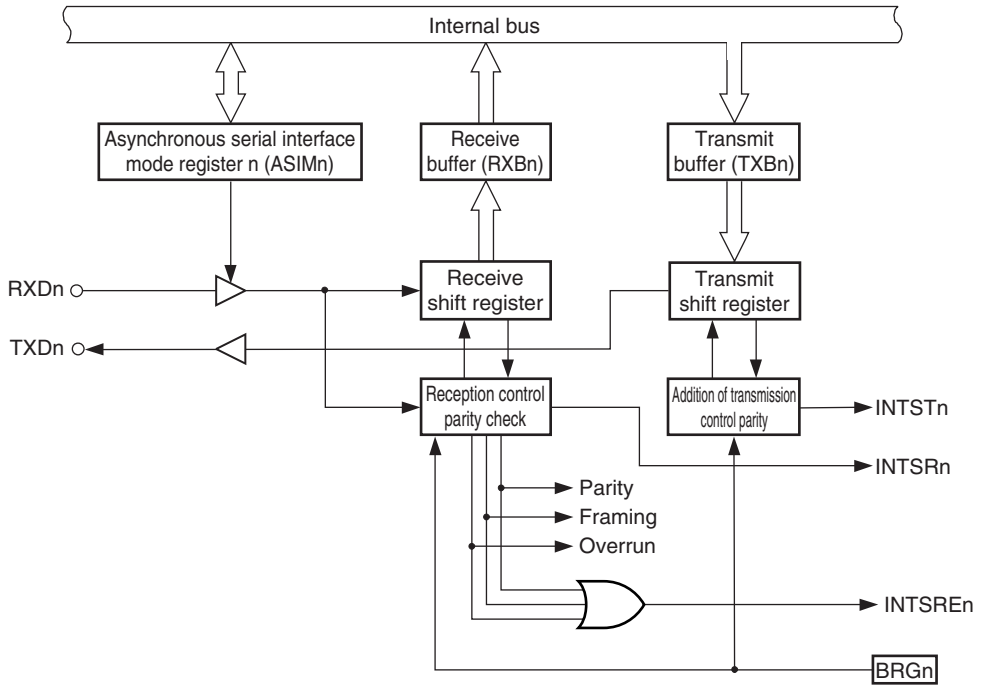
2. fxx: Main clock frequency

12.2 Asynchronous Serial Interface (UART0 and UART1)

The asynchronous serial interface (UART0 and UART1) has the following features.

- Two modes
  - Operation stop mode (used when serial transfers are not performed to enable a reduction in power consumption)
  - Asynchronous serial interface mode
- Full-duplex transmission
- 2-pin configuration
  - TXD0 and TXD1: Transmit data output pins
  - RXD0 and RXD1: Receive data input pins
- 3 types of interrupt sources
  - Receive error interrupt (INTSRE0 and INTSRE1)
  - Receive end interrupt (INTSR0 and INTSR1)
  - Transmit end interrupt (INTST0 and INTST1)
- Character length: 7 bits/8 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1 bit/2 bits
- On-chip baud rate generator

The following figure shows the configuration of the asynchronous serial interface (UART0 and UART1).



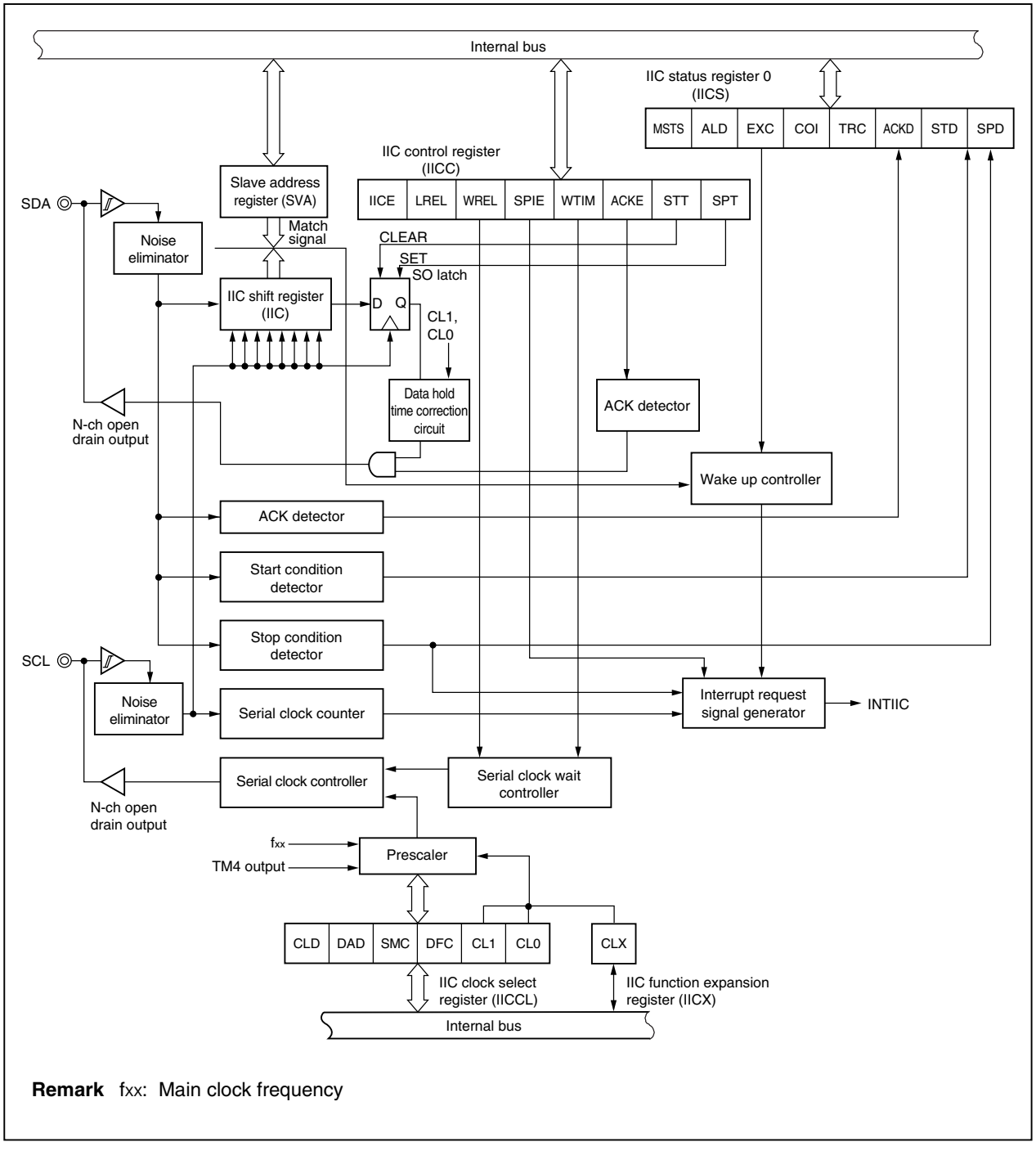
Remark n = 0, 1

12.3 I²C Bus (I²C) (μPD703201Y, 703204Y, 70F3201Y, 70F3204Y)

The I²C bus has the following features.

- Two modes
  - Operation stop mode (used when serial transfers are not performed to enable a reduction in power consumption)
  - I²C bus mode (supporting multi masters)

The following figure shows the configuration of the I²C bus



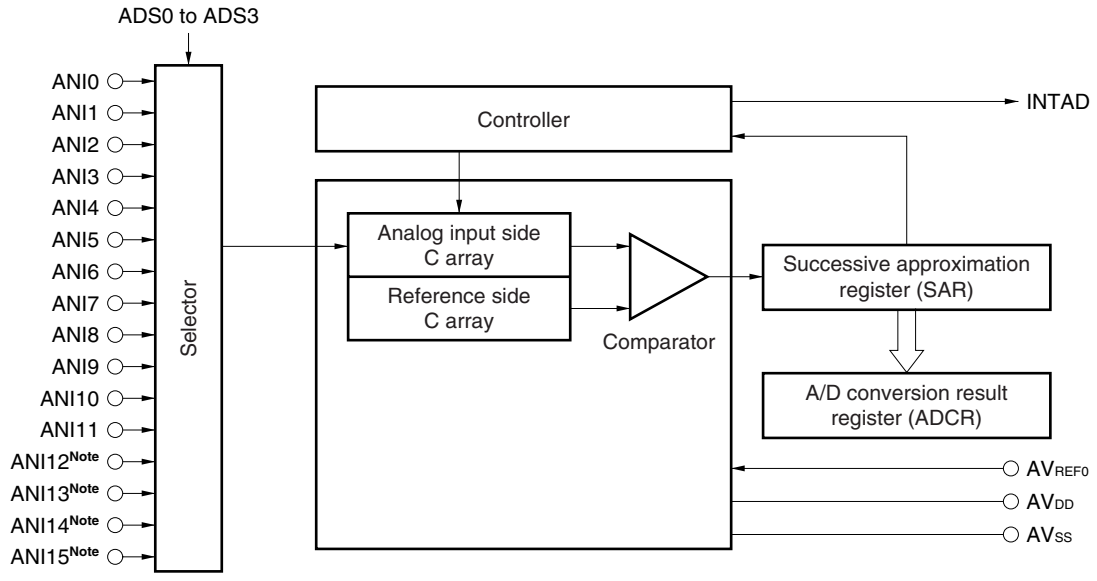
Remark fxx: Main clock frequency

13. A/D CONVERTER

The A/D converter has the following features.

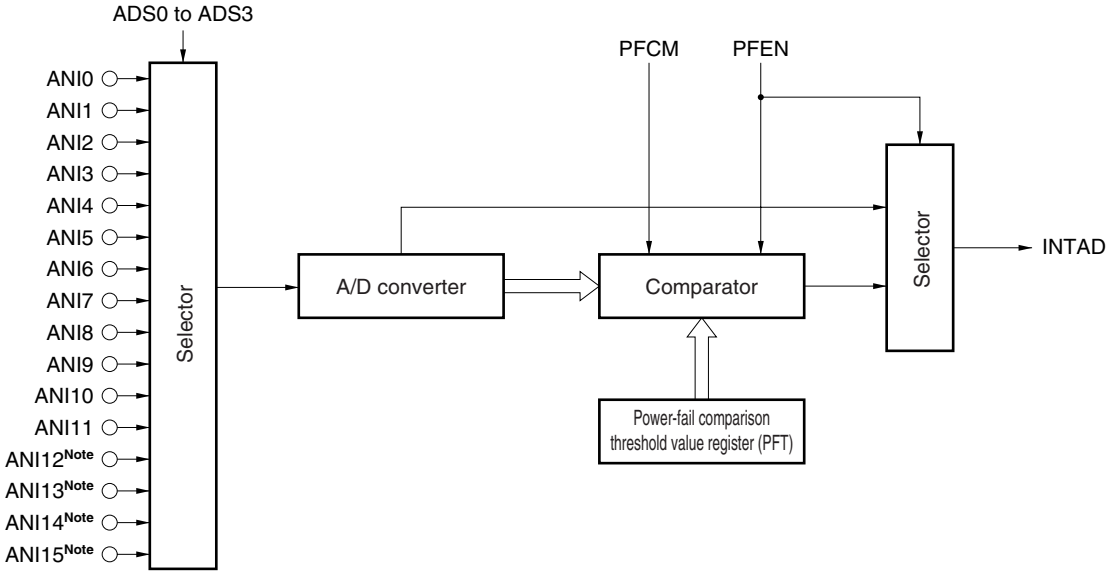
- 10-bit resolution
- 12 channels (V850ES/SA2)
  16 channels (V850ES/SA3)
- Successive comparison approximation method
- Power fail detection function available
- Operation voltage: $AV_{DD} = AV_{REF0}$ = 2.2 to 2.7 V
- Analog input voltage: AV_{SS} to AV_{REF0}
- Conversion rate: 9.5 to 1.50 μs

The following figure shows the configuration of the A/D converter.



Note V850ES/SA3 only

The following figure shows the configuration of the power fail detection function.



Note V850ES/SA3 only

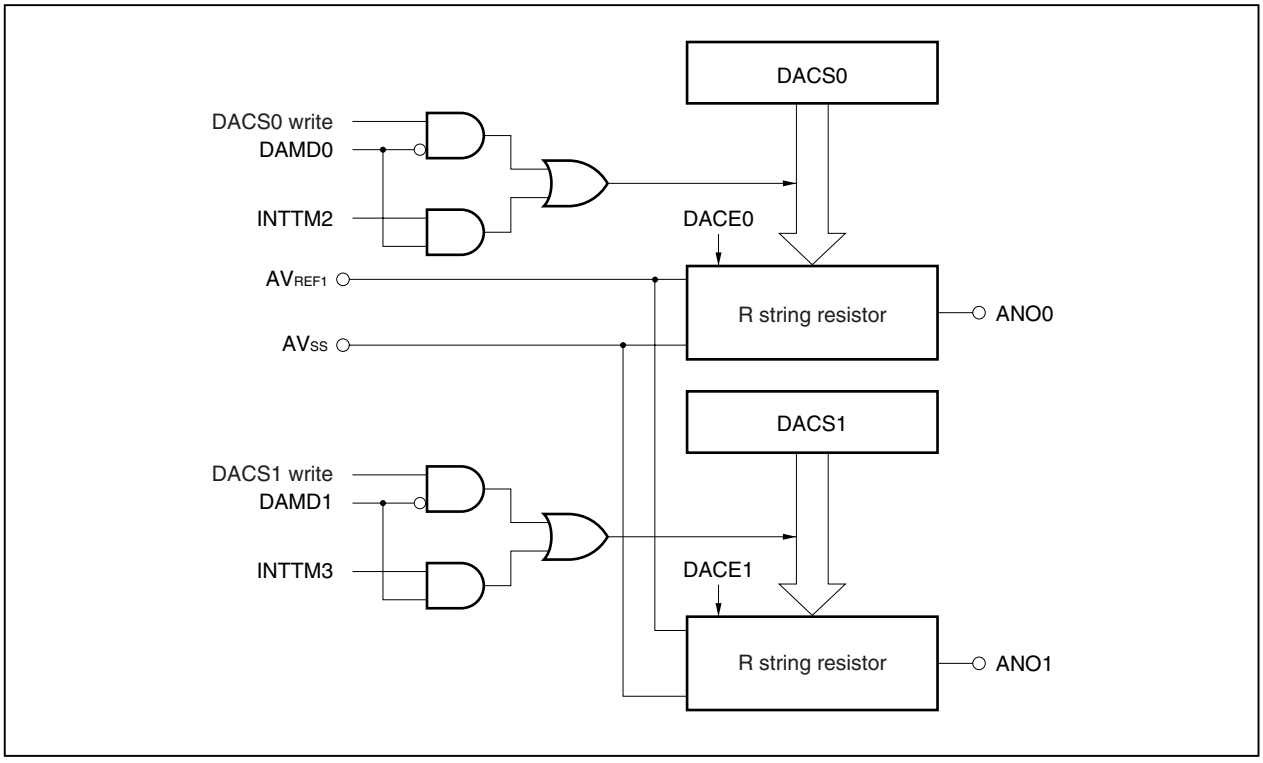
14. D/A CONVERTER

The D/A converter has the following features.

- 8-bit resolution × 2 channels (DAC0, DAC1)
- R string method
- Conversion time: 20 μs max. (AV_{REF1} = 2.2 to 2.7 V)
- Analog output voltage: AV_{REF1} × m/256 (m = 0 to 255; Value set in the DACSn register)
- Operation mode: Normal mode/real-time output mode

Remark n = 0, 1

The following figure shows the configuration of the D/A converter.



15. DMA FUNCTION

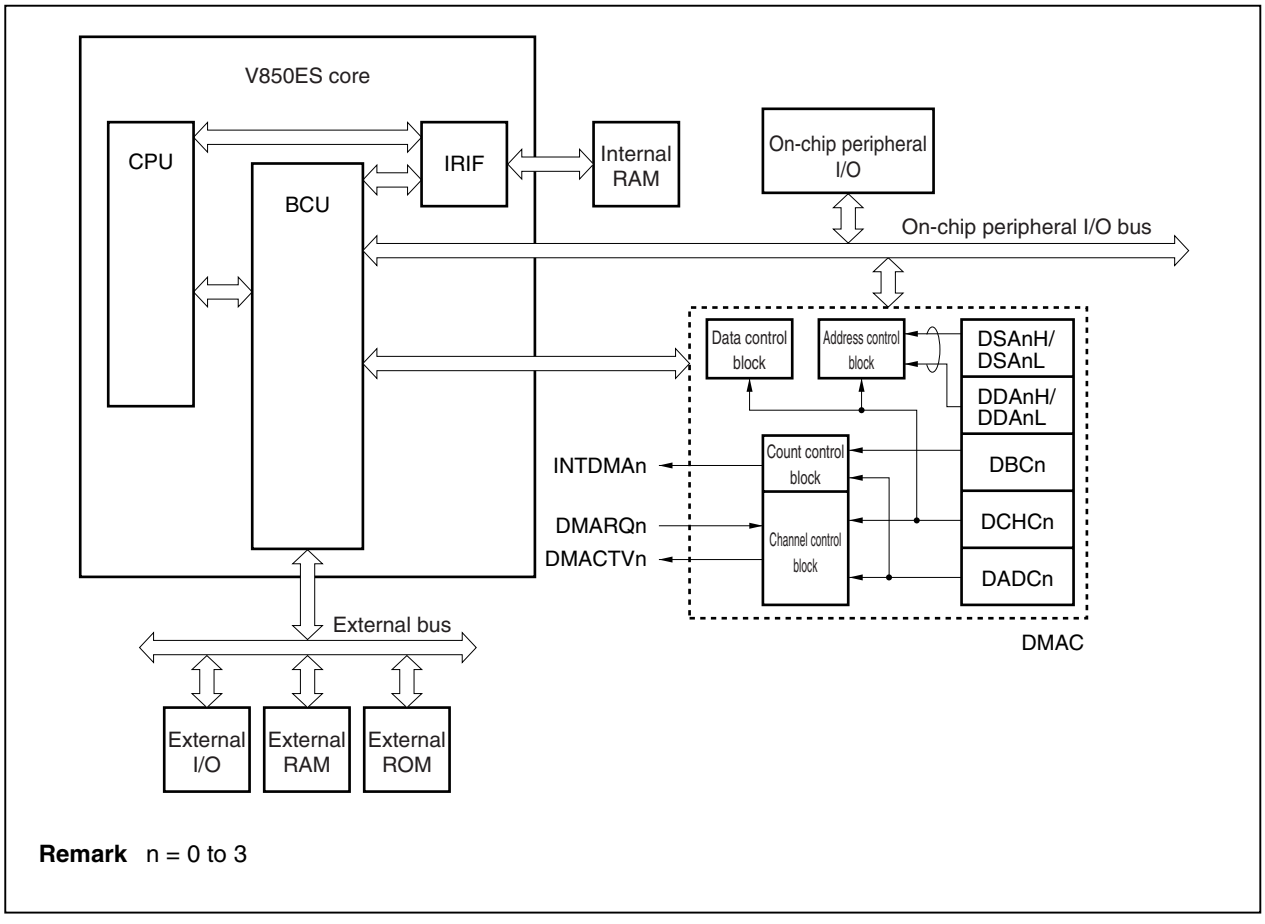
The DMA function has the following features.

- Transfer unit: 8 bits/16 bits
- Maximum transfer count: 65,536 (2^{16}) times
- Transfer type: 2-cycle transfer
- Transfer mode: Single transfer
- Transfer request: Request via interrupt from on-chip peripheral I/O or external pins, request via software trigger
- Transfer object: On-chip peripheral I/O, internal RAM, external memory

The relationship between the transfer type and transfer object is shown below (√: Transfer enabled, ×: Transfer disabled).

Transfer Source \ Transfer Destination	On-Chip Peripheral I/O	Internal RAM	External Memory
On-chip peripheral I/O	√	√	√
Internal RAM	√	×	√
External memory	√	√	√

The following figure shows the configuration of the DMA function.



Remark n = 0 to 3

16. ROM CORRECTION FUNCTION

The ROM correction function is a function that replaces part of a program in the mask ROM with a program in the internal RAM for execution.

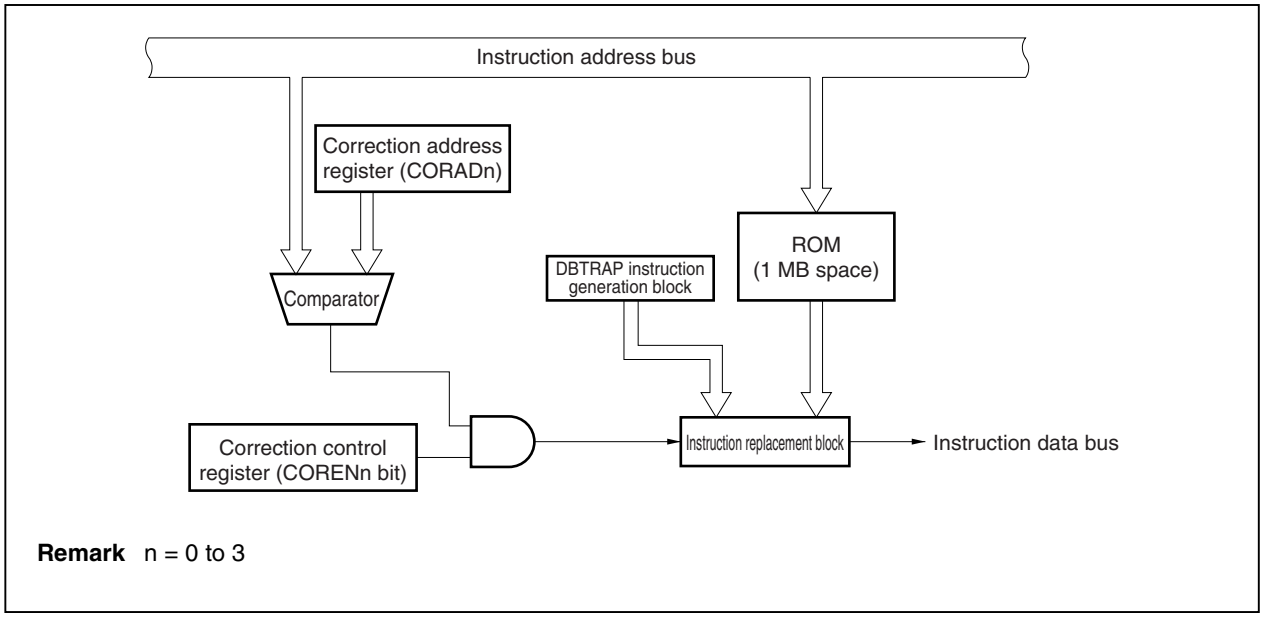
First, the address where the program replacement should start (correction address) is set in the correction address register (CORADn). When the CPU reads the instruction of the address set in CORADn, the instruction is replaced with the DBTRAP instruction and the program jumps to 00000060H.

A value that is the address saved in the DBPC minus 2 (address to which ROM correction generated) is compared with the address set in CORADn, and the program jumps to the correction program on the corresponding RAM. After executing the correction program, a restore address is set in the DBPC, the DBRET instruction is executed, and then execution is restored to the normal program.

Up to four correction addresses can be specified in CORADn.

Remark n = 3

The following figure shows the configuration of ROM correction.



Remark n = 0 to 3

17. RESET FUNCTION

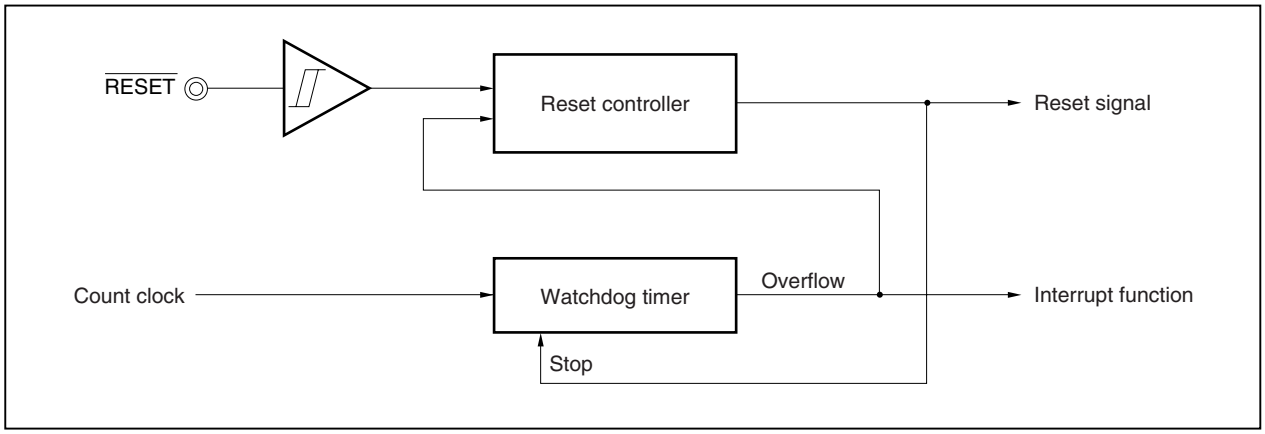
When a low-level signal is input to the $\overline{\text{RESET}}$ pin or the watchdog timer overflows (WDTRES), a system reset is applied and the various on-chip hardware devices are reset to their initial states.

When the $\overline{\text{RESET}}$ pin goes from low level to high level, or when the WDTRES signal is automatically canceled, the reset state is released.

When reset is released via $\overline{\text{RESET}}$ pin input, the CPU starts execution of the program after securing the oscillation stabilization time (OSTS register reset value: $2^{19}/f_{XX}$).

When reset is released by the WDTRES signal, the main clock oscillator does not stop and oscillation stabilization time is not inserted.

The following figure shows the configuration of the reset function.



18. FLASH MEMORY (μPD70F3201, 70F3201Y, 70F3204, 70F3204Y)

The μPD70F3201 and 70F3201Y, and 70F3204 and 70F3204Y are the flash memory versions of the V850ES/SA2 and V850ES/SA3, respectively, and incorporate 256 KB of flash memory.

Writing to flash memory can be performed while the device is mounted on the target system (on board). Writing is performed using a dedicated flash programmer connected to the target system or to a writing adapter.

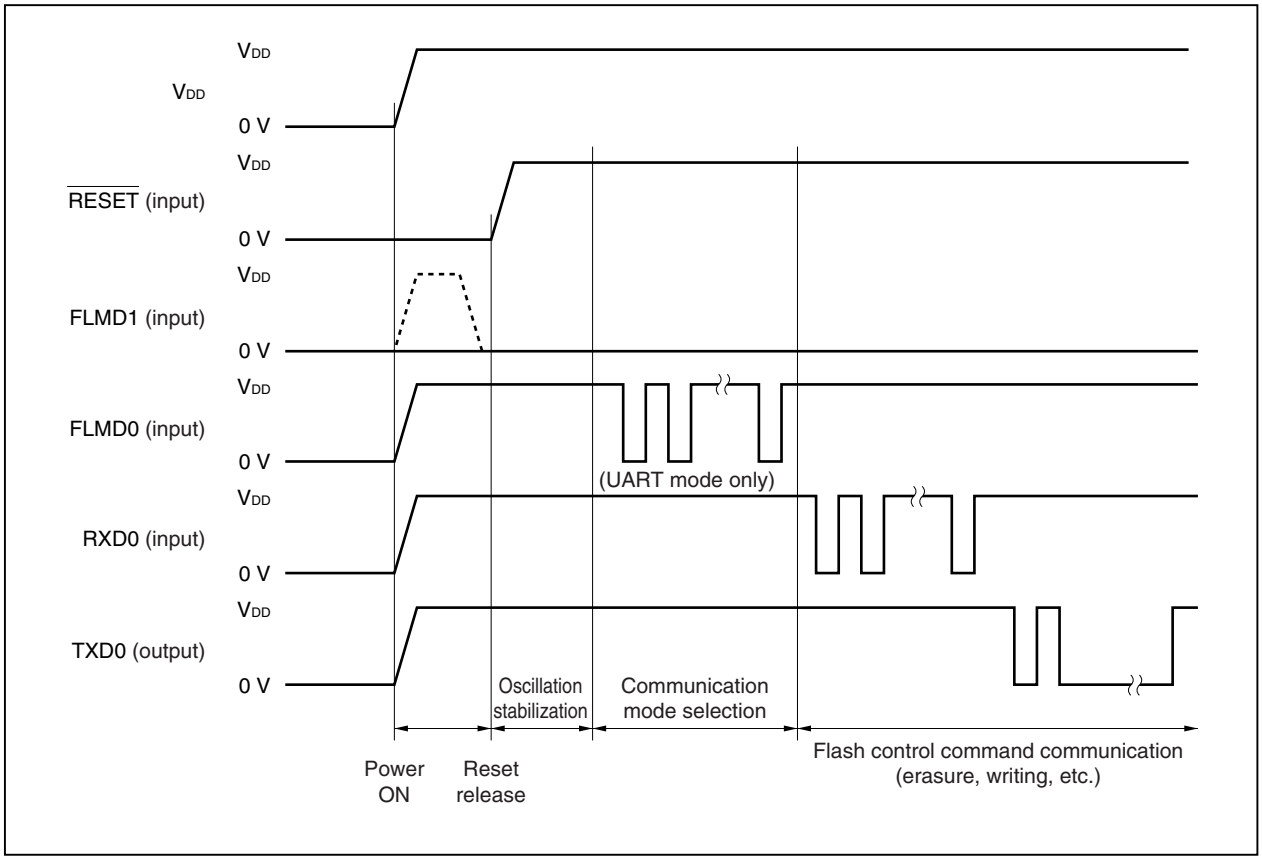
The flash memory has the following features.

- Flash memory: 256 KB (4 KB × 4 blocks, 60 KB × 4 blocks)
- Erasure/writing possible using single power supply (V_{DD} = 2.2 to 2.7 V)
- Erasure unit
  - Overall area batch erasure (256 KB)
  - Block units erasure (4 KB/block, 60 KB/block)
- Erasure/writing method
  - Serial mode (using CSI0 or UART0)
  - Self-programming mode

An overview of flash memory programming is shown below.

- Pins used in programming
  - Power supply pins (V_{DD}, EV_{DD}, AV_{DD}, V_{SS}, EV_{SS}, AV_{SS}, $V_{DD}BU$, $V_{SS}BU$)
  - Mode pins (FLMD0, FLMD1)
  - Clock supply pins (X1, X2)
  - Serial communication pins ($\overline{SCK0}$, SO0, SI0 or RXD0, TXD0)
  - $\overline{RESET}$ pin
- Programming timing

The following figure shows the programming timing (overview) when using UART.



19. INSTRUCTION SET LIST

19.1 Conventions

(1) Register symbols used to describe operands

Register Symbol	Explanation
reg1	General-purpose register: Used as source register.
reg2	General-purpose register: Used mainly as destination register. Also used as source register in some instructions.
reg3	General-purpose register: Used mainly to store the remainder of division results and the higher 32 bits of multiplication results.
bit#3	3-bit data for specifying the bit number
immX	X bit immediate data
dispX	X bit displacement data
regID	System register number
vector	5-bit data that specifies the trap vector (00H to 1FH)
cccc	4-bit data that shows the condition code
sp	Stack pointer (r3)
ep	Element pointer (r30)
listX	X item register list

(2) Register symbols used to describe opcodes

Register Symbol	Explanation
R	1-bit data of the code that specifies reg1 or regID
r	1-bit data of the code that specifies reg2
w	1-bit data of the code that specifies reg3
d	1-bit displacement data
I	1-bit immediate data (indicates the higher bits of immediate data)
i	1-bit immediate data
cccc	4-bit data that shows the condition codes
CCCC	4-bit data that shows the condition codes of the Bcond instruction
bbb	3-bit data for specifying the bit number
L	1-bit data that specifies a program register in the register list
S	1-bit data that specifies a system register in the register list

(3) Register symbols used in operation

Register Symbol	Explanation
←	Input for
GR [ ]	General-purpose register
SR [ ]	System register
zero-extend (n)	Expand n with zeros until word length.
sign-extend (n)	Expand n with signs until word length.
load-memory (a, b)	Read size b data from address a.
store-memory (a, b, c)	Write data b into address a in size c.
load-memory-bit (a, b)	Read bit b of address a.
store-memory-bit (a, b, c)	Write c to bit b of address a.
saturated (n)	Execute saturated processing of n (n is a 2's complement). If, as a result of calculations, n ≥ 7FFFFFFFH, let it be 7FFFFFFFH. n ≤ 80000000H, let it be 80000000H.
result	Reflects the results in a flag.
Byte	Byte (8 bits)
Half-word	Halfword (16 bits)
Word	Word (32 bits)
+	Addition
–	Subtraction
ll	Bit concatenation
×	Multiplication
÷	Division
%	Remainder from division results
AND	Logical product
OR	Logical sum
XOR	Exclusive OR
NOT	Logical negation
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

(4) Register symbols used in an execution clock

Register Symbol	Explanation
i	If executing another instruction immediately after executing the first instruction (issue).
r	If repeating execution of the same instruction immediately after executing the first instruction (repeat).
l	If using the results of instruction execution in the instruction immediately after the execution (latency).

(5) Register symbols used in flag operations

Identifier	Explanation
(Blank)	No change
0	Clear to 0
X	Set or cleared in accordance with the results.
R	Previously saved values are restored.

(6) Condition codes

Condition Name (cond)	Condition Code (cccc)	Condition Expression	Explanation
V	0 0 0 0	OV = 1	Overflow
NV	1 0 0 0	OV = 0	No overflow
C/L	0 0 0 1	CY = 1	Carry Lower (less than)
NC/NL	1 0 0 1	CY = 0	No carry Not lower (greater than or equal)
Z/E	0 0 1 0	Z = 1	Zero Equal
NZ/NE	1 0 1 0	Z = 0	Not zero Not equal
NH	0 0 1 1	(CY or Z) = 1	Not higher (less than or equal)
H	1 0 1 1	(CY or Z) = 0	Higher (greater than)
N	0 1 0 0	S = 1	Negative
P	1 1 0 0	S = 0	Positive
T	0 1 0 1	—	Always (unconditional)
SA	1 1 0 1	SAT = 1	Saturated
LT	0 1 1 0	(S xor OV) = 1	Less than signed
GE	1 1 1 0	(S xor OV) = 0	Greater than or equal signed
LE	0 1 1 1	((S xor OV) or Z) = 1	Less than or equal signed
GT	1 1 1 1	((S xor OV) or Z) = 0	Greater than signed

19.2 Instruction Set (In Alphabetical Order)

(1/6)

Mnemonic	Operand	Opcode	Operation		Execution Clock i	Execution Clock r	Execution Clock l	Flags CY	Flags OV	Flags S	Flags Z	Flags SAT
ADD	reg1,reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010010iiiii	GR[reg2]←GR[reg2]+sign-extend(imm5)		1	1	1	×	×	×	×	
ADDI	imm16,reg1,reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1	×	×	×	×	
AND	reg1,reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]		1	1	1		0	×	×	
ANDI	imm16,reg1,reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)		1	1	1		0	0	×	
Bcond	disp9	ddddd1011dddcccc **Note 1**	if conditions are satisfied then PC←PC+sign-extend(disp9)	When conditions are satisfied	2 Note 2	2 Note 2	2 Note 2					
				When conditions are not satisfied	1	1	1					
BSH	reg2,reg3	rrrrr11111100000 wwwww01101000010	GR[reg3]←GR[reg2] (23 : 16) ll GR[reg2] (31 : 24) ll GR[reg2] (7 : 0) ll GR[reg2] (15 : 8)		1	1	1	×	0	×	×	
BSW	reg2,reg3	rrrrr11111100000 wwwww01101000000	GR[reg3]←GR[reg2] (7 : 0) ll GR[reg2] (15 : 8) ll GR [reg2] (23 : 16) ll GR[reg2] (31 : 24)		1	1	1	×	0	×	×	
CALLT	imm6	0000001000iiiiii	CTPC←PC+2(return PC) CTPSW←PSW adr←CTBP+zero-extend(imm6 logically shift left by 1) PC←CTBP+zero-extend(Load-memory(adr,Half-word))		4	4	4					
CLR1	bit#3, disp16[reg1]	10bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,0)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100100	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,0)		3 Note 3	3 Note 3	3 Note 3				×	
CMOV	cccc,imm5,reg2,reg3	rrrrr111111iiiii wwwww011000cccc0	if conditions are satisfied then GR[reg3]←sign-extended(imm5) else GR[reg3]←GR[reg2]		1	1	1					
	cccc,reg1,reg2,reg3	rrrrr111111RRRR wwwww011001cccc0	if conditions are satisfied then GR[reg3]←GR[reg1] else GR[reg3]←GR[reg2]		1	1	1					
CMP	reg1,reg2	rrrrr001111RRRRR	result←GR[reg2]–GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010011iiiii	result←GR[reg2]–sign-extend(imm5)		1	1	1	×	×	×	×	
CTRET		0000011111100000 0000000101000100	PC←CTPC PSW←CTPSW		3	3	3	R	R	R	R	R
DBRET		0000011111100000 0000000101000110	PC←DBPC PSW←DBPSW		3	3	3	R	R	R	R	R

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DBTRAP		1111100001000000	DBPC←PC+2 (restored PC) DBPSW←PSW PSW.NP←1 PSW.EP←1 PSW.ID←1 PC←00000060H	3	3	3					
DI		0000011111100000 0000000101100000	PSW.ID←1	1	1	1					
DISPOSE	imm5,list12	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L L 0 0 0 0 0	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	imm5,list12,[reg1]	0 0 0 0 0 1 1 0 0 1 i i i i i L L L L L L L L L L L L R R R R R **Note 5**	sp←sp+zero-extend(imm5 logically shift left by 2) R[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded PC←GR[reg1]	n+3 Note 4	n+3 Note 4	n+3 Note 4					
DIV	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000000	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	35	35	35					
DIVH	reg1,reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1]Note 6	35	35	35		×	×	×	
	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000000	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVHU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000010	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
DIVU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000010	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
EI		1000011111100000 0000000101100000	PSW.ID←0	1	1	1					
HALT		0000011111100000 0000000100100000	Stop	1	1	1					
HSW	reg2,reg3	rrrrr11111100000 wwwww01101000100	GR[reg3]←GR[reg2](15 : 0) ll GR[reg2] (31 : 16)	1	1	1	×	0	×	×	
JARL	disp22,reg2	rrrrr11110ddddddd ddddddddddddddd0 **Note 7**	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)	2	2	2					
JMP	[reg1]	00000000011RRRRR	PC←GR[reg1]	3	3	3					
JR	disp22	0000011110ddddddd ddddddddddddddd0 **Note 7**	PC←PC+sign-extend(disp22)	2	2	2					
LD.B	disp16[reg1],reg2	rrrrr111000RRRRR ddddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 11					
LD.BU	disp16[reg1],reg2	rrrrr11110bRRRRR ddddddddddddddd1 **Notes 8, 10**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 11					

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Mnemonic	Operand	Opcode	Operation		Execution Clock			Flags				
					i	r	l	CY	OV	S	Z	SAT
LD.H	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Half-word))		1	1	Note 11					
LDSR	reg2,regID	rrrrr111111RRRRR 0000000000100000 **Note 12**	SR[regID]←GR[reg2]	Other than regID = PSW	1	1	1					
				regID = PSW	1	1	1	×	×	×	×	×
LD.HU	disp16[reg1],reg2	rrrrr111111RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-exend(disp16) GR[reg2]←zero-extend(Load-memory(adr,half-word)		1	1	Note 11					
LD.W	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-exend(disp16) GR[reg2]←Load-memory(adr,Word)		1	1	Note 11					
MOV	reg1,reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]		1	1	1					
	imm5,reg2	rrrrr010000iiiii	GR[reg2]←sign-extend(imm5)		1	1	1					
	imm32,reg1	00000110001RRRRR iiiiiiiiiiiiiiii iiiiiiiiiiiiiiii	GR[reg1]←imm32		2	2	2					
MOVEA	imm16,reg1,reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1					
MOVHI	imm16,reg1,reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+(imm16 ll 0^{16})		1	1	1					
MUL	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100000	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	4	5					
	imm9,reg2,reg3	rrrrr111111iiiii wwwww01001IIII00 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xsign-extend(imm9)		1	4	5					
MULH	reg1,reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2]Note 6xGR[reg1]Note 6		1	1	2					
	imm5,reg2	rrrrr010111iiiii	GR[reg2]←GR[reg2]Note 6xsign-extend(imm5)		1	1	2					
MULHI	imm16,reg1,reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]Note 6ximm16		1	1	2					
MULU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100010	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	4	5					
	imm9,reg2,reg3	rrrrr111111iiiii wwwww01001IIII10 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xzero-extend(imm9)		1	4	5					
NOP		0000000000000000	Pass at least one clock cycle doing nothing.		1	1	1					
NOT	reg1,reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])		1	1	1		0	×	×	
NOT1	bit#3,disp16[reg1]	01bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100010	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
OR	reg1,reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16,reg1,reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)	1	1	1		0	×	×	
PREPARE	list12,imm5	0000011110iiiiiL LLLLLLLLLLL00001	Store-memory(sp–4,GR[reg in list12],Word) sp←sp–4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5)	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	list12,imm5, sp/imm Note 14	0000011110iiiiiL LLLLLLLLLLLff011 imm16/imm32 **Note 15**	Store-memory(sp–4,GR[reg in list12],Word) sp←sp–4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5) ep←sp/imm	n+2 Note 4 Note 16	n+2 Note 4 Note 16	n+2 Note 4 Note 16					
RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP=1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	3	3	3	R	R	R	R	R
SAR	reg1,reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010101iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SASF	cccc,reg2	rrrrr1111110cccc 0000001000000000	if conditions are satisfied then GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000001H else GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000000H	1	1	1					
SATADD	reg1,reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	×	×	×	×	×
	imm5,reg2	rrrrr010001iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5)	1	1	1	×	×	×	×	×
SATSUB	reg1,reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16,reg1,reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16)	1	1	1	×	×	×	×	×
SATSUBR	reg1,reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc,reg2	rrrrr1111110cccc 0000000000000000	If conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 17**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 18**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Half-word))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 17, 19**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Half-word))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 20**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 18**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Half-word)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 20**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR ddddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Half-word)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	00000000010RRRRR	adr←(PC+2) + (GR [reg1] logically shift left by 1) PC←(PC+2) + (sign-extend (Load-memory (adr,Half-word))) logically shift left by 1	5	5	5					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SXB	reg1	00000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0))	1	1	1					
SXH	reg1	00000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	0 0 0 0 0 0 1 1 1 1 1 1 i i i i i 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	EIPC ←PC+4 (Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt Code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit (adr,bit#3))	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not (Load-memory-bit (adr,reg2))	3 Note 3	3 Note 3	3 Note 3				×	
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	00000000100RRRRR	GR[reg1]←zero-extend (GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	00000000110RRRRR	GR[reg1]←zero-extend (GR[reg1] (15 : 0))	1	1	1					

Notes 1. ddddddddd: Higher 8 bits of disp9.

2. 3 clocks if the final instruction includes the PSW write access.

3. If there is no wait state (3 + the number of read access wait states).

4. n is the total number of list X load registers. (According to the number of wait states. Also, if there are no wait states, n is the number of list X registers.)

5. RRRRR: Other than 00000.

6. The lower halfword data only is valid.

7. ddddddddddddddddddddd: The higher 21 bits of disp22.

8. ddddddddddddddd: The higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states).

10. b: Bit 0 of disp16.

11. According to the number of wait states (2 if there are no wait states).

12. In this instruction, for convenience of mnemonic description, the source register is made reg2, but the reg1 field is used in the opcode. Therefore, the meaning of register specification in the mnemonic description and in the opcode differs from other instructions.

rrrrr = regID specification

RRRRR = reg2 specification

13. iiiii: Lower 5 bits of imm9.

IIII: Lower 4 bits of imm9.

14. sp/imm: Specified by bits 19 and 20 of the sub-opcode.

Notes 15. ff = 00: Load sp in ep.
01: Load sign expanded 16-bit immediate data (bits 47 to 32) in ep.
10: Load 16-bit logically left shifted 16-bit immediate data (bits 47 to 32) in ep.
11: Load 32-bit immediate data (bits 63 to 32) in ep.

16. If imm = imm32, n + 3 clocks.

17. rrrrr : Other than 00000.

18. ddddddd: Higher 7 bits of disp8.

19. dddd: Higher 4 bits of disp5.

20. dddddd: Higher 6 bits of disp8.

20. ELECTRICAL SPECIFICATIONS (TARGET VALUES)

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +3.6	V
	AV_{DD}		–0.5 to +3.6	V
	EV_{DD}		–0.5 to +3.6	V
	$V_{DD}BU$		–0.5 to +3.6	V
	AV_{SS}		–0.5 to +0.5	V
	EV_{SS}		–0.5 to +0.5	V
	$V_{SS}BU$		–0.5 to +0.5	V
Input voltage	V_I	Other than X1, XT1, and port 7	–0.5 to EV_{DD} + 0.3[Note]	V
Clock input voltage	V_K	X1, V_{DD} = 2.2 to 2.7 V	–0.5 to V_{DD} + 0.3[Note]	V
	V_{KT}	XT1, $V_{DD}BU$ = 2.2 to 2.7 V	–0.5 to $V_{DD}BU$ + 0.3[Note]	V
Analog input voltage	V_{IAN}	Port 7	–0.5 to AV_{DD} + 0.3[Note]	V
Analog reference voltage	AV_{REF}	AV_{REF0}, AV_{REF1}	–0.5 to AV_{DD} + 0.3[Note]	V
Output current, low	I_{OL}	Per pin	4	mA
		Total for all pins	100	mA
Output current, high	I_{OH}	Per pin	–4	mA
		Total for all pins	–100	mA
Output voltage	V_O	V_{DD} = 2.5 V ±0.2 V	–0.5 to V_{DD} + 0.3 V	V
Operating ambient temperature	T_A	Normal operation mode	–40 to +85	°C
		Flash programming mode	T.B.D.	°C
Storage temperature	T_{stg}	μPD703201, 703201Y, 703204, 703204Y	–65 to +150	°C
		μPD70F3201, 70F3201Y, 70F3204, 70F3204Y	T.B.D.	°C

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fx = 1 MHz Unmeasured pins returned to 0 V			10	pF
I/O capacitance	C_{IO}				10	pF
Output capacitance	C_O				10	pF

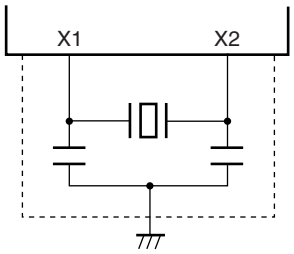
Operating Conditions (V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	@ V_{DD} = 2.3 to 2.7 V, operation with main clock	0.0625		17	MHz
		@ V_{DD} = 2.2 to 2.7 V, operation with main clock	0.0625		13.5	MHz

Recommended Oscillator

(1) Main clock oscillator (T_A = –40 to +85°C)

(a) Connection of ceramic resonator or crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_X (f_{XX})	V_{DD} = 2.3 to 2.7 V	2		17	MHz
		V_{DD} = 2.2 to 2.7 V	2		13.5	MHz
Oscillation stabilization time		Upon reset release		$2^{19}/f_X$		s
		Upon STOP mode release		**Note**		s

Note The TYP. value differs depending on the setting of the oscillation stabilization time select register (OSTS).

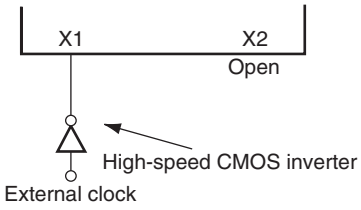
Caution Ensure that the duty of the oscillation waveform is between 45% and 55%.

Remarks 1. Connect the oscillator as close as possible to the X1 and X2 pins.

2. Do not route the wiring near broken lines.

3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

(b) External clock input

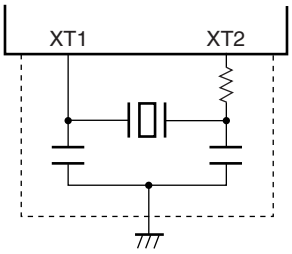


Cautions 1. Connect the high-speed CMOS inverter as close as possible to the X1 pin.

2. Sufficiently evaluate the matching between the V850ES/SA2, V850ES/SA3 and the high-speed CMOS inverter.

(2) Subclock oscillator (T_A = –40 to +85°C)

(a) Connection of crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}		32	32.768	35	kHz
Oscillation stabilization time				10		s

Caution Ensure that the duty of the oscillation waveform is between 45% and 55%.

Remarks 1. Connect the oscillator as close as possible to the XT1 and XT2 pins.

2. Do not route the wiring near broken lines.

3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = V_{DD}BU = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = V_{SS}BU = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**		0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	**Note 2**		T.B.D.		EV_{DD}	V
	V_{IH3}	**Note 3**		0.7AV_{DD}		AV_{DD}	V
	V_{IH4}	X1		0.8V_{DD}		V_{DD}	V
	V_{IH5}	XT1, XT2		0.8V_{DD}BU		V_{DD}BU	V
Input voltage, low	V_{IL1}	**Note 1**		EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	**Note 2**		EV_{SS}		T.B.D.	V
	V_{IL3}	**Note 3**		AV_{SS}		0.3AV_{DD}	V
	V_{IL4}	X1		V_{SS}		0.2V_{DD}	V
	V_{IL5}	XT1, XT2		V_{SS}BU		0.2V_{DD}BU	V
Output voltage, high	V_{OH1}	**Note 4**	I_{OH} = –1 mA	0.8EV_{DD}			V
	V_{OH2}	**Note 5**	I_{OH} = –3 mA	0.8EV_{DD}			V
Output voltage, low	V_{OL1}	**Note 4** (Except pins P40 and P42)	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	P40, P42	I_{OL} = 3 mA			0.4	V
	V_{OL3}	**Note 5**	I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD} = EV_{DD} = V_{DD}BU				5	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V				–5	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD} = EV_{DD} = V_{DD}BU				5	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–5	μA

Notes 1. P21, P31, P90, P91, P94 to P97, P99, P911, P914, PCD1 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15 (and their alternate-function pins)

2. $\overline{\text{RESET}}$, P00 to P05, P20, P22, P30, P32, P40 to P46, P92, P93, P98, P910, P912, P913, P915 (and their alternate-function pins)

3. P70 to P715, P80, P81 (and their alternate-function pins)

4. P00 to P05, P20 to P22, P30 to P32, P40 to P46, PCD1 to PCD3, PCM4 to PCM5, PCS4 to PCS7, PCT2, PCT3, PCT5, PCT7 (and their alternate-function pins)

5. P90 to P915, PCM0 to PCM3, PCS0 to PCS3, PCT0, PCT1, PCT4, PCT6, PDH0 to PDH7, PDL0 to PDL15 (and their alternate-function pins)

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V) (2/2)

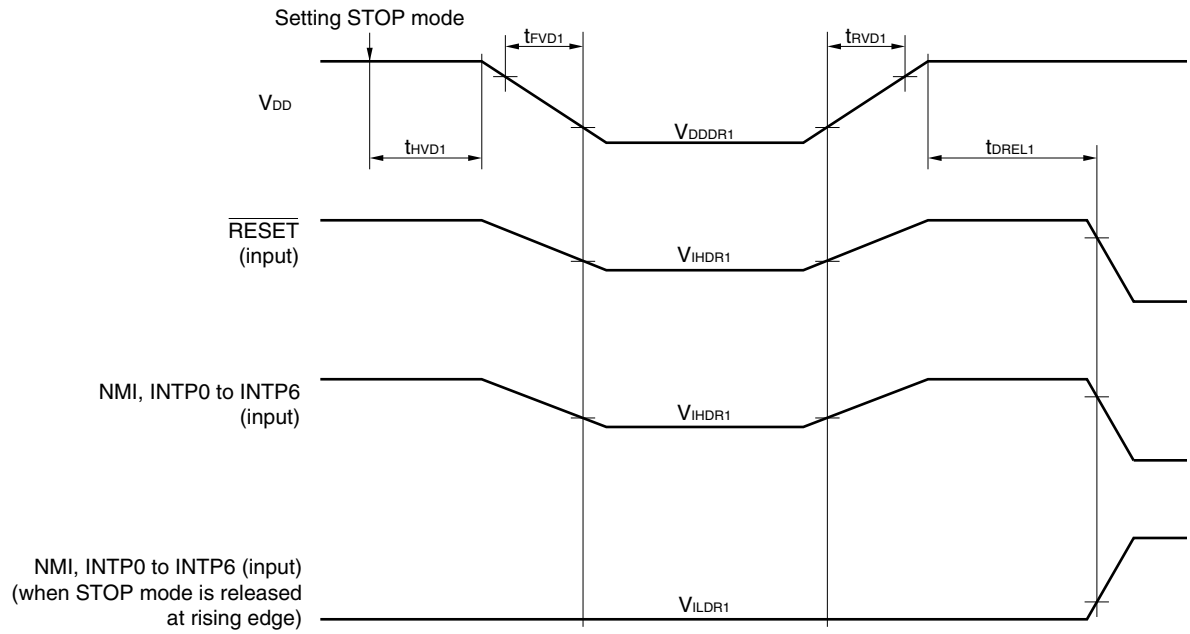
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	Normal operation All peripheral functions operating	V_{DD} = 2.3 to 2.7 V, f_{XX} = f_{CLK} = 17 MHz		T.B.D.	T.B.D.	mA
			f_{XX} = f_{CLK} = 13.5 MHz		T.B.D.	T.B.D.	mA
	I_{DD2}	HALT mode All peripheral functions operating	V_{DD} = 2.3 to 2.7 V, f_{XX} = f_{CLK} = 17 MHz		T.B.D.	T.B.D.	mA
			f_{XX} = f_{CLK} = 13.5 MHz		T.B.D.	T.B.D.	mA
	I_{DD3}	IDLE mode RTC operating	V_{DD} = 2.3 to 2.7 V, f_{XX} = f_{CLK} = 17 MHz		T.B.D.	T.B.D.	mA
			f_{XX} = f_{CLK} = 13.5 MHz		T.B.D.	T.B.D.	mA
	I_{DD4}	STOP mode	Subclock oscillator, RTC operating		T.B.D.	T.B.D.	μA
			Subclock oscillator stopped (XT1 = V_{SS})		T.B.D.	T.B.D.	μA
	I_{DD5}	Backup mode	f_{XT} = 32.768 kHz, RTC operating		T.B.D.	T.B.D.	μA
			Subclock oscillation stopped (XT1 = V_{SS})		T.B.D.	T.B.D.	μA
Pull-up resistance	R_L	V_{IN} = 0 V		10	30	100	kΩ

Data Retention Characteristics

(1) In STOP mode (T_A = –40 to +85°C, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR1}	STOP mode	1.8		2.7	V
Data retention current	I_{DDDR1}	V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = V_{DDDR1}		T.B.D.	T.B.D.	μA
Supply voltage rise time	t_{RVD1}		200			μs
Supply voltage fall time	t_{FVD1}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD1}		0			ms
STOP release signal input time	t_{DREL1}		0			ms
Data retention high-level input voltage	V_{IHDR1}	All input ports	V_{IHn}		V_{DDDR1}	V
Data retention low-level input voltage	V_{ILDR1}	All input ports	0		V_{ILn}	V

Remark n = 1 to 5

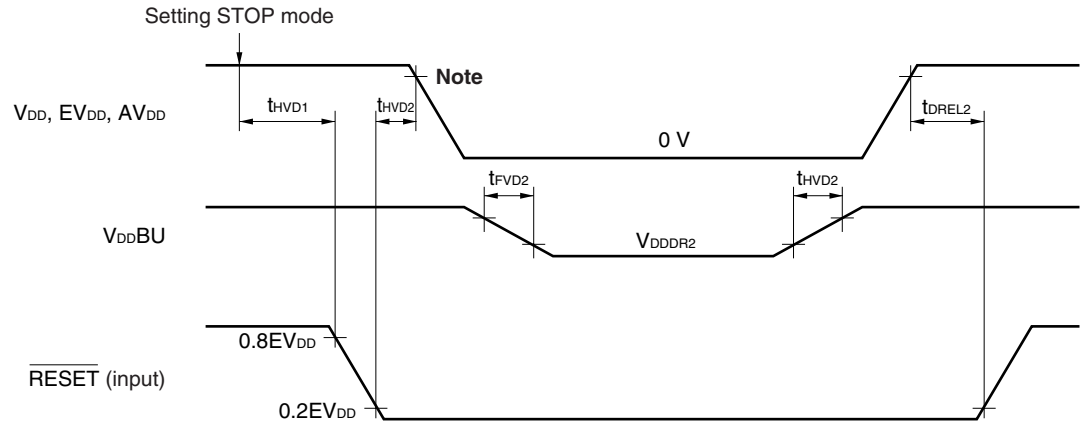


Caution Shifting to STOP mode and restoring from STOP mode must be performed at V_{DD} = 2.3 V min. (f_{CLK} = 17 MHz) and V_{DD} = 2.2 V min. (f_{CLK} = 13.5 MHz), respectively.

(2) In backup mode (T_A = –40 to +85°C, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = V_{DD} = AV_{DD} = EV_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR2}	Backup mode	1.6		2.7	V
Data retention current	I_{DDDR2}	$V_{DD}BU$ = V_{DDDR2}		T.B.D.	T.B.D.	μA
Backup supply voltage rise time	t_{RVD2}		T.B.D.			μs
Backup supply voltage fall time	t_{FVD2}		T.B.D.			μs
Mode setting time from $\overline{RESET}$↓ to V_{DD}↓	t_{HVD2}		T.B.D.			ms
Mode release signal input time from V_{DD}↑ to $\overline{RESET}$↑	t_{DREL2}		T.B.D.			ms

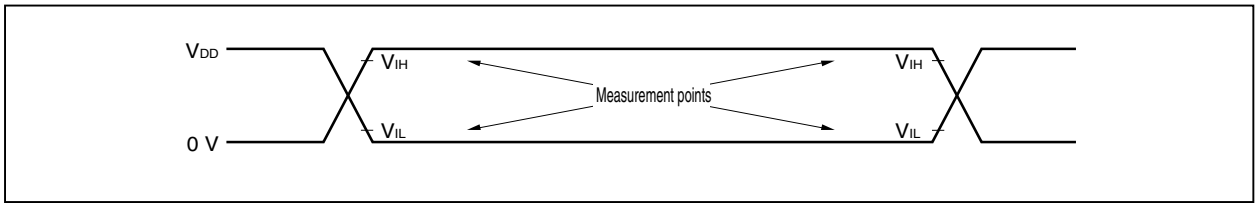
Caution Shifting to backup mode and restoring from backup mode must be performed at V_{DD} = 2.3 V min. (f_{CLK} = 17 MHz) and V_{DD} = 2.2 V min. (f_{CLK} = 13.5 MHz), respectively.



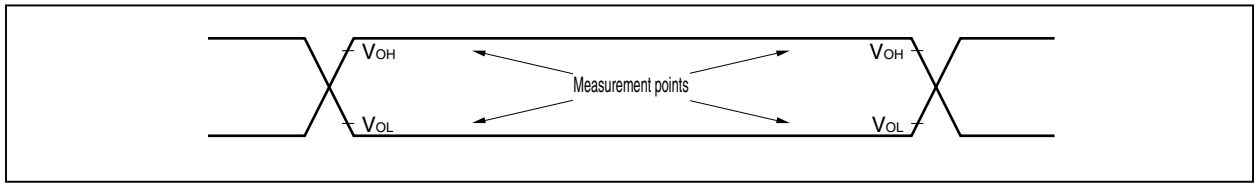
Note Shifting to backup mode and restoring from backup mode must be performed at V_{DD} = 2.3 V min. (f_{CLK} = 17 MHz) and V_{DD} = 2.2 V min. (f_{CLK} = 13.5 MHz), respectively.

AC Characteristics

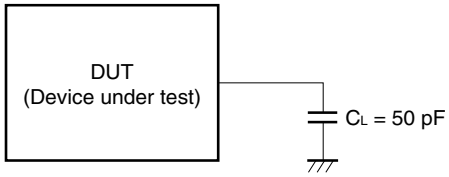
AC test input measurement points (V_{DD}, AV_{DD}, EV_{DD}, $V_{DD}BU$)



AC test output measurement points



Load conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, reduce the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

Clock Timing

(1) Operating conditions (T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.3 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		58.8		ns
XT1 input cycle				28.5		μs
X1 input high-level width	t_{WXH}	<2>		26.4		ns
XT1 input high-level width				12.8		μs
X1 input low-level width	t_{WXL}	<3>		26.4		ns
XT1 input low-level width				12.8		μs
X1 input rise time	t_{XR}	<4>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
X1 input fall time	t_{XF}	<5>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
CLKOUT output cycle	t_{CYK}	<6>		58.8 ns	16 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.5t_{CYK} – 5		ns
CLKOUT low-level width	t_{WKL}	<8>		0.5t_{CYK} – 5		ns
CLKOUT rise time	t_{KR}	<9>			5	ns
CLKOUT fall time	t_{KF}	<10>			5	ns

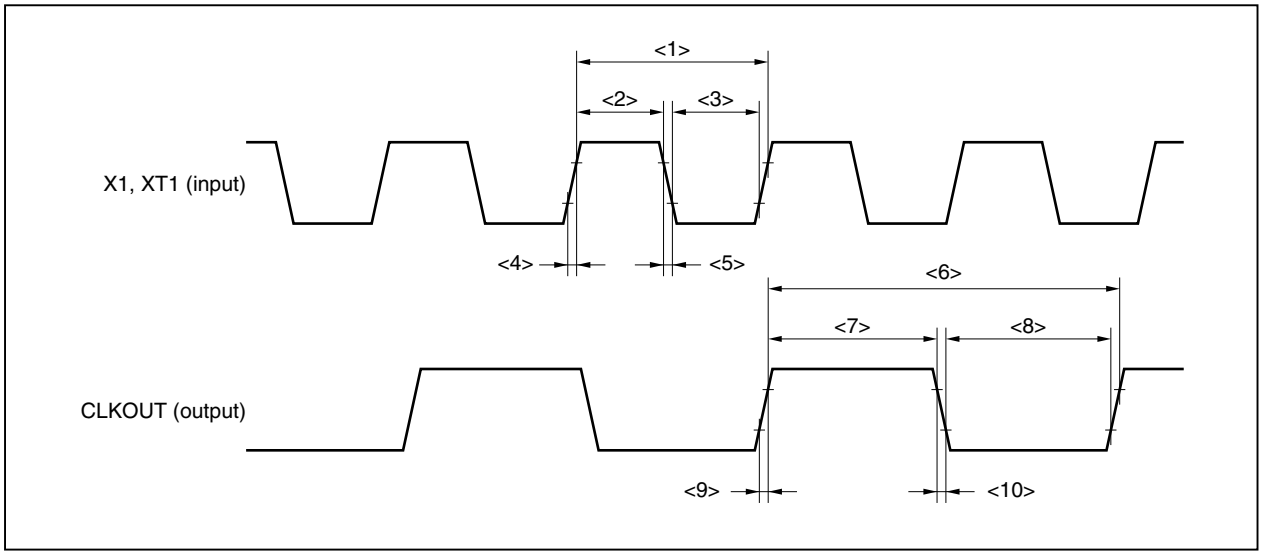
Remark Ensure that the duty for the X1 and XT1 input waveforms is between 45% and 55%.

(2) Operating conditions (T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		T.B.D.		ns
XT1 input cycle				T.B.D.		μs
X1 input high-level width	t_{WXH}	<2>		T.B.D.		ns
XT1 input high-level width				T.B.D.		μs
X1 input low-level width	t_{WXL}	<3>		T.B.D.		ns
XT1 input low-level width				T.B.D.		μs
X1 input rise time	t_{XR}	<4>			T.B.D.	ns
X1 input fall time	t_{XF}	<5>			T.B.D.	ns
CLKOUT output cycle	t_{CYK}	<6>		T.B.D.	T.B.D.	
CLKOUT high-level width	t_{WKH}	<7>		T.B.D.		ns
CLKOUT low-level width	t_{WKL}	<8>		T.B.D.		ns
CLKOUT rise time	t_{KR}	<9>			T.B.D.	ns
CLKOUT fall time	t_{KF}	<10>			T.B.D.	ns

Remark Ensure that the duty for the X1 and XT1 input waveforms is between 45% and 55%.

Clock timing



Bus Timing

(1) Multiplexed bus mode

(a) CLKOUT asynchronous: In multiplexed bus mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<11>		0.5T – 15		ns
Address hold time (from ASTB↓)	t_{HSTA}	<12>		0.5T – 15		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}	<13>			2	ns
Data input setup time from address	t_{SAID}	<14>			(2 + n)T – 25	ns
Data input setup time from $\overline{RD}$↓	t_{SRID}	<15>			(1 + n)T – 25	ns
Delay time from ASTB↓ to $\overline{RD}$↓, $\overline{WRm}$↓	$t_{DSTRDWR}$	<16>		0.5T – 15		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}	<17>		0		ns
Address output time from RD↑	t_{DRDA}	<18>		(1 + i)T – 15		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$	<19>		0.5T – 15		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}	<20>		(1.5 + i)T – 15		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}	<21>		(1 + n)T – 15		ns
ASTB high-level width	t_{WSTH}	<22>		T – 15		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}	<23>			15	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}	<24>		(1 + n)T – 20		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}	<25>		T – 15		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<26>	n ≥ 1		1.5T – 25	ns
	t_{SAWT2}	<27>	n ≥ 1		(1.5 + n)T – 25	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<28>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<29>	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<30>	n ≥ 1		T – 25	ns
	t_{SSTWT2}	<31>	n ≥ 1		(1 + n)T – 25	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<32>	n ≥ 1	nT		ns
	t_{HSTWT2}	<33>	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<34>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<35>		T – 15		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}	<36>		–3		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}	<37>		1.5T	(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}	<38>		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after the read cycle (0 or 1).

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(b) CLKOUT synchronous: In multiplexed bus mode

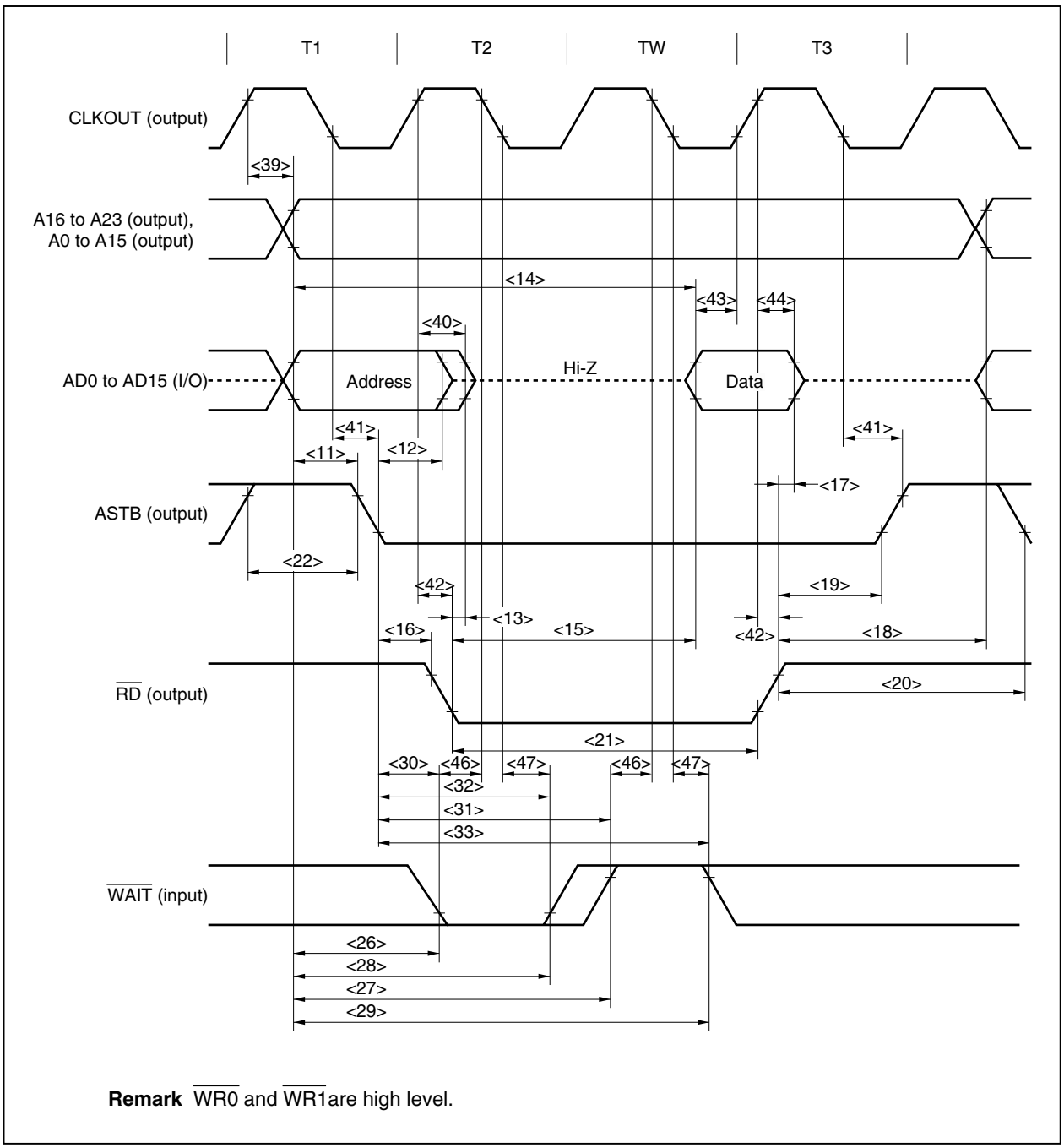
(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<39>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<40>		–12	7	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<41>		–12	7	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}	<42>		–5	14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<43>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<44>		5		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<45>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<46>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<47>		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}	<48>		15		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}	<49>		5		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<50>			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}	<51>			19	ns

Remarks 1. m = 0, 1

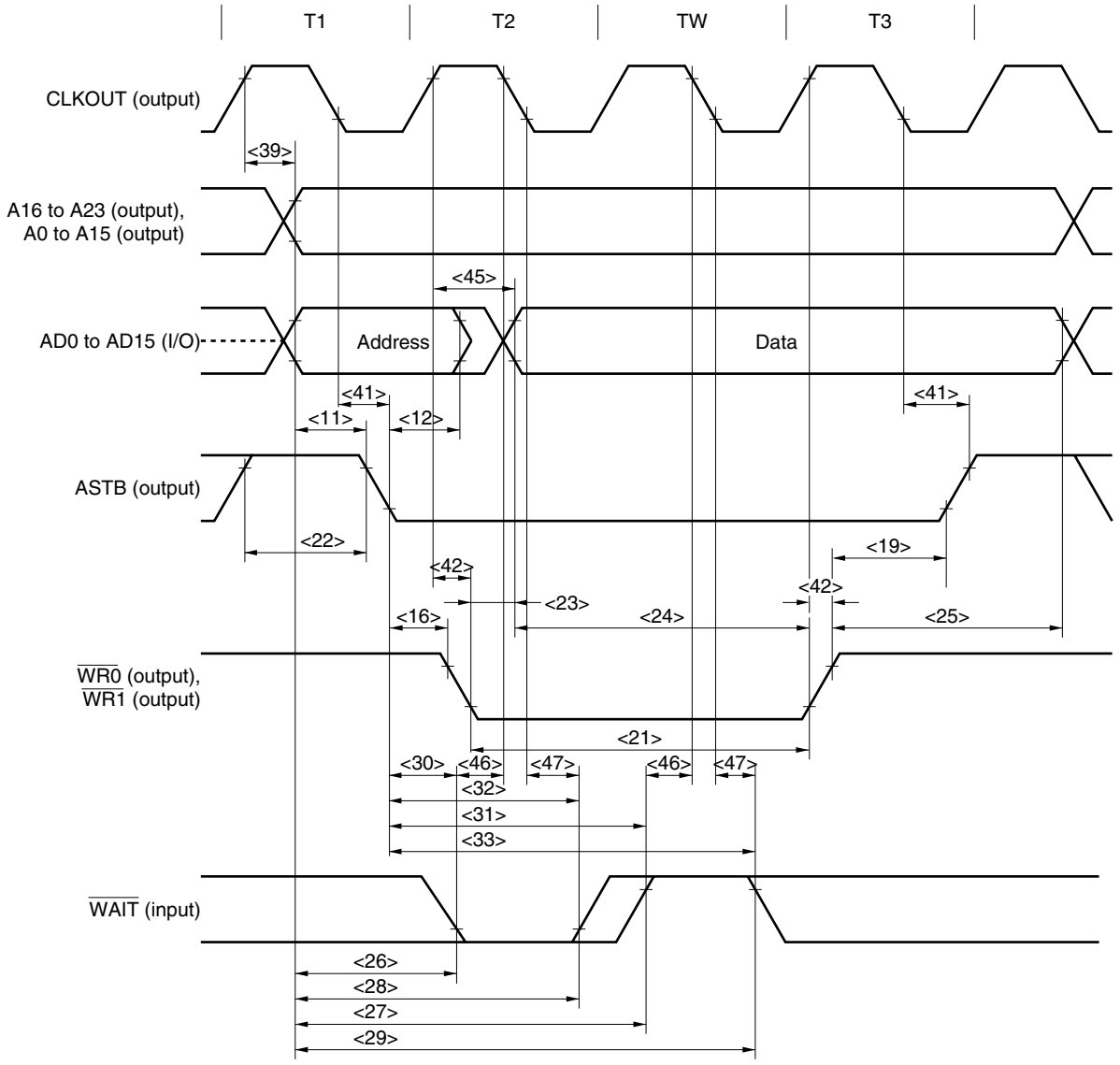
2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplexed Bus Mode



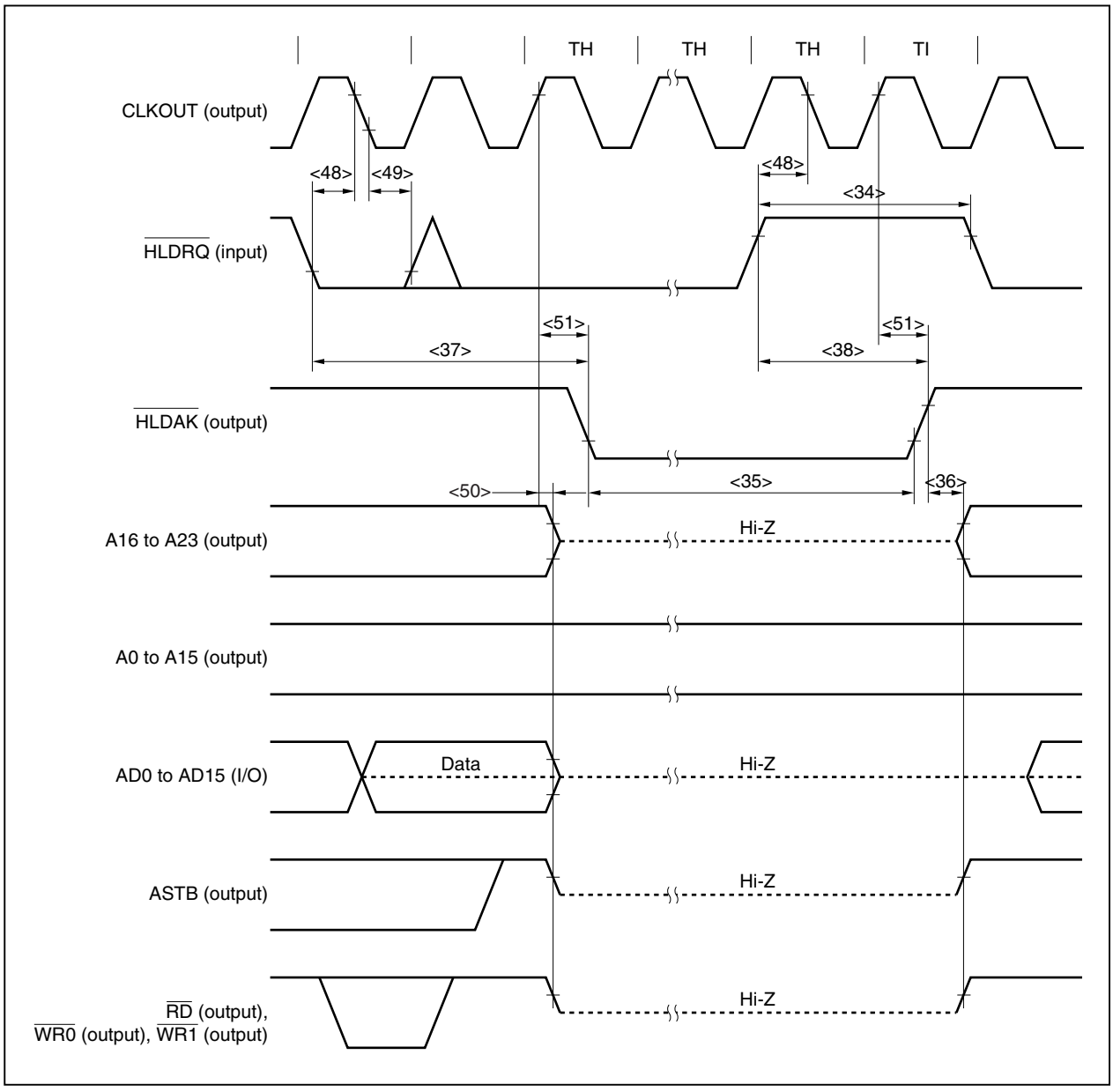
Remark $\overline{WR0}$ and $\overline{WR1}$are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplexed Bus Mode



Remark $\overline{RD}$ is high level.

Bus Hold: In Multiplexed Bus Mode



(2) In separate bus mode

(a) Read cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{RD}\downarrow$)	t_{SARD}	<52>		0.5T – 15		ns
Address hold time (from $\overline{RD}\uparrow$)	t_{HARD}	<53>		2		ns
$\overline{RD}$ low-level width	t_{WRDL}	<54>		(1.5 + n) T – 10		ns
Data setup time (to $\overline{RD}\uparrow$)	t_{SISD}	<55>		20		ns
Data hold time (from $\overline{RD}\uparrow$)	t_{HISD}	<56>		0		ns
Data setup time (to address)	t_{SAID}	<57>			(2 + n) T – 25	ns
$\overline{WAIT}$ setup time (to $\overline{RD}\downarrow$)	t_{SRDWT1}	<58>			0.5T – 20	ns
	t_{SRDWT2}	<59>			(0.5 + n) T – 20	ns
$\overline{WAIT}$ hold time (from $\overline{RD}\downarrow$)	t_{HRDWT1}	<60>		0.5T		ns
	t_{HRDWT2}	<61>		(0.5 + n) T		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<62>			T – 20	ns
	t_{SAWT2}	<63>			(1 + n) T – 20	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<64>		T		ns
	t_{HAWT2}	<65>		(1 + n) T		ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

2. n: Number of wait clocks inserted in bus cycle
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are the values for when clocks with a 1:1 duty ratio are input from X1.

(b) Read cycle (CLKOUT synchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT$\uparrow$ to address, CS	t_{DKSA}	<66>		0	19	ns
Data input setup time (to CLKOUT$\uparrow$)	t_{SISDK}	<67>		15		ns
Data input hold time (from CLKOUT$\uparrow$)	t_{HKISD}	<68>		5		ns
Delay time from CLKOUT$\downarrow\uparrow$ to $\overline{RD}$	t_{DKSR}	<69>		0	19	ns
$\overline{WAIT}$ setup time (to CLKOUT$\uparrow$)	t_{SWTK}	<70>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT$\uparrow$)	t_{HKWT}	<71>		5		ns

Remark The values in the above specifications are the values for when clocks with a 1:1 duty ratio are input from X1.

(c) Write cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{WRm}$↓)	t_{SAW}	<72>		T – 15		ns
Address hold time (from $\overline{WRm}$↑)	t_{HAW}	<73>		0.5T – 10		ns
$\overline{WRm}$ low-level width	t_{WWRL}	<74>		(0.5 + n) T – 10		ns
Data output time from $\overline{WRm}$↓	t_{DOSDW}	<75>		–5		ns
Data setup time (to $\overline{WRm}$↑)	t_{SOSDW}	<76>		(0.5 + n) T – 10		ns
Data hold time (from $\overline{WRm}$↑)	t_{HOSDW}	<77>		0.5T – 10		ns
Data setup time (to address)	t_{SAOD}	<78>		T – 25		ns
$\overline{WAIT}$ setup time (to $\overline{WRm}$↓)	t_{SWRWT1}	<79>		20		ns
	t_{SWRWT2}	<80>		nT – 20		ns
$\overline{WAIT}$ hold time (from $\overline{WRm}$↓)	t_{HWRWT1}	<81>		0		ns
	t_{HWRWT2}	<82>		nT		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<83>			T – 20	ns
	t_{SAWT2}	<84>			(1 + n) T – 20	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<85>		T		ns
	t_{HAWT2}	<86>		(1 + n) T		ns

Remarks 1. m = 0, 1

2. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

3. n: Number of wait clocks inserted in bus cycle
The sampling timing changes when a programmable wait is inserted.

4. The values in the above specifications are the values for when clocks with a 1:1 duty ratio are input from X1.

(d) Write cycle (CLKOUT synchronous): In separate bus mode

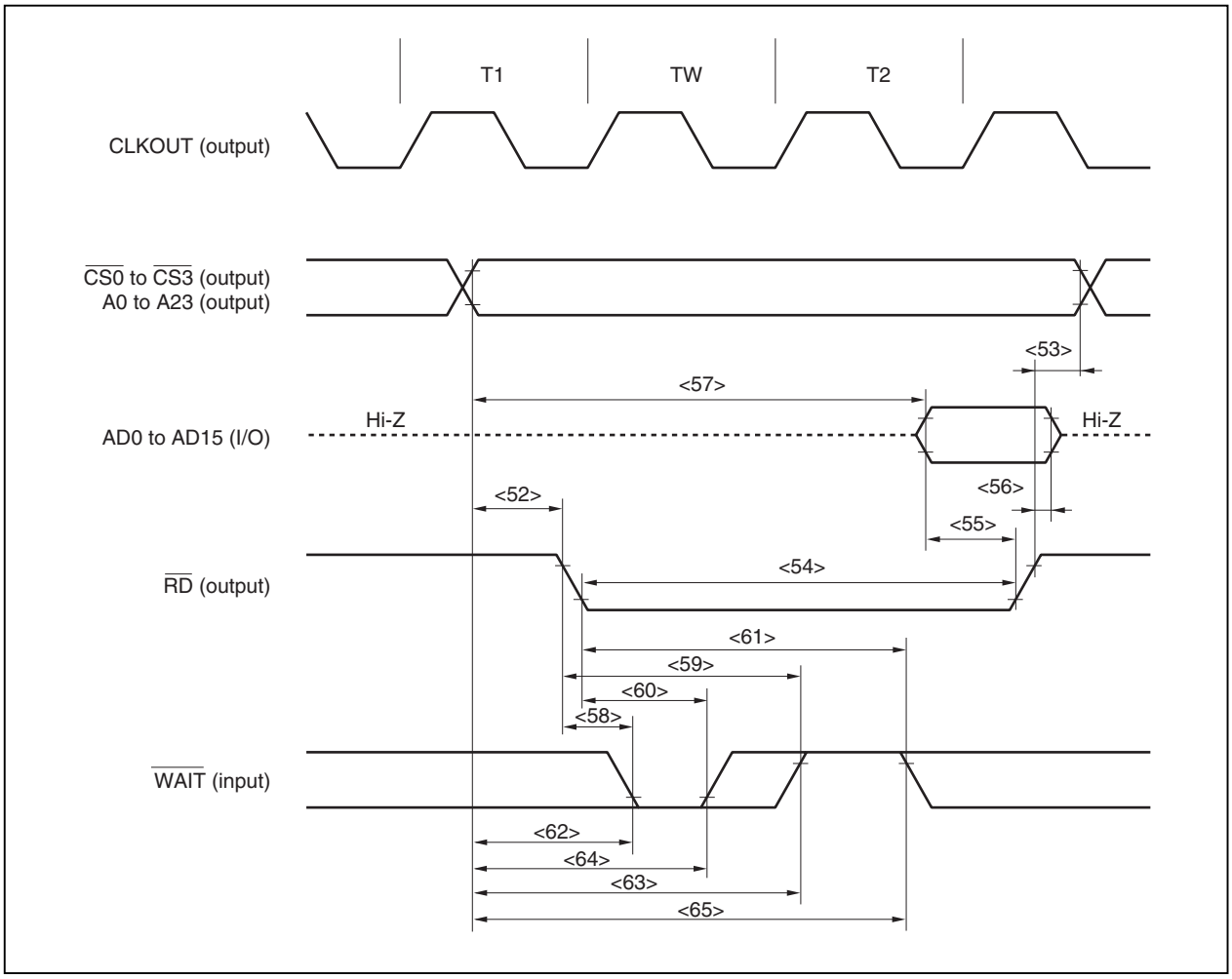
(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<87>		0	19	ns
Delay time from CLKOUT↑ to data output	t_{DKSD}	<88>		0	19	ns
Delay time from CLKOUT↑↓ to $\overline{WRm}$	t_{DKSW}	<89>		0	19	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<90>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<91>		5		ns

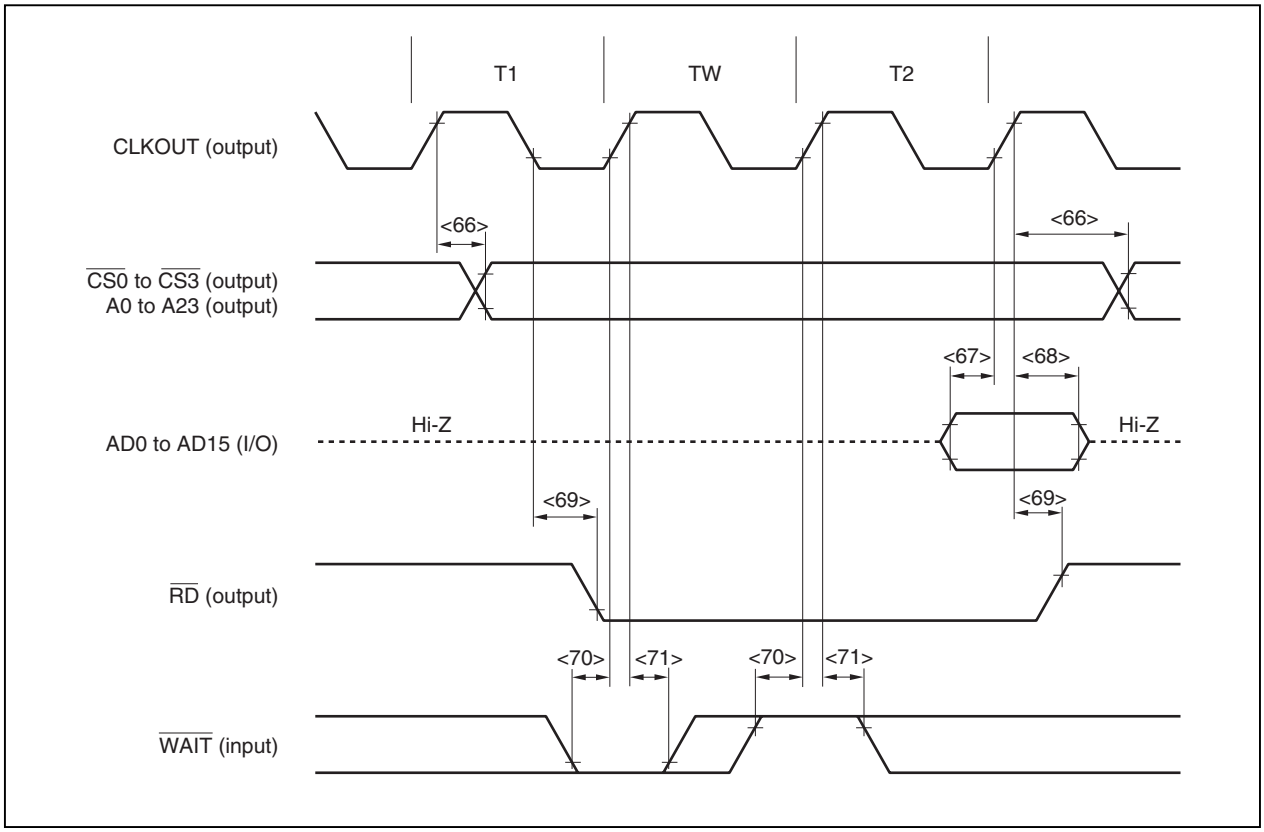
Remarks 1. m = 0, 1

2. The values in the above specifications are the values for when clocks with a 1:1 duty ratio are input from X1.

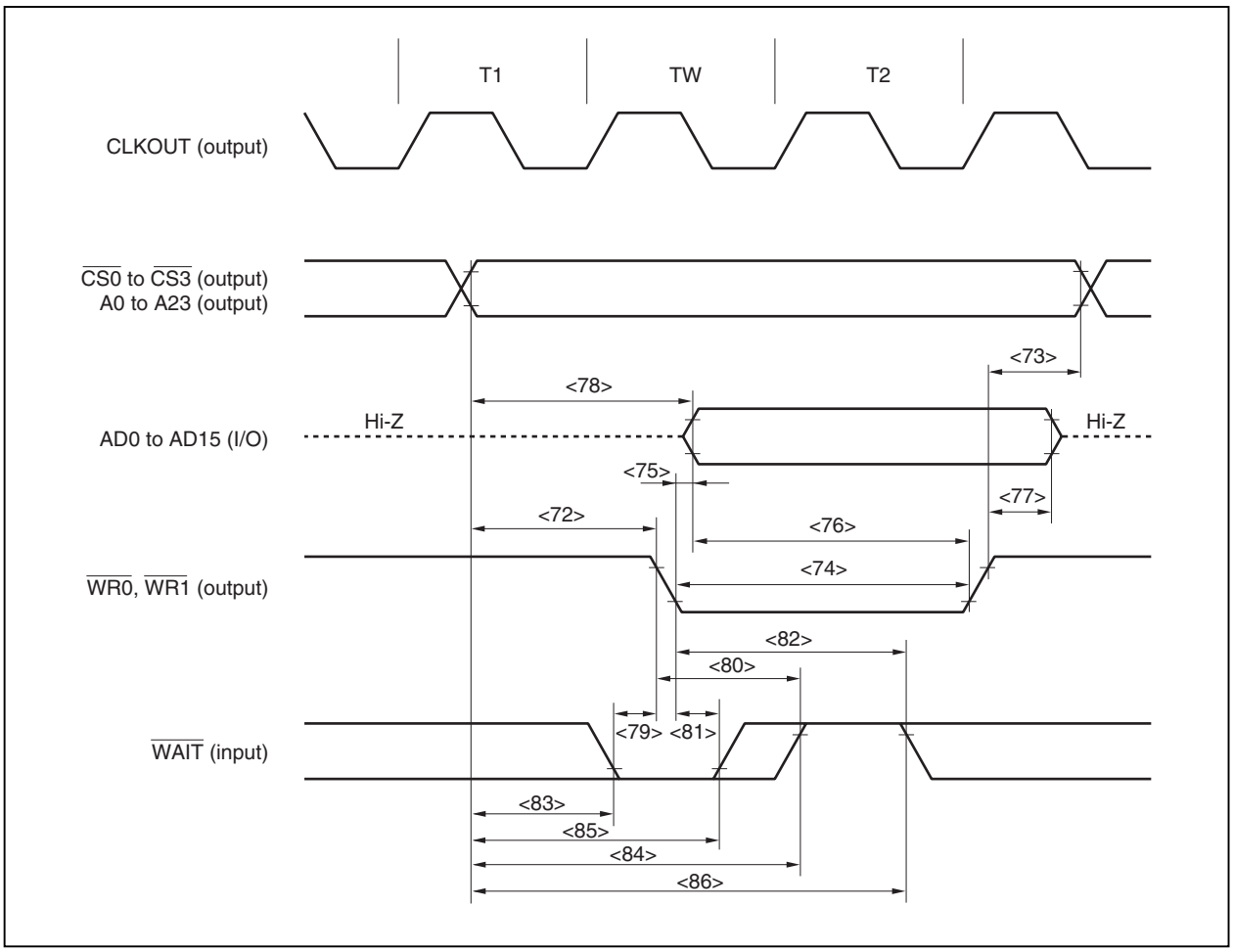
Read Cycle (CLKOUT Asynchronous, 1 Wait): In Separate Bus Mode



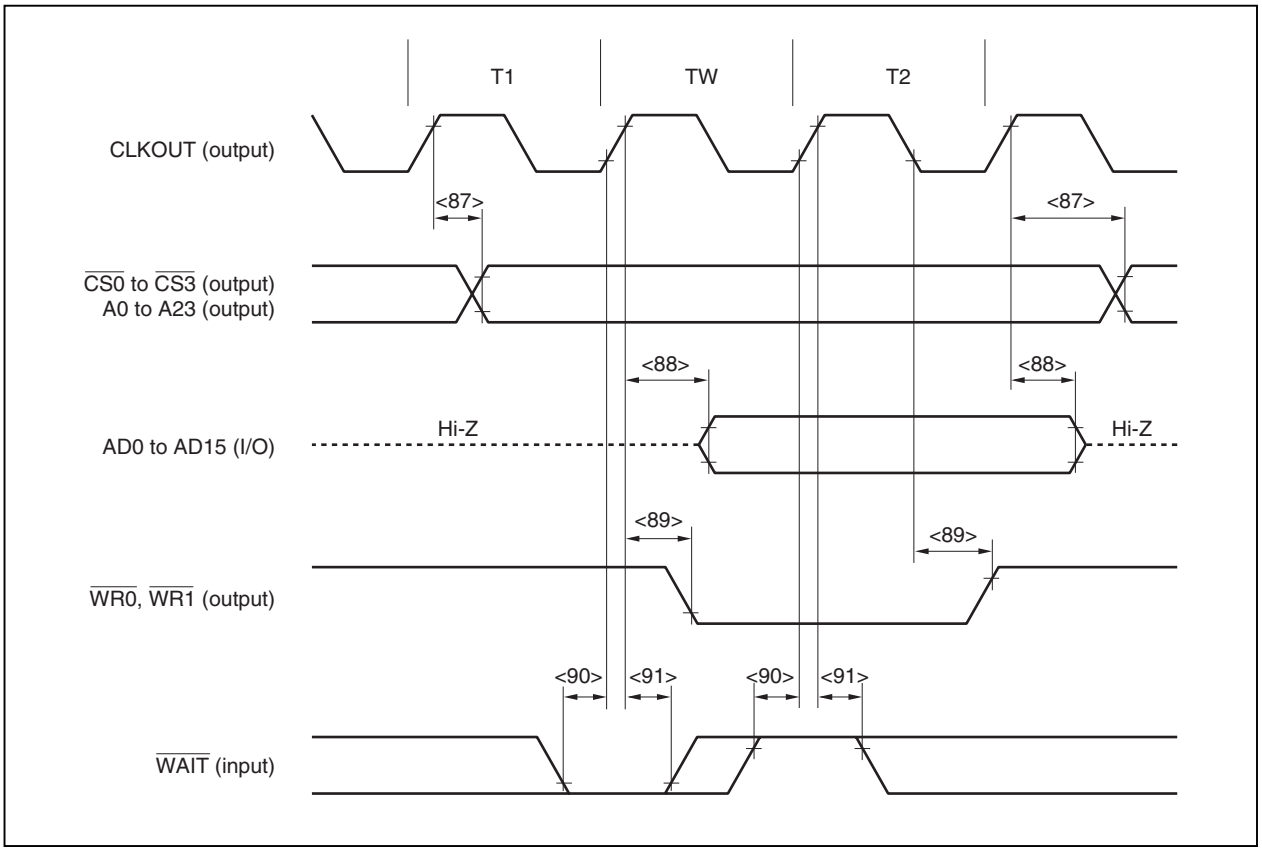
Read Cycle (CLKOUT Synchronous, 1 Wait): In Separate Bus Mode



Write Cycle (CLKOUT Asynchronous, 1 Wait): In Separate Bus Mode



Write Cycle (CLKOUT Synchronous, 1 Wait): In Separate Bus Mode



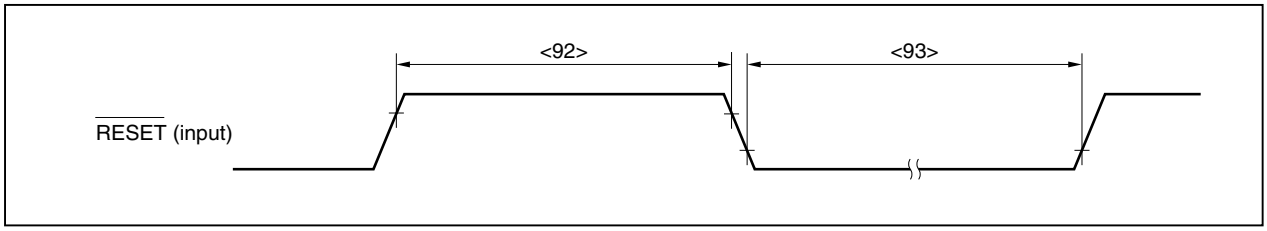
Reset/Interrupt Timing

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

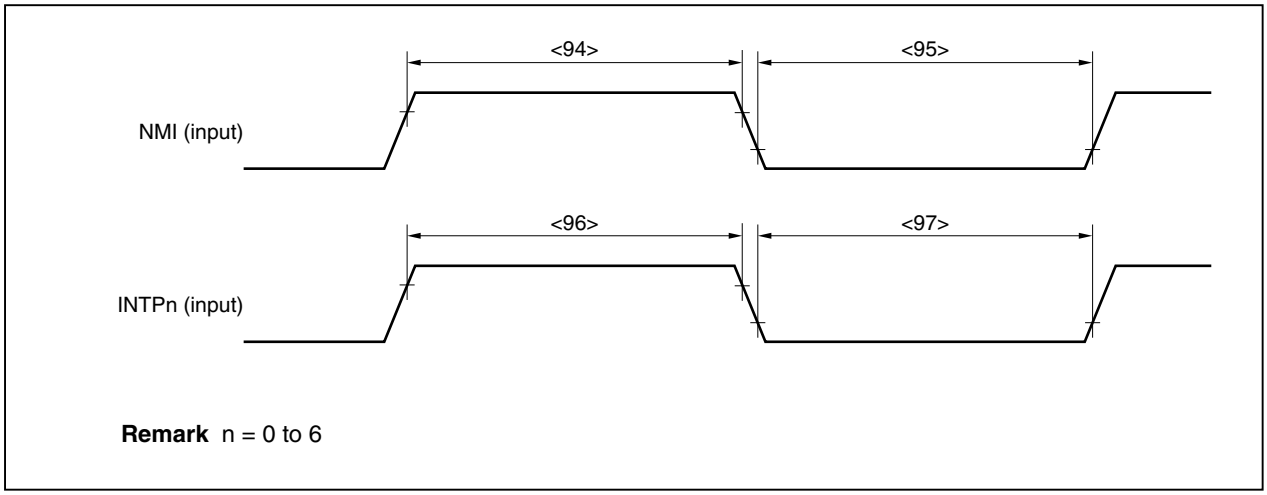
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}	<92>		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL}	<93>		500		ns
NMI high-level width	t_{WNIH}	<94>		500		ns
NMI low-level width	t_{WNIL}	<95>		500		ns
INTPn high-level width	t_{WITH}	<96>	n = 0 to 6 (analog noise elimination)	500		ns
INTPn low-level width	t_{WITL}	<97>	n = 0 to 6 (analog noise elimination)	500		ns

Remark T = 1/fxx

Reset



Interrupt



Remark n = 0 to 6

Timer Timing

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width		n = 0, 1	2T + 20		ns
		n = 2 to 5	40		ns
TIn low-level width		n = 0, 1	2T + 20		ns
		n = 2 to 5	40		ns
TCLRn high-level width		n = 0, 1	2T + 20		ns
TCLRn low-level width		n = 0, 1	2T + 20		ns
INTPnm high-level width	t_{WITH}	nm = 00, 01, 10, 11	2T + 20		ns
INTPnm low-level width	t_{WITL}	nm = 00, 01, 10, 11	2T + 20		ns

Remark T = 1/fxx

CSI Timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY1}	<98>	Output	200		ns
$\overline{SCKn}$ high-/low-level width	t_{KH1}, t_{KL1}	<99>	Output	t_{KCY1}/2 – 10		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK1}	<100>		30		ns
SIn hold time (from $\overline{SCKn}$↑)	t_{KSI1}	<101>		30		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO1}	<102>			30	ns

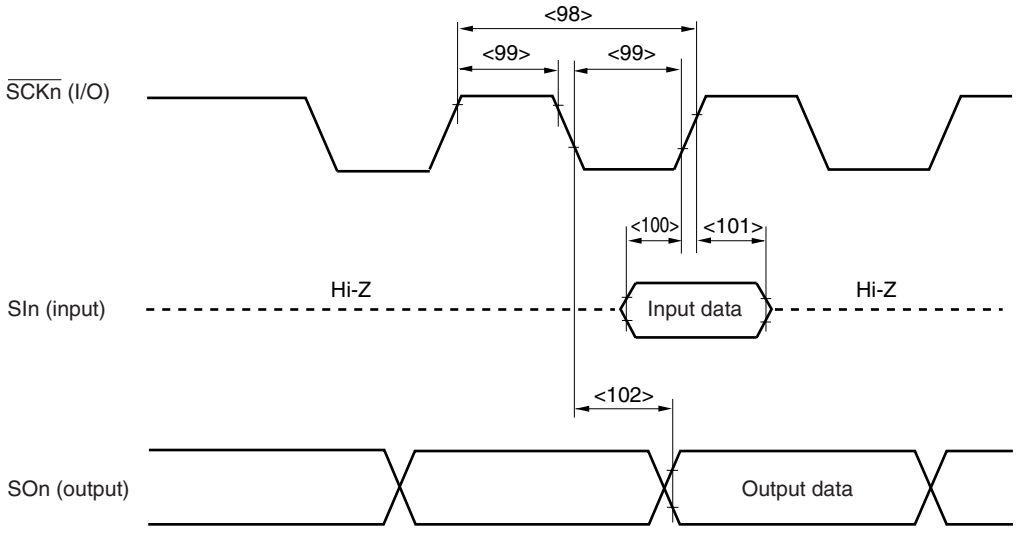
Remark n = 0 to 3 (V850ES/SA2), n = 0 to 4 (V850ES/SA3)

(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY2}	<98>	Output	200		ns
$\overline{SCKn}$ high-/low-level width	t_{KH2}, t_{KL2}	<99>	Output	90		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK2}	<100>		50		ns
SIn hold time (from $\overline{SCKn}$↑)	t_{KSI2}	<101>		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO2}	<102>			50	ns

Remark n = 0 to 3 (V850ES/SA2), n = 0 to 4 (V850ES/SA3)



Remark n = 0 to 3 (V850ES/SA2), n = 0 to 4 (V850ES/SA3)

I²C Bus Mode (μPD703201Y, 703204Y, 70F3201Y, 70F3204Y only)

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = $V_{DD}BU$ = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = $V_{SS}BU$ = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL clock frequency		f_{CLK}		0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	<103>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<104>	4.0	–	0.6	–	μs
SCL clock low-level width		t_{LOW}	<105>	4.7	–	1.3	–	μs
SCL clock high-level width		t_{HIGH}	<106>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<107>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<108>	5.0	–	–	–	μs
	I²C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<109>	250	–	100[Note 4]	–	ns
SDA and SCL signal rise time		t_R	<110>	–	1,000	20 + 0.1Cb[Note 5]	300	ns
SDA and SCL signal fall time		t_F	<111>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<112>	4.0	–	0.6	–	μs
Pulse width with spike suppressed by input filter		t_{SP}	<113>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA signal (at $V_{IHmin.}$ of SCL signal) in order to occupy the undefined area at the falling edge of SCL.

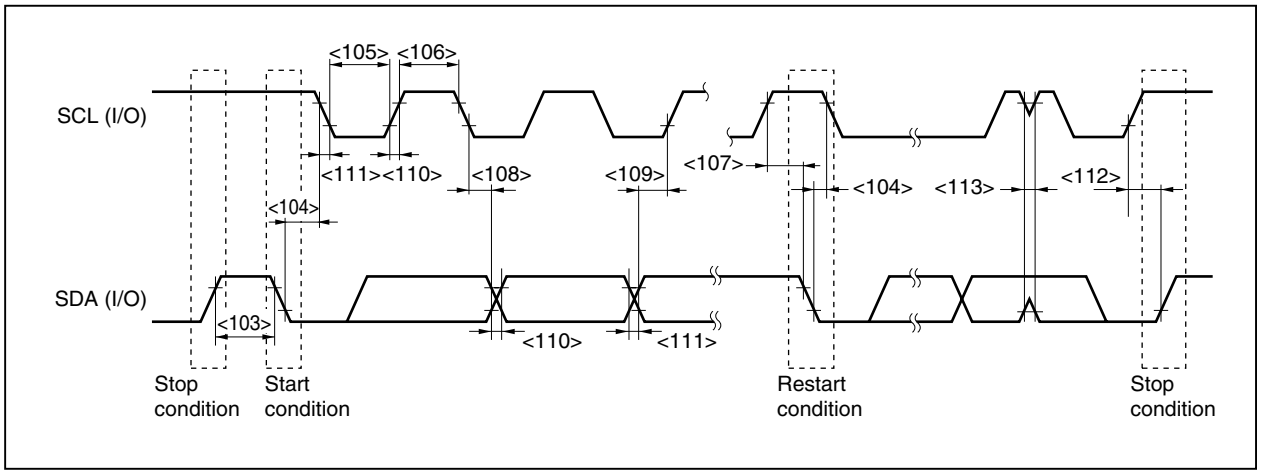
3. If the system does not extend the SCL signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed-mode I²C bus can be used in a normal-mode I²C bus system. In this case, set the high-speed-mode I²C bus so that it meets the following conditions.

- If the system does not extend the SCL signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL signal's low state hold time:
  Transmit the following data bit to the SDA line prior to releasing the SCL line ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns: Normal mode I²C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

I²C Bus Mode (μPD703201Y, 703204Y, 70F3201Y, 70F3204Y only)



A/D Converter

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF0} = 2.2 to 2.7 V, AV_{SS} = V_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]					T.B.D.	%FSR
Conversion time	t_{CONV}		T.B.D.			μs
Zero-scale error[Note 1]					T.B.D.	%FSR
Full-scale error[Note 1]					T.B.D.	%FSR
Integral linearity error[Note 2]					T.B.D.	LSB
Differential linearity error[Note 2]					T.B.D.	LSB
Analog reference voltage	AV_{REF}	$AV_{REF0} = AV_{DD}$	2.2		2.7	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF0} current	AI_{REF0}			T.B.D.		μA
AV_{DD} power supply current	AI_{DD}			T.B.D.		mA

Notes 1. Excluding quantization error (±0.05 %FSR)

2. Excluding quantization error (±0.5 LSB)

Remark LSB: Least Significant Bit
FSR: Full Scale Range

D/A Converter

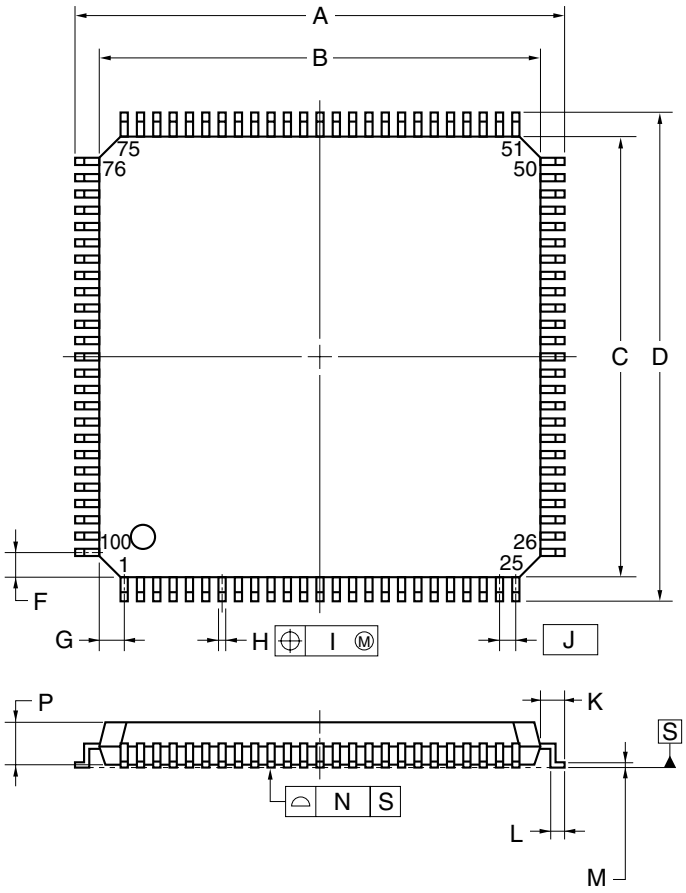
(T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 2.2 to 2.7 V, AV_{SS} = V_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		Load conditions: 2 MΩ, 30 pF AV_{REF1} = V_{DD}			T.B.D.	%FSR
Settling time					T.B.D.	μs
Output resistance				T.B.D.		kΩ
Analog reference voltage	AV_{REF}	AV_{REF1} = V_{DD}	2.2		2.7	V
AV_{REF1} current	AV_{REF1}	Per channel		T.B.D.		mA

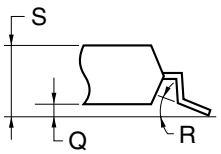
Note Excludes quantization error (±0.05%FSR).

21. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



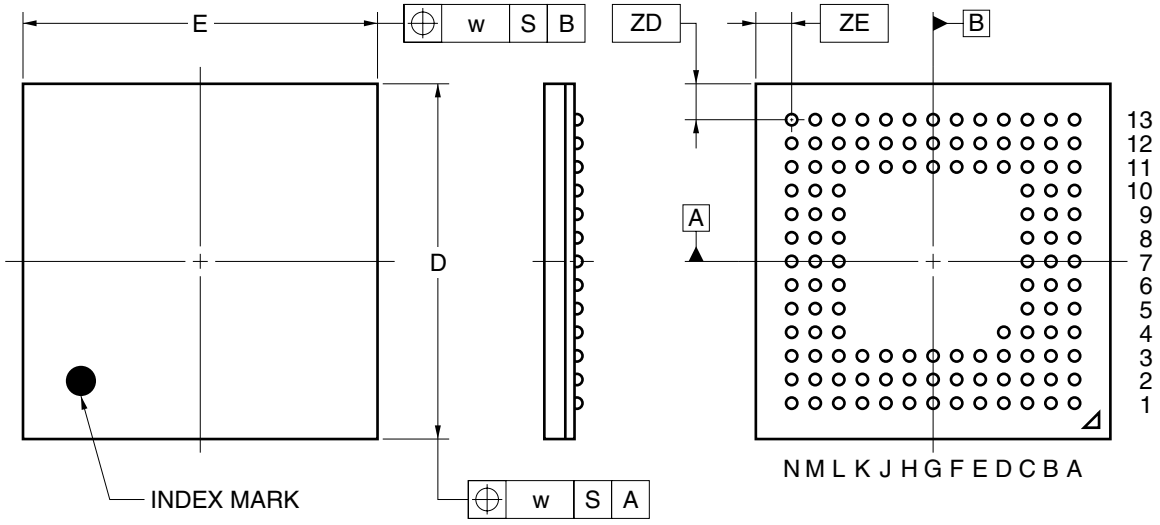
NOTE

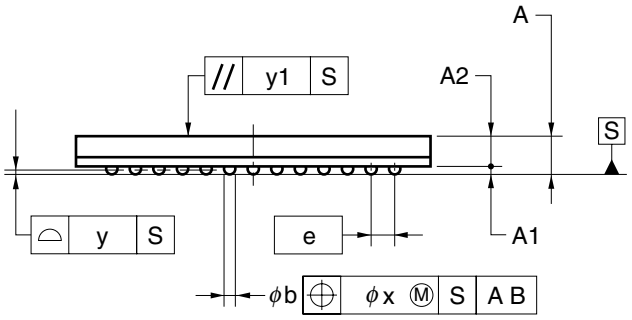
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

121-PIN PLASTIC FBGA (12x12)





ITEM	MILLIMETERS
D	12.00±0.10
E	12.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P121F1-80-EA6

APPENDIX DEVELOPMENT TOOLS

(1) Hardware

Product Name			Description
In-circuit emulator		IE-V850ES-××[Note] (provisional name)	In-circuit emulator for V850ES
In-circuit emulator option board		IE-703204-MC-EM1[Note] (provisional name)	Option board to emulate V850ES/SA2, V850ES/SA3 peripheral functions in combination with in-circuit emulator
Emulation probe	V850ES/SA2	**Note**	Emulation probe for 100-pin LQFP
	V850ES/SA3	**Note**	Emulation probe for 121-pin FBGA
Power supply unit		IE-70000-MC-PS-B	Power supply for in-circuit emulator
PC interface board		IE-70000-CD-IF-A	Interface board for connection to PC (for PCMCIA)
		IE-70000-PCI-IF	Interface board for connection to PC (for PCI)
Flash programmer		**Note**	Flash programmer for writing a program to a single-power-supply flash memory product.
Program adapter	V850ES/SA2	**Note**	Program adapter for 100-pin LQFP
	V850ES/SA3	**Note**	Program adapter for 121-pin FBGA

Note Under development

(2) Software

Product Name			Description
Compiler		CA850	C compiler compliant with ANSI-C
Debugger		ID850	Debugger used in combination with in-circuit emulator
Real-time OS		RX850	Real-time OS compliant with μITRON specifications
Device file	V850ES/SA2	DF703201[Note]	Definition file for V850ES/SA2
	V850ES/SA3	DF703204[Note]	Definition file for V850ES/SA3

Note Under development

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
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