

Accurate Power Surveillance and Software Monitoring

Features

- Standby mode, maximum current 35 μ A
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, voltage reference 1.17 V
- $\pm 1.5\%$ voltage reference accuracy at +25 $^{\circ}$ C
- $\pm 3\%$ voltage reference accuracy for -40 to +85 $^{\circ}$ C
- Programmable reset voltage monitoring
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy $\pm 10\%$
- System enable (\overline{EN}) output offers added security
- TTL/CMOS compatible
- -40 to +85 $^{\circ}$ C temperature range
- On request extended temperature range, -40 to +125 $^{\circ}$ C
- DIP8 and SO8 packages

Description

The V6130 offers a high level of integration by voltage monitoring and software monitoring in an 8 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The \overline{RES} and \overline{EN} outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- Automotive electronics

Typical Operating Configuration

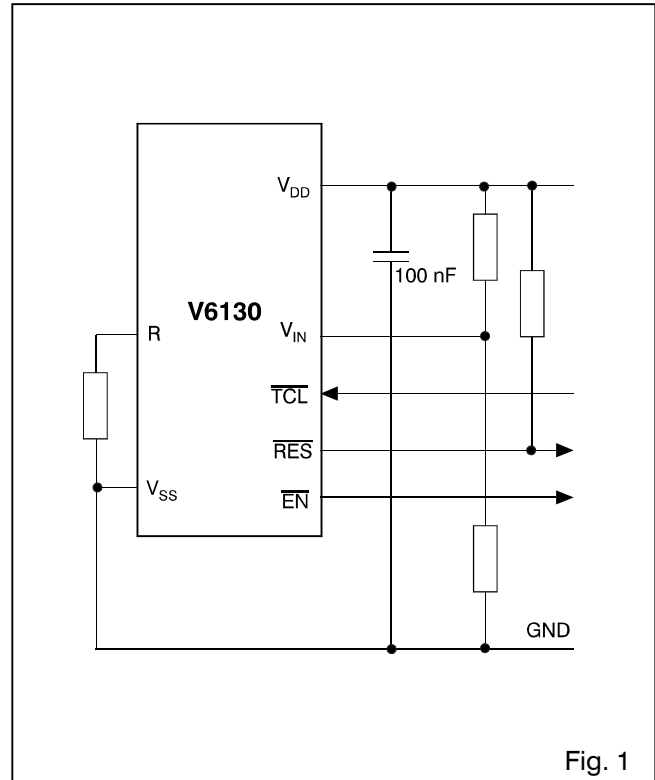


Fig. 1

Pin Assignment

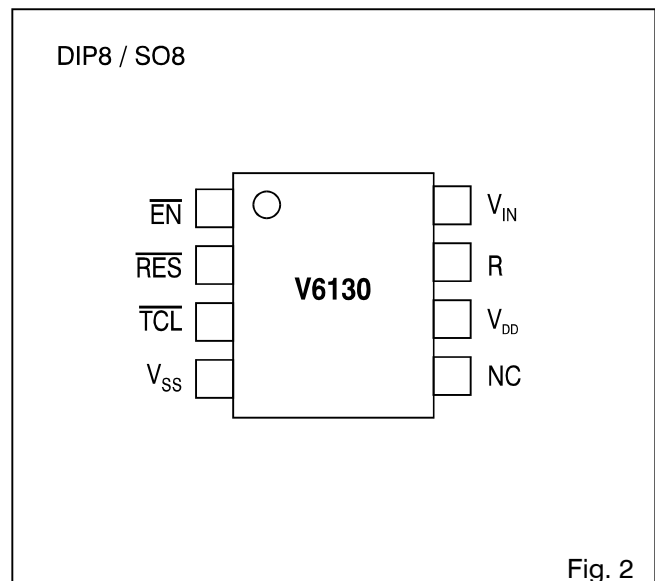
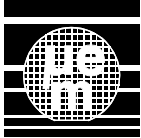


Fig. 2



Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	$V_{SS} + 8\text{ V}$
Minimum voltage at V_{DD}	V_{DDmin}	$V_{SS} - 0.3\text{ V}$
Max. voltage at any signal pin	V_{MAX}	$V_{DD} + 0.3\text{ V}$
Min. voltage at any signal pin	V_{MIN}	$V_{SS} - 0.3\text{ V}$
Storage temperature	T_{STO}	-65 to +150 °C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250 °C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless

otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating temperature ¹⁾	T_J	-40	+125	°C
Supply voltage ²⁾	V_{DD}	1.2	7	V
RES & EN guaranteed ³⁾	V_{DD}	1.2		V
Comparator input voltage	V_{IN}	0	V_{DD}	V
RC-oscillator programming	R	10	1000	kΩ

Table 2

¹⁾ The maximum operating temperature is confirmed by sampling at initial device qualification. In production, all devices are tested at +85 °C. On request devices tested at +125 °C can be supplied.

²⁾ A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

³⁾ RES must be pulled up externally to V_{DD} event if it is unused. (Note: RES and EN are used as inputs by EM test.)

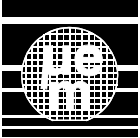
Electrical Characteristics

$3.0 \leq V_{DD} \leq 5.5\text{ V}$, $C = 100\text{ nF}$, $T_A = -40\text{ to }+85\text{ °C}$, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	$R_{EXT} = \text{don't care}$, $TCL = V_{DD}$, $V_{IN} = 0\text{ V}$		22	35	μA
Supply current	I_{SS}	$R_{EXT} = 100\text{ k}\Omega$, I/Ps at V_{DD} , O/Ps $1\text{ M}\Omega$ to V_{DD}		55	100	μA
RES and EN						
Output Low Voltage	V_{OL}	$V_{DD} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$		0.4		V
	V_{OL}	$V_{DD} = 4.5\text{ V}$, $I_{OL} = 8\text{ mA}$		0.2	0.4	V
	V_{OL}	$V_{DD} = 2.0\text{ V}$, $I_{OL} = 4\text{ mA}$		0.2	0.4	V
	V_{OL}	$V_{DD} = 1.2\text{ V}$, $I_{OL} = 0.5\text{ mA}$		0.06	0.2	V
EN						
Output High Voltage	V_{OH}	$V_{DD} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$	3.5	4.1		V
	V_{OH}	$V_{DD} = 2.0\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	1.8	1.9		V
	V_{OH}	$V_{DD} = 1.2\text{ V}$, $I_{OH} = -30\text{ }\mu\text{A}$	1.0	1.1		V
TCL and V_{IN}						
TCL input low level	V_{IL}		V_{SS}		0.8	V
TCL input high level	V_{IH}		2.0		V_{DD}	V
Leakage current $\overline{\text{TCL}}$ input	I_{LI}	$V_{SS} \leq V_{TCL} \leq V_{DD}$		0.05	1	μA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference ¹⁾	V_{REF}	$T_A = +25\text{ °C}$	1.148	1.170	1.200	V
	V_{REF}	$T_A = -20\text{ to }+70\text{ °C}$	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis ¹⁾	V_{HY}			2		mV

Table 3

¹⁾ The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig.5).



I_{SS} Standby versus Temperature at $V_{DD} = 5.5 V$

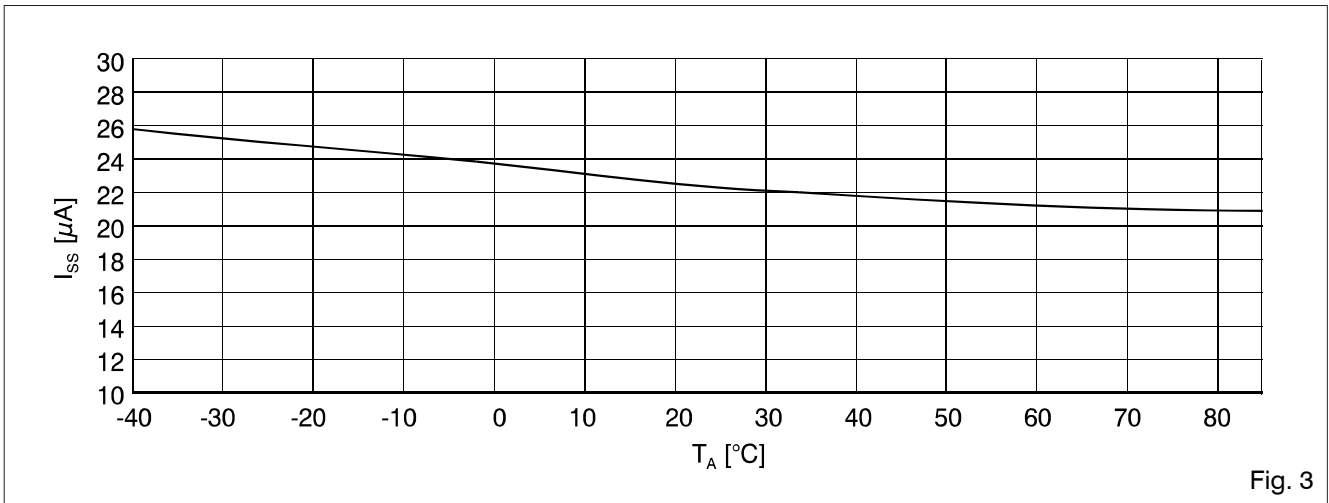


Fig. 3

Timing Characteristics

$V_{DD} = 5.0 V \pm 3\%$, $C = 100 nF$, $T_A = -40$ to $+85^\circ C$, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays: TCL to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	$R_{EXT} = 118 k\Omega, \pm 1\%$	90	100	110	ms
Watchdog Time	T_{WD}	$R_{EXT} = 118 k\Omega, \pm 1\%$	90	100	110	ms
Open Window Percentage	OWP			$\pm 0.2 T_{WD}$		
Closed Window Time	T_{CW}			$0.8 T_{WD}$		
Open Window Time	T_{OW}	$R_{EXT} = 118 k\Omega, \pm 1\%$	72	80	88	ms
Watchdog Reset Pulse	T_{WDR}	$R_{EXT} = 118 k\Omega, \pm 1\%$	36	40	44	ms
	T_{WDR}			$T_{WD} / 40$		ms
T_{CL} Input Pulse Width	T_{TCL}	$R_{EXT} = 118 k\Omega, \pm 1\%$	150	2.5		ns

Table 4

Timing Waveforms

Watchdog Timeout Period

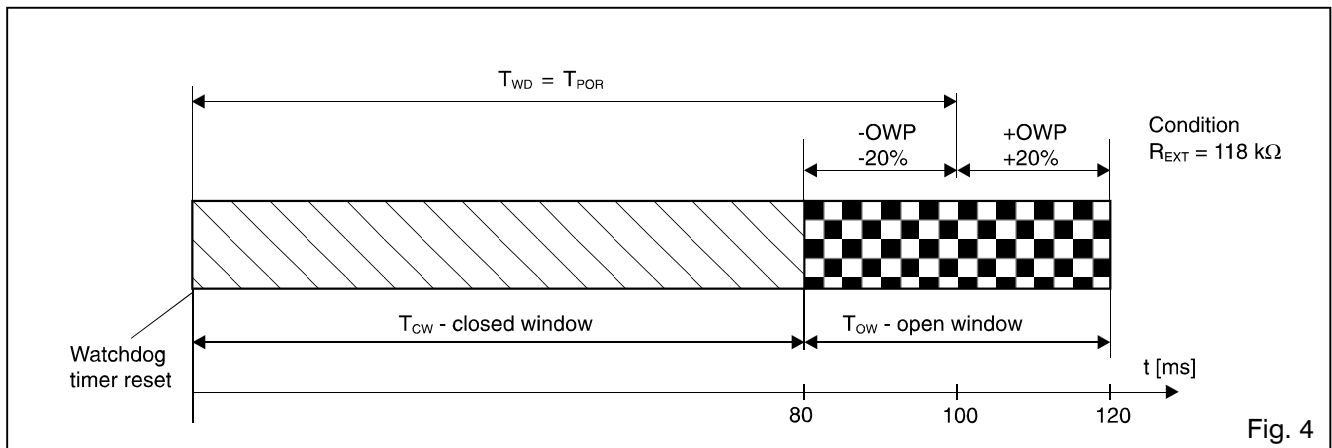
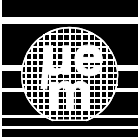
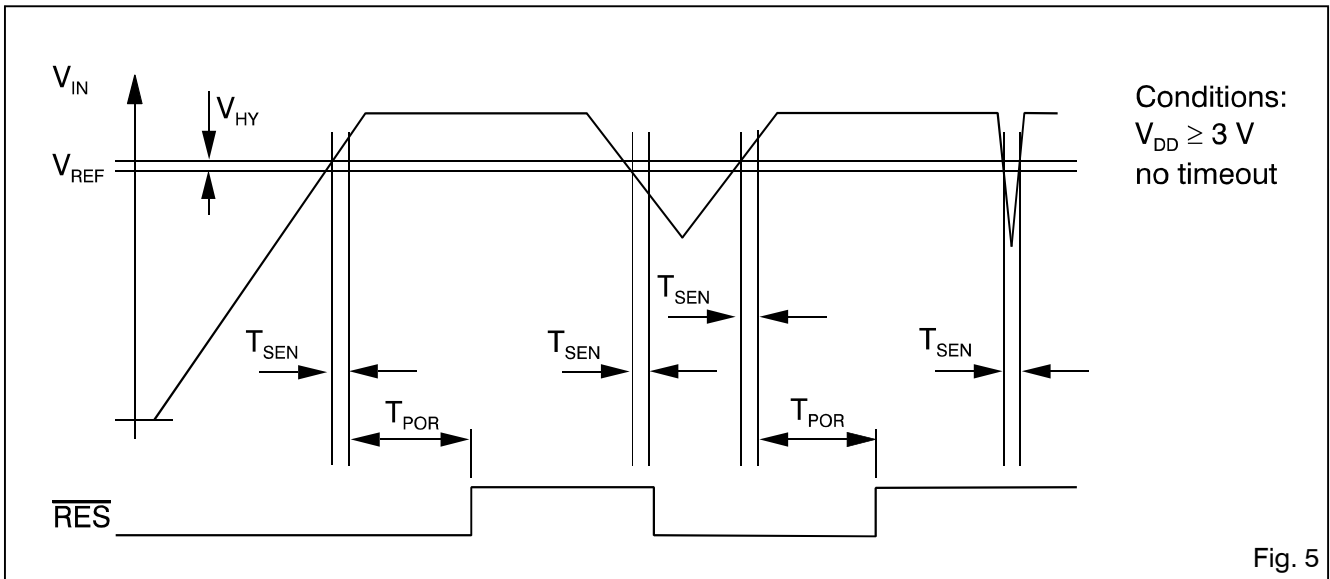


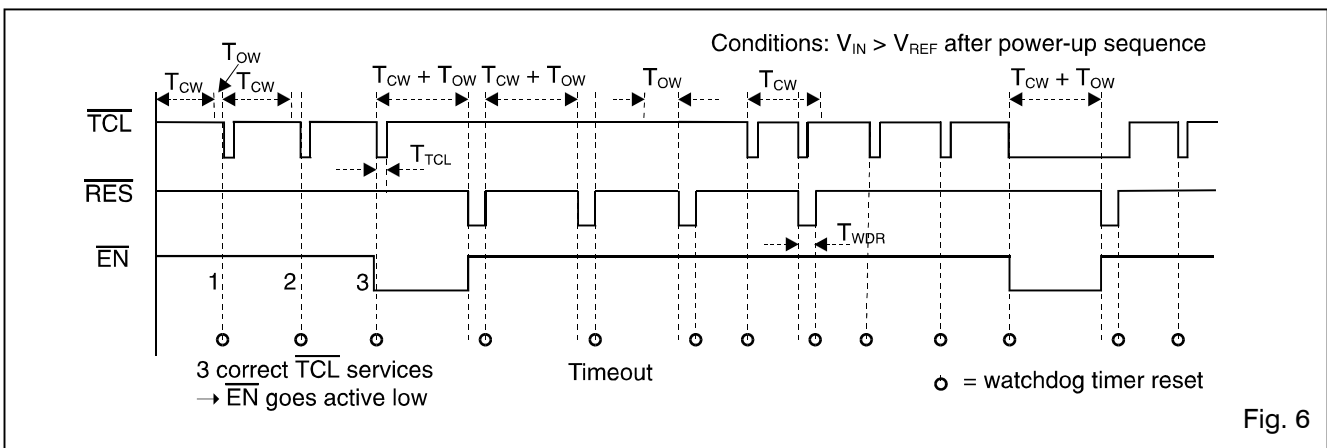
Fig. 4



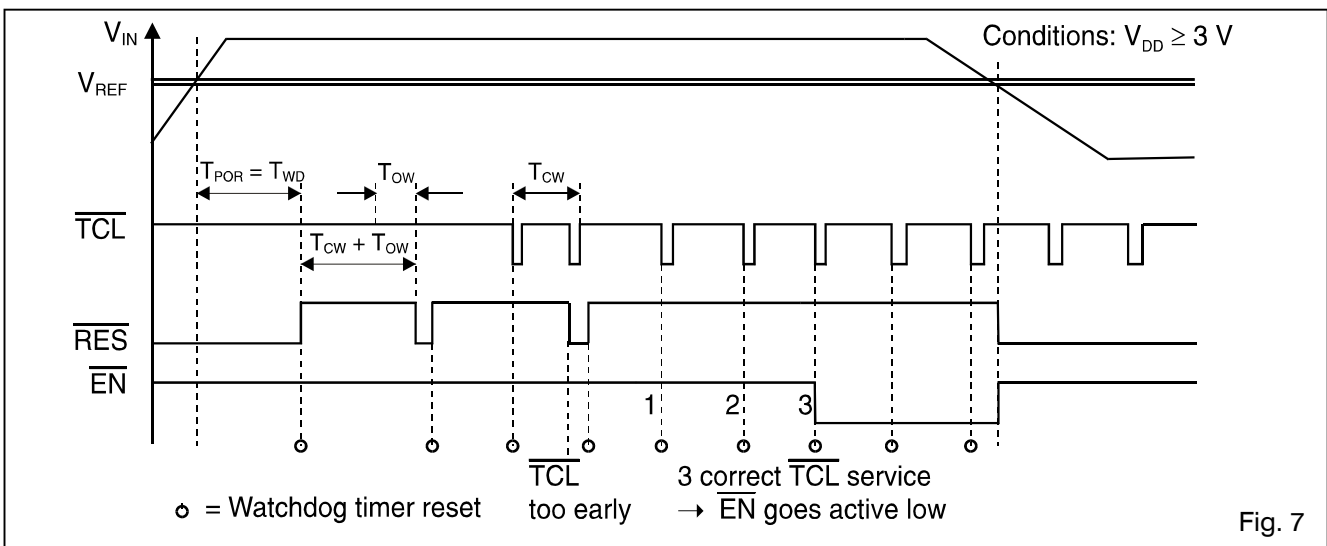
Voltage Monitoring

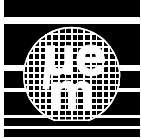


Timer Reaction



Combined Voltage and Timer Reaction





Block Diagram

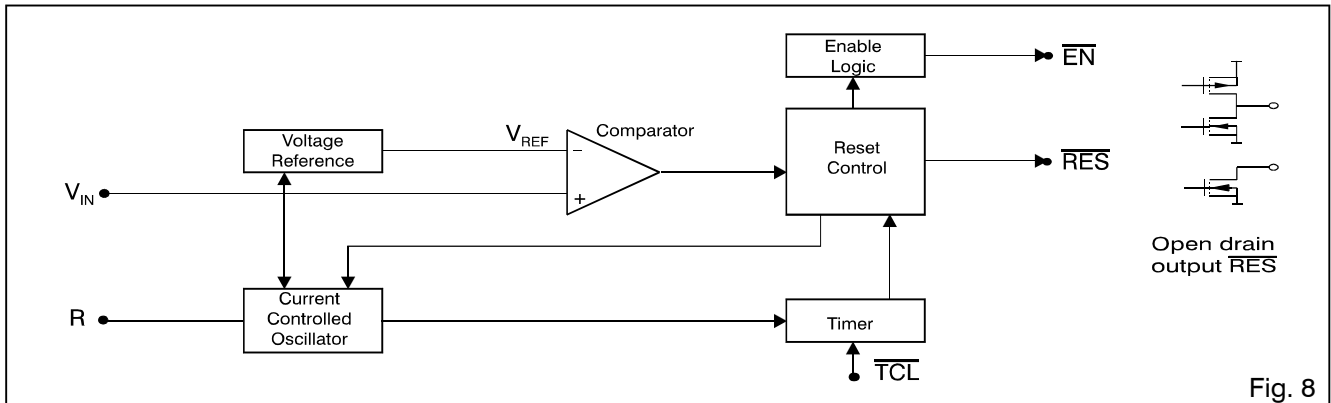


Fig. 8

Pin Description

Pin	Name	Function
1	\overline{EN}	Push-pull active low enable output
2	\overline{RES}	Open drain active low reset output. \overline{RES} must be pulled up to V_{DD} even if unused
3	\overline{TCL}	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	NC	No connection
6	V_{DD}	Voltage supply
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level on the V_{IN} input. The external voltage level is typically obtained from a voltage divider as shown in Fig. 9. The user defines an external voltage divider to set the desired threshold level for power-on reset and power-down reset in his system. The internal comparator reference voltage is typically 1.17 V.

At power-up the reset output (\overline{RES}) is held low (see Fig. 5). When V_{IN} becomes greater than V_{REF} , the \overline{RES} output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 118 k Ω connected at R pin). The POR delay prevents repeated toggling of \overline{RES} even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The \overline{RES} output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF} . The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μ s.

Timer Programming

The on-chip oscillator needs an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9). It allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width ($T_{WD}/40$).

With $R_{EXT} = 118$ k Ω , the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note: The current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig.4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

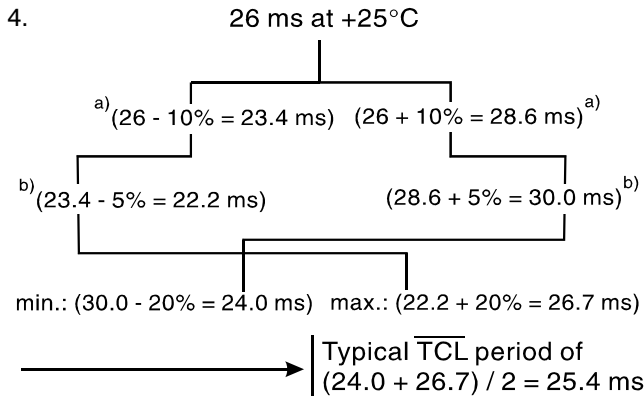
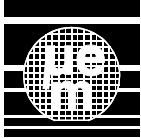
The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if $T_{WD} = 100$ ms (actual value) and $OWP = \pm 20\%$ this means the closed window lasts during first the 80 ms ($T_{CW} = 80$ ms = 100 ms - 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is $\pm 10\%$ accurate, software must use the following calculation for servicing signal \overline{TCL} during the open window:

Related to curves (Fig. 10 to Fig. 20), especially Fig. 19 and Fig. 20, the relation between T_{WD} and R_{EXT} could easily be defined. Let us take an example describing the variations due to production and temperature:

1. Choice, $T_{WD} = 26$ ms.
2. Related to Fig. 20, the coefficient (T_{WD} to R_{EXT}) is 1.125 where R_{EXT} is in k Ω and T_{WD} in ms.
3. R_{EXT} (typ.) = 26 x 1.125 = 29.3 k Ω .



The ratio between $T_{WD} = 26$ ms and the \overline{TCL} period = 25.4 ms is 0.975.
 Then the relation over the production and the full temperature range is, \overline{TCL} period = 0.975 x T_{WD}

$$\text{or } \overline{TCL} \text{ period} = \frac{0.975 \times R_{EXT}}{1.125}, \text{ as typical value.}$$

- a) While PRODUCTION value unknown for the customer when $R_{EXT} \neq 118$ k Ω .
 - b) While operating TEMPERATURE range $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.
5. If you fixed a \overline{TCL} period = 26 ms

$$\Rightarrow R_{EXT} = \frac{26 \times 1.125}{0.975} = 30 \text{ k}\Omega.$$

If during your production the T_{WD} time can be measured at $T_A = +25^\circ\text{C}$ and the μC can adjust the \overline{TCL} period, then the \overline{TCL} period range will be much larger for the full operating temperature.

Timer Clearing and \overline{RES} Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the \overline{TCL} input within the programmed open window timeout period, a short watchdog \overline{RES} pulse is generated which is equal to $T_{WD}/40 = 2.5$ ms typically (see Fig. 6).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, a conventional watchdog will not reset the system even though the software is malfunctioning; the V6130 will generate a system reset because the watchdog is cleared too quickly.

If no \overline{TCL} signal is applied before the closed and open windows expire, \overline{RES} will start to generate square waves of period $(T_{CW} + T_{OW} + T_{WDR})$. The watchdog will remain in this state until the next \overline{TCL} falling edge appears during an open window, or until a fresh power-up sequence. The

system enable output, \overline{EN} , can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - \overline{EN} Output").

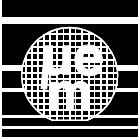
The \overline{RES} output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9)

Combined Voltage and Timer Action

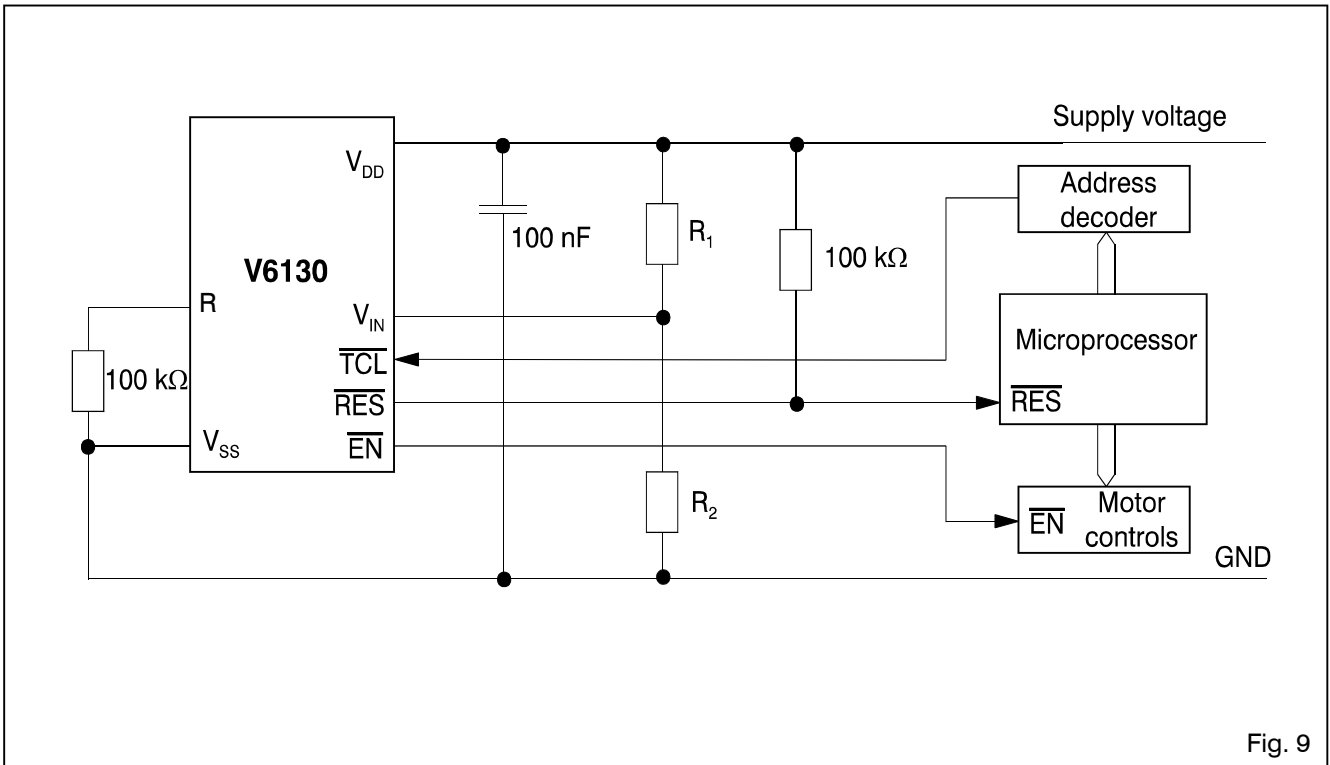
The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF} , the power-on-reset, POR, delay is initialized and holds \overline{RES} active for the time of the POR delay. A \overline{TCL} pulse will have no effect until this power-on-reset delay is completed. After the POR delay has elapsed, \overline{RES} goes inactive and the watchdog timer starts acting. If no \overline{TCL} pulse occurs, \overline{RES} goes active low for a short time T_{WDR} after each closed and open window period. A \overline{TCL} pulse coming during the open window clears the watchdog timer. When the \overline{TCL} pulse occurs too early (during the closed window), \overline{RES} goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs , overrides the timer and immediately forces \overline{RES} active and \overline{EN} inactive. Any further \overline{TCL} pulse has no effect until the next power-up sequence has completed.

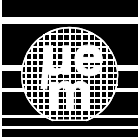
Enable - \overline{EN} Output

The system enable output, \overline{EN} , is inactive always when \overline{RES} is active and remains inactive after a \overline{RES} pulse until the watchdog is serviced correctly 3 consecutive times (ie. the \overline{TCL} pulse must come in the open window). After three consecutive services of the watchdog with \overline{TCL} during the open window, the \overline{EN} goes active low. A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V6130 prevents the above failure mode by using the \overline{EN} output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

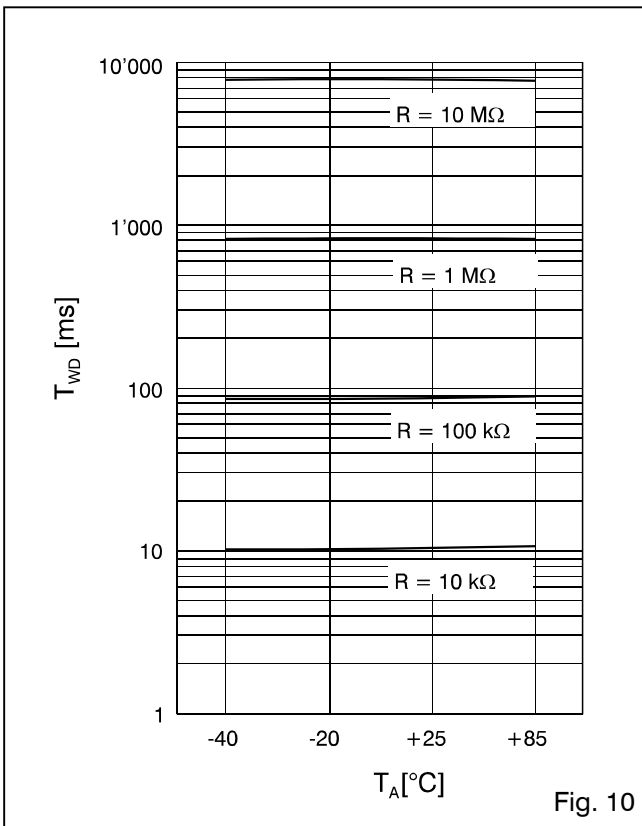


Typical Application

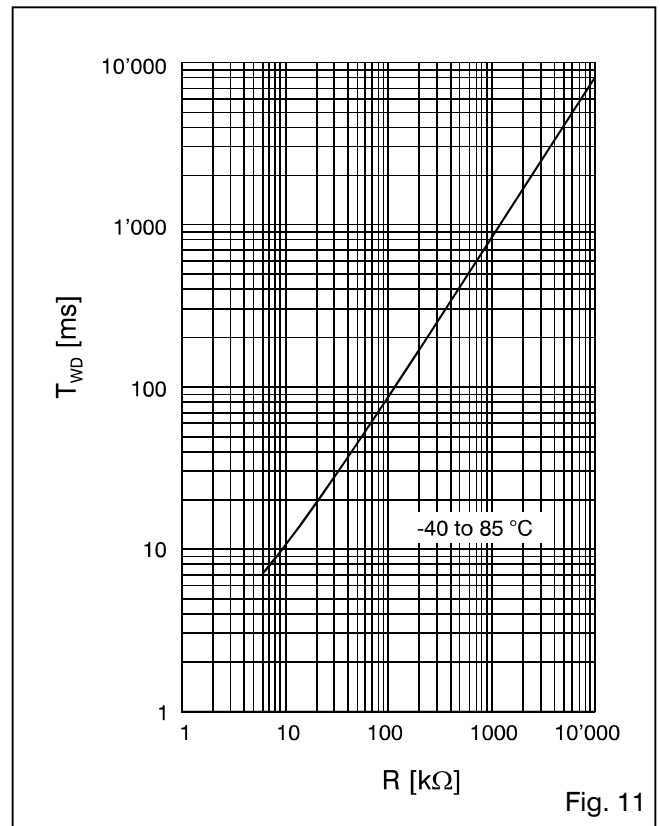




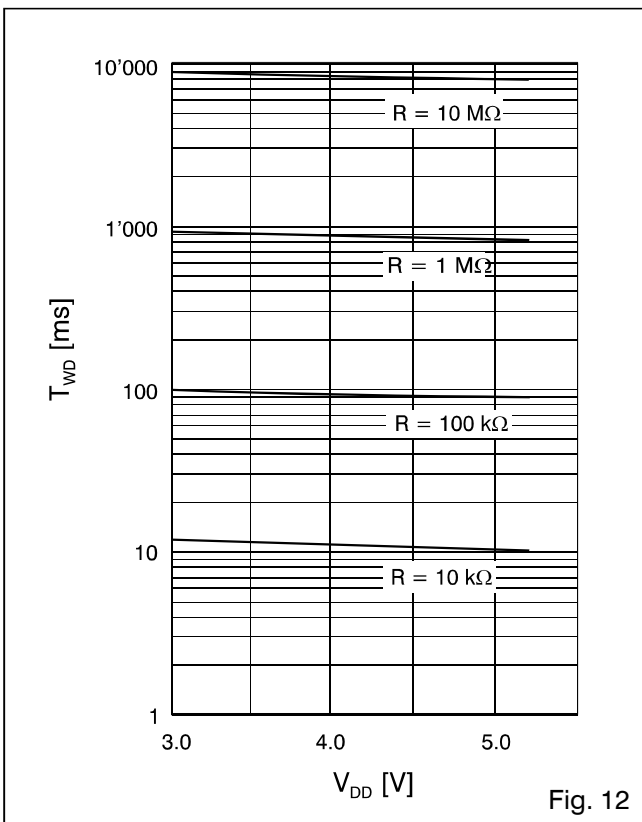
T_{WD} versus Temperature at 5 V



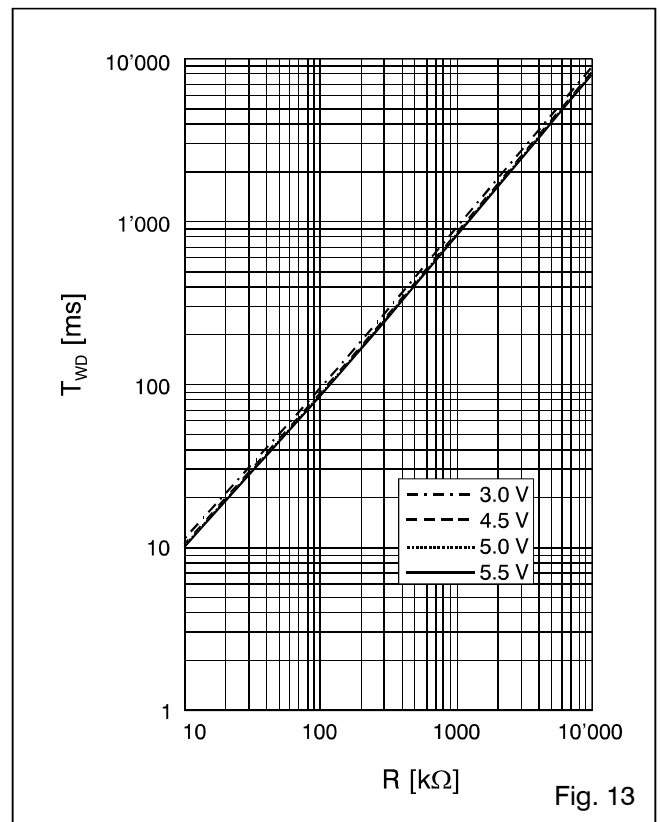
T_{WD} versus R at 5 V

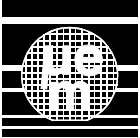


T_{WD} versus V_{DD} at $T_A = +25^\circ\text{C}$



T_{WD} versus R at $T_A = +25^\circ\text{C}$





T_{WD} versus R at $T_A = +25\text{ }^\circ\text{C}$

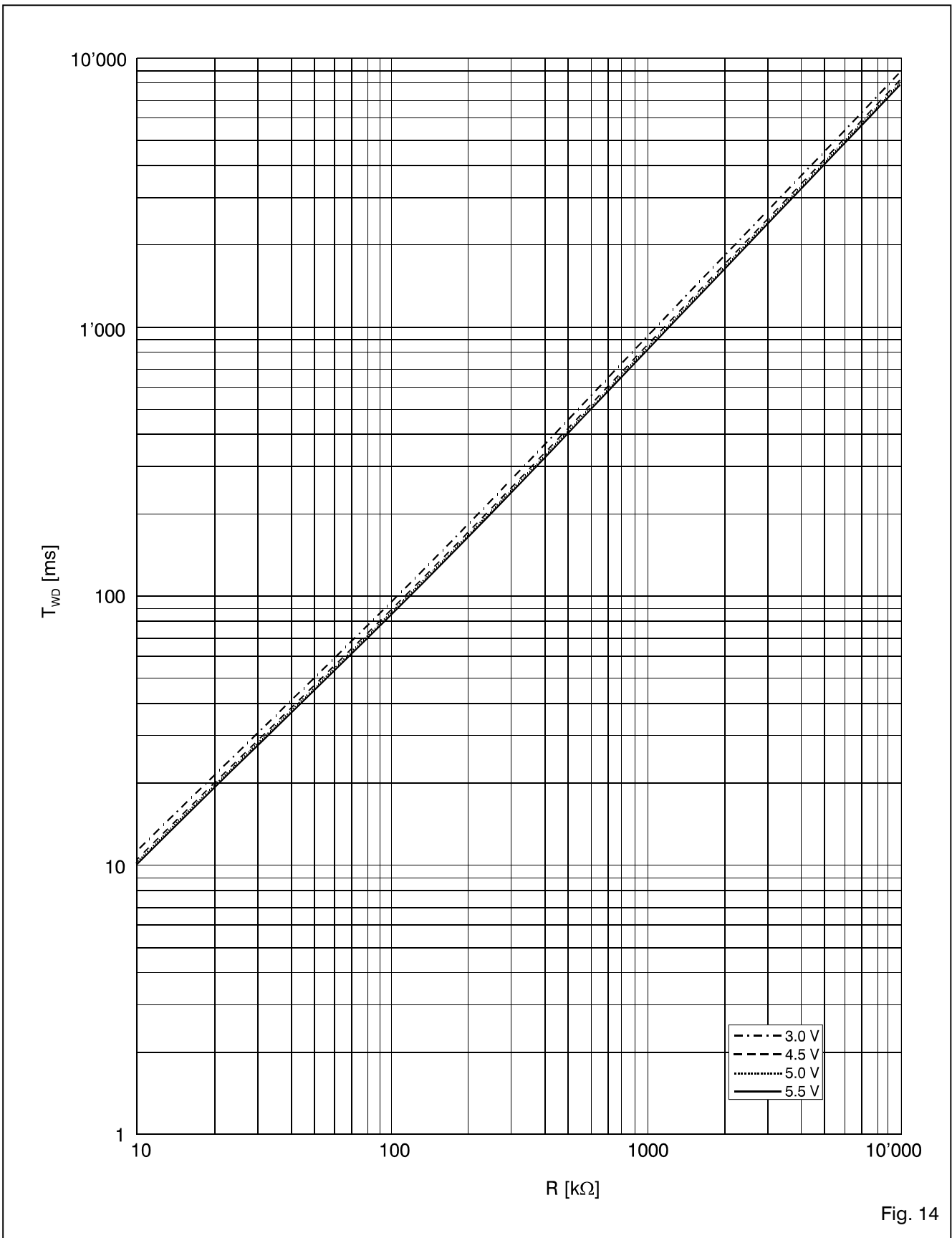
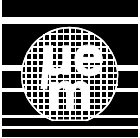
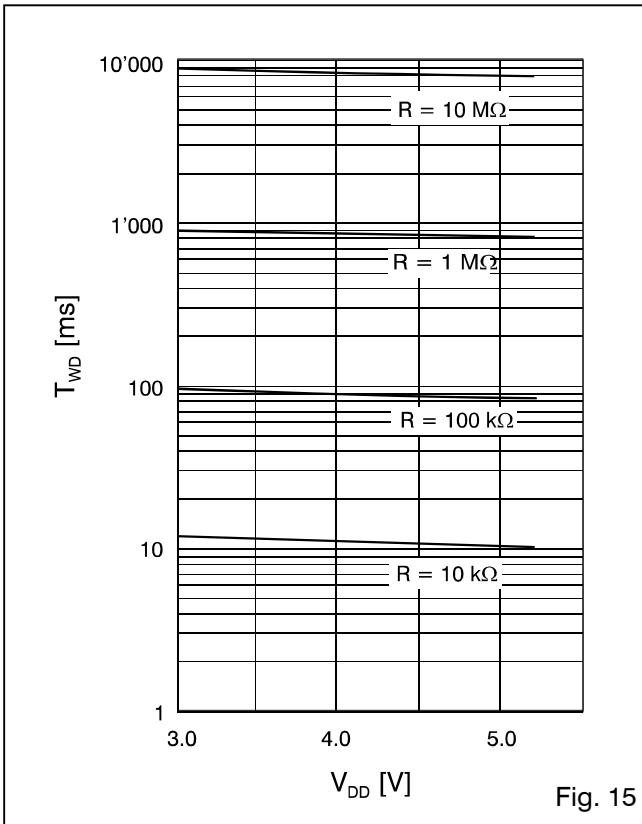


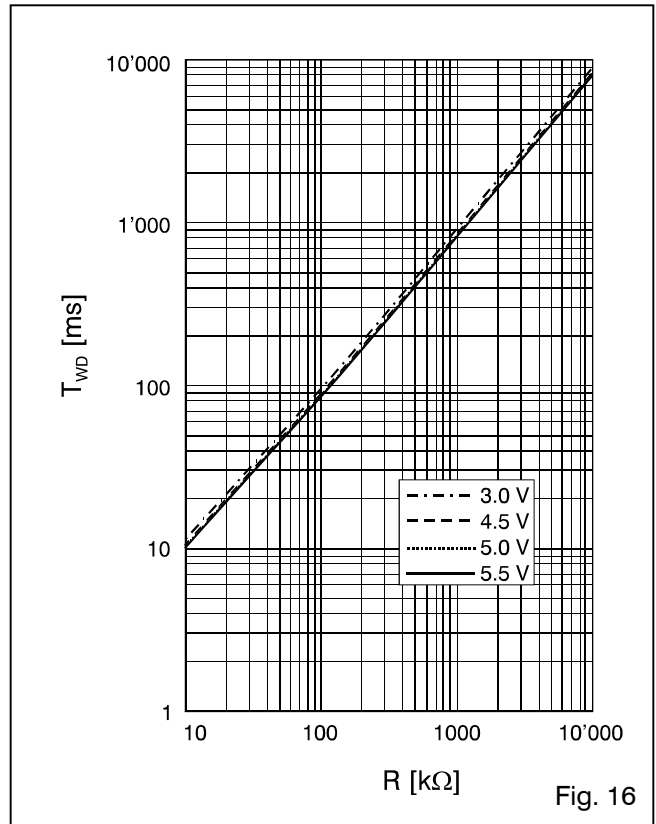
Fig. 14



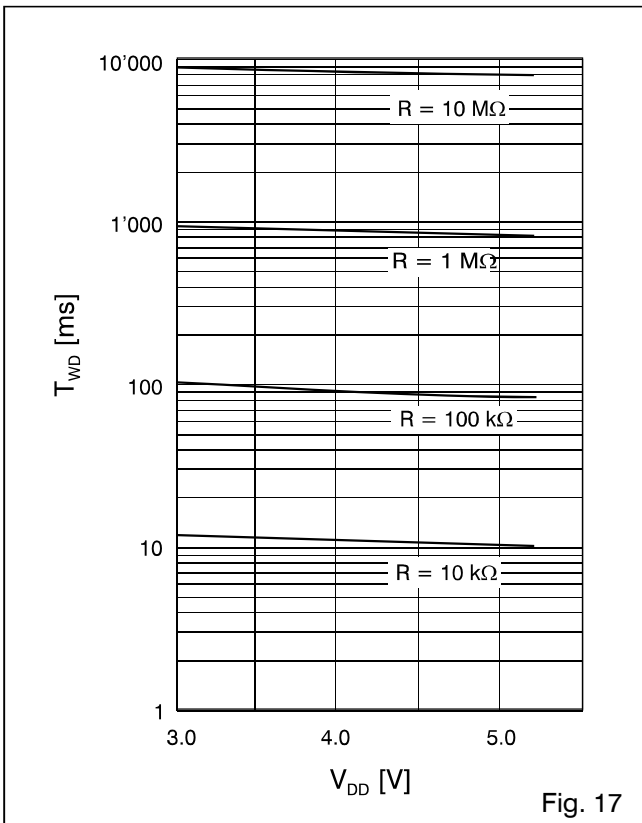
T_{WD} versus V_{DD} at $T_A = +85^\circ\text{C}$



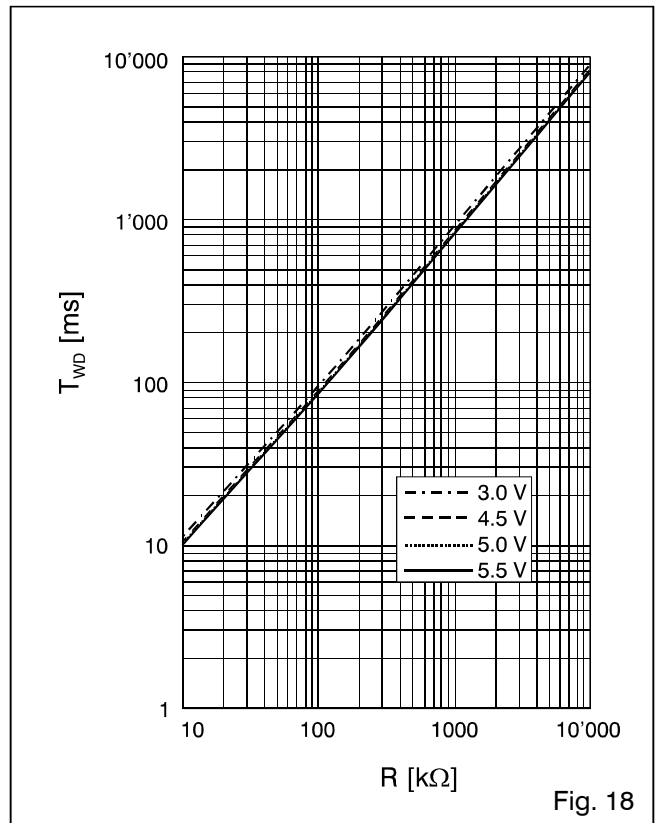
T_{WD} versus R at $T_A = +85^\circ\text{C}$

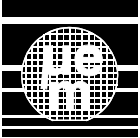


T_{WD} versus V_{DD} at $T_A = -40^\circ\text{C}$



T_{WD} versus R at $T_A = -40^\circ\text{C}$





T_{WD} Coefficient versus R_{EXT} at $T_A = +25^\circ\text{C}$

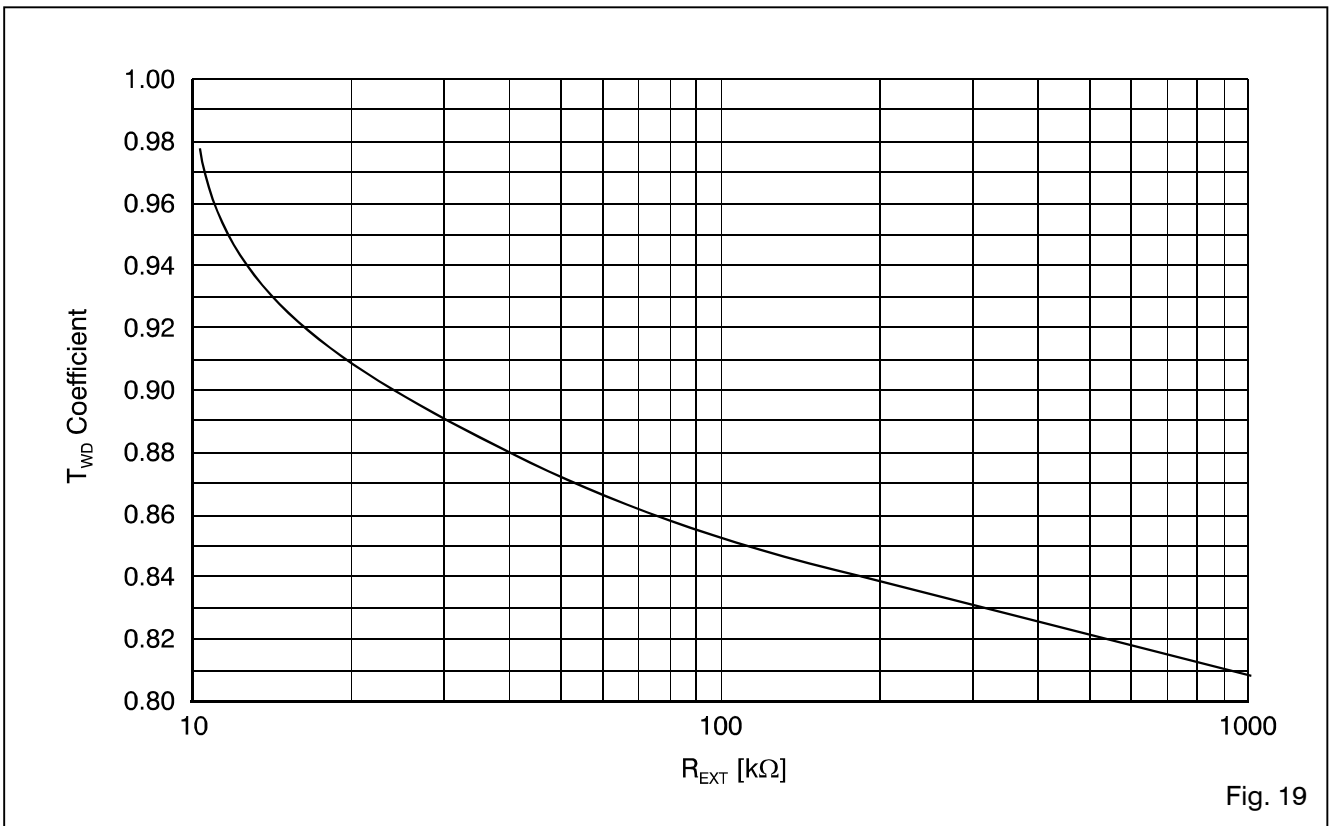


Fig. 19

R_{EXT} Coefficient versus T_{WD} at $T_A = +25^\circ\text{C}$

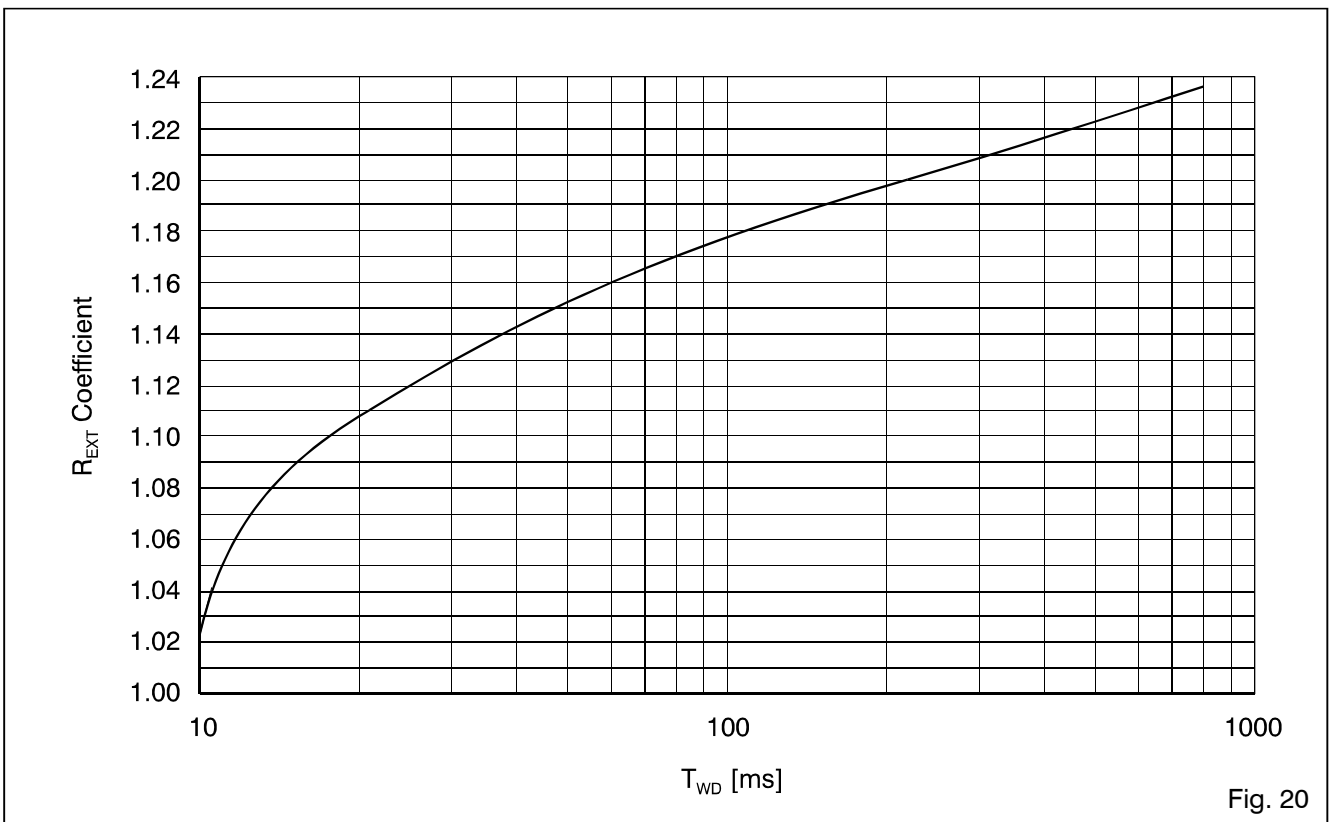
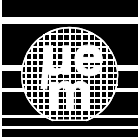
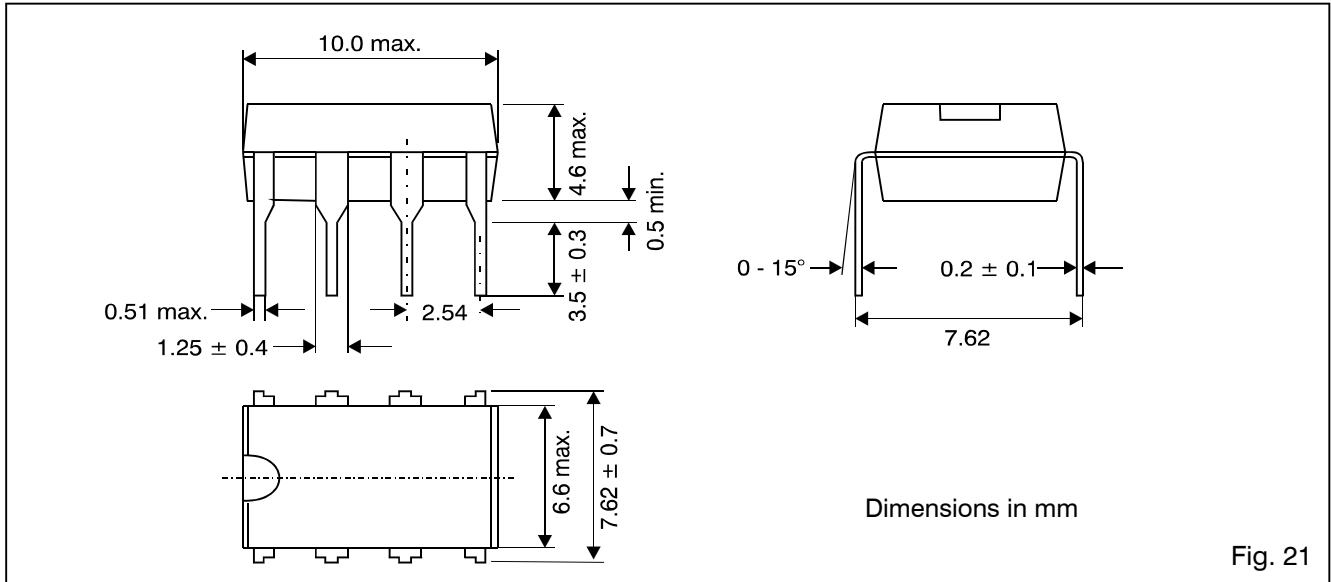


Fig. 20

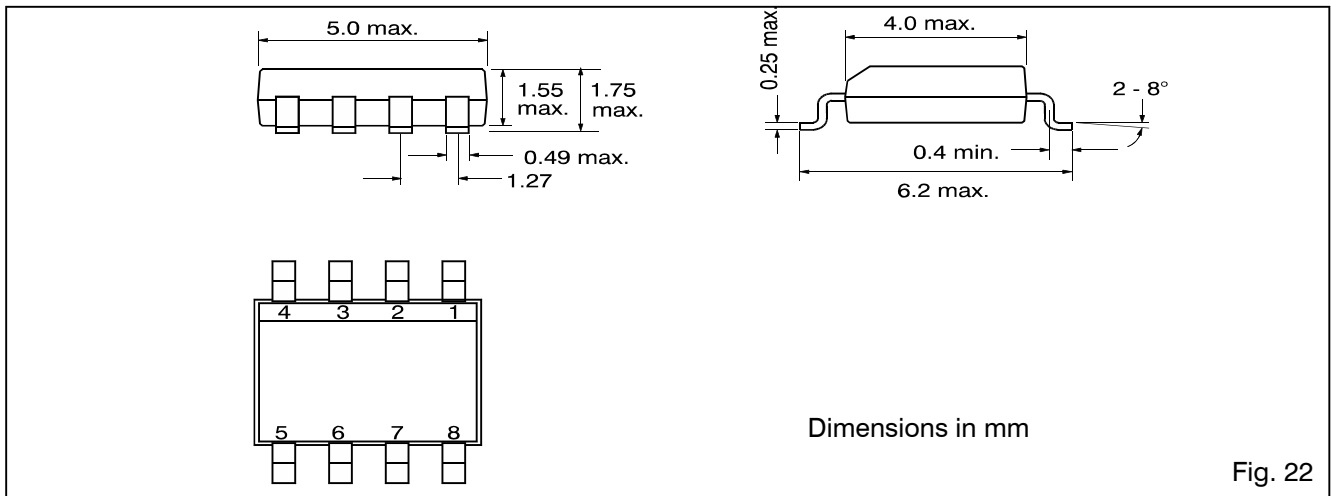


Package and Ordering Information

Dimensions of DIP8 Package



Dimensions of SO8 Package



Ordering Information

The V6130 is available in the following packages:

Type	Package
V6130 8P	DIP8
V6130 8S	SO8

When ordering please specify complete part number.

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