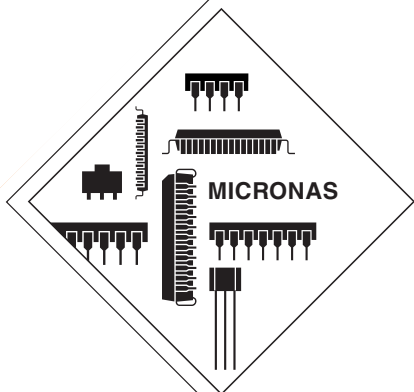


ADVANCE INFORMATION

VDP 313xY Video Processor Family



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Video Processor Family

1. Introduction

The VDP 313xY is a video IC family of high-quality single-chip video processors. Modular design and a sub-micron technology allow the economic integration of features in all classes of TV sets. The VDP 313xY family is based on the VDP 31xxB including YC_RC_B inputs for DVD component signals.

The main features of the VDP 3130Y are

1.1. Features

Video Decoding and Processing

- four CVBS, one S-VHS input, one YC_RC_B component input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- adaptive 2H comb filter Y/C separator
- multistandard color decoder PAL/NTSC/SECAM including all substandards
- multistandard sync decoder
- automatic standard recognition
- black-line detector
- linear horizontal scaling (0.25...4), as well as nonlinear horizontal scaling "Panoramavision"

- black-level expander
- dynamic peaking
- soft limiter (gamma correction)
- color transient improvement

RGB Processing and Deflection

- programmable RGB matrix
- two analog RGB / Fastblank inputs
- half-contrast switch
- picture frame generator
- scan velocity modulation output
- high-performance H/V deflection
- separate ADC for tube measurements
- EHT compensation
- angle and bow correction
- one 20.25 MHz crystal, few external components
- I²C-Bus Interface
- 64-pin PSDIP package

1.2. System Architecture

Fig. 1-1 shows the block diagram of the video processor

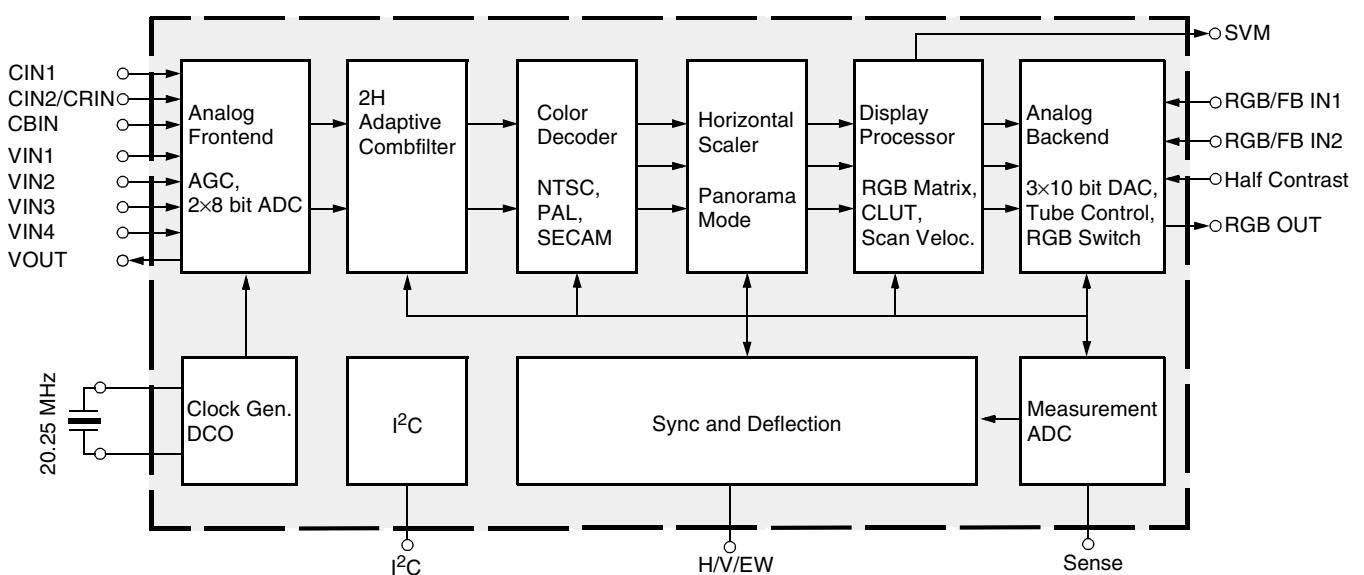


Fig. 1-1: Block diagram of the VDP 313xY

1.3. Video Processor Family

Each member of the family contains the entire video, display, and deflection processing for 4:3 and 16:9, 50/60 Hz TV sets. Its performance and flexibility allow the user to standardize his product development. Hardware and software applications can profit from the modularity, as well as manufacturing, systems support or maintenance. An overview of the VDP 313xY video processor family is shown in Fig. 1–2.

The new VDP 313xY family is the next generation of Video and Deflection Processors. The main differences towards the VDP 31xxB family are

- YC_RC_B component input
- angle and bow correction
- automatic standard recognition
- detection of Macrovision signals
- no dig. RGB interface for TPU 3050
- no stand-by input mode and CLK5 output
- minor changes of pinout

| VDP 313xY Family | 1H Combfilter | 2H adapt. Comb | Horizontal Scaler | Color Trans. Impr. | Scan Vel. Mod. | Prog. RGB Matrix | RGB Insertion | Tube Control |
|------------------|---------------|----------------|-------------------|--------------------|----------------|------------------|---------------|--------------|
| VDP 3134Y | ✓ | | | | | ✓ | ✓ | ✓ |
| VDP 3133Y | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ |
| VDP 3132Y | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ |
| VDP 3131Y | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| VDP 3130Y | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Fig. 1–2: VDP 313xY family overview

2. Functional Description

2.1. Introduction

The VDP 313xY includes complete video, display and deflection processing. All processing is done digitally, the video frontend and video backend are interfacing to the analog world. Most functions of the VDP can be controlled by software via I²C-Bus interface (see Section 2.14.1. on page 29).

2.2. Video Front End

This block provides the analog interfaces to all video inputs and mainly carries out analog-to-digital conversion for the following digital video processing. A block diagram is given in Fig. 2–1.

Most of the functional blocks in the front-end are digitally controlled (clamping, AGC, and clock-DCO). The control loops are closed by the Fast Processor (FP) embedded in the video decoder.

2.2.1. Input Selection

Up to seven analog inputs can be connected. Four inputs are for input of composite video or S-VHS luminance signal. These inputs are clamped to the sync back porch and are amplified by a variable gain amplifier. Two inputs are for connection of S-VHS carrier-chrominance signal. These inputs are internally biased and have a fixed gain amplifier. For analog YC_RC_B signals (e.g. from DVD players) the selected luminance input is used together with CBIN and CRIN.

2.2.2. Clamping

The composite video input signals are AC coupled to the IC. The clamping voltage is stored on the coupling capacitors and is generated by digitally controlled cur-

rent sources. The clamping level is the back porch of the video signal.

S-VHS chrominance is also AC coupled. The input pin is internally biased to the center of the ADC input range.

The chrominance inputs for YC_RC_B need to be AC coupled using clamping capacitors. It is strongly recommended to use 5 MHz anti-alias low-pass filters on each input. Each channel is sampled at 10.125 MHz with a resolution of 8 bit and a clamping level of 128.

2.2.3. Automatic Gain Control

A digitally working automatic gain control adjusts the magnitude of the selected baseband by +6/–4.5 dB in 64 logarithmic steps to the optimal range of the ADC. The gain of the video input stage including the ADC is 213 steps/V with the AGC set to 0 dB.

The gain of the chrominance path in the YC_RC_B mode is fix and adapted to a nominal amplitude of 0.7 V_{pp}. However, if an overflow of the ADC occurs an extended signal range of 1 V_{pp} can be selected.

2.2.4. Analog-to-Digital Converters

Two ADCs are provided to digitize the input signals. Each converter runs with 20.25 MHz and has 8 bit resolution. An integrated bandgap circuit generates the required reference voltages for the converters. The two ADCs are of a 2-stage subranging type.

2.2.5. Digitally Controlled Clock Oscillator

The clock generation is also a part of the analog front end. The crystal oscillator is controlled digitally by the control processor. The clock frequency can be adjusted within ±150 ppm.

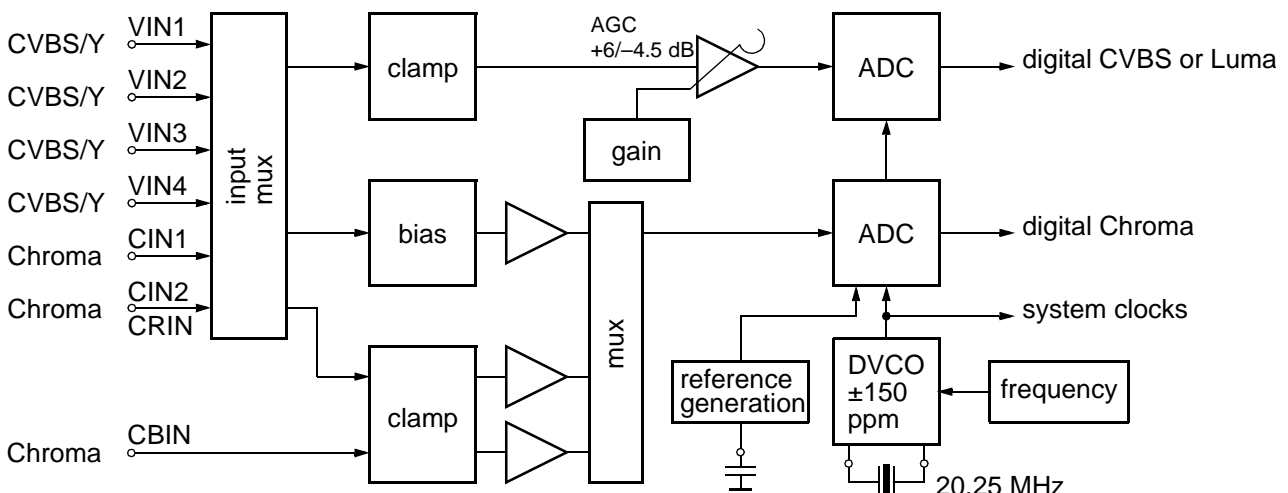


Fig. 2–1: Video front-end

2.3. Adaptive Comb Filter

The adaptive comb filter is used for high-quality luminance/chrominance separation for PAL or NTSC signals. The comb filter improves the luminance resolution (bandwidth) and reduces interferences like cross-luminance and cross-color artifacts. The adaptive algorithm can eliminate most of the mentioned errors without introducing new artifacts or noise.

A block diagram of the comb filter is shown in Fig. 2–1. The filter uses two line delays to process the information of three adjacent video lines. To have a fixed phase relationship of the color subcarrier in the three channels, the system clock (20.25 MHz) is fractionally locked to the color subcarrier. This allows the processing of all color standards and substandards using a single crystal frequency.

The CVBS signal in the three channels is filtered at the subcarrier frequency by a set of bandpass/notch filters. The output of the three channels is used by the adaption logic to select the weighting that is used to reconstruct the luminance/chrominance signal from the 4 bandpass/notch filter signals. By using soft mixing of the 4 signals switching artifacts of the adaption algorithm are completely suppressed.

The comb filter uses the middle line as reference, therefore, the comb filter delay is one line. If the comb filter is switched off, the delay lines are used to pass the luminance/ chrominance signals from the A/D converters to the luminance/ chrominance outputs. Thus, the comb filter delay is always one line.

Various parameters of the comb filter are adjustable, hence giving to the user the ability to adjust his own desired picture quality.

Two parameters (KY, KC) set the global gain of luminance and chrominance comb separately; these values directly weigh the adaption algorithm output. In this way, it is possible to obtain a luminance/chrominance separation ranging from standard notch/bandpass to full comb decoding.

The parameter KB allows to choose between the two proposed comb booster modes. This so-called feature widely improves vertical high to low frequency transitions areas, the typical example being a multiburst to dc change. For KB = 0, this improvement is kept moderate, whereas, in case of KB = 1, it is maximum, but the risk to increase the “hanging dots” amount for some given color transitions is higher.

Using the default setting, the comb filter has separate luminance and chrominance decision algorithms; it is however possible to switch the chrominance comb factor to the current luminance adaption output by setting CC to 1.

Another interesting feature is the programmable limitation of the luminance comb amount; proper limitation, associated to adequate luminance peaking, gives rise to an enhanced 2-D resolution homogeneity. This limitation is set by the parameter CLIM, ranging from 0 (no limitation) to 31 (max. limitation).

The DAA parameter (1:off, 0:on) is used to disable/enable a very efficient built-in “rain effect” suppressor; many comb filters show this side effect which gives some vertical correlation to a 2-D uniform random area, due to the vertical filtering. This unnatural-looking phenomenon is mostly visible on tuner images, since they are always corrupted by some noise; and this looks like rain.

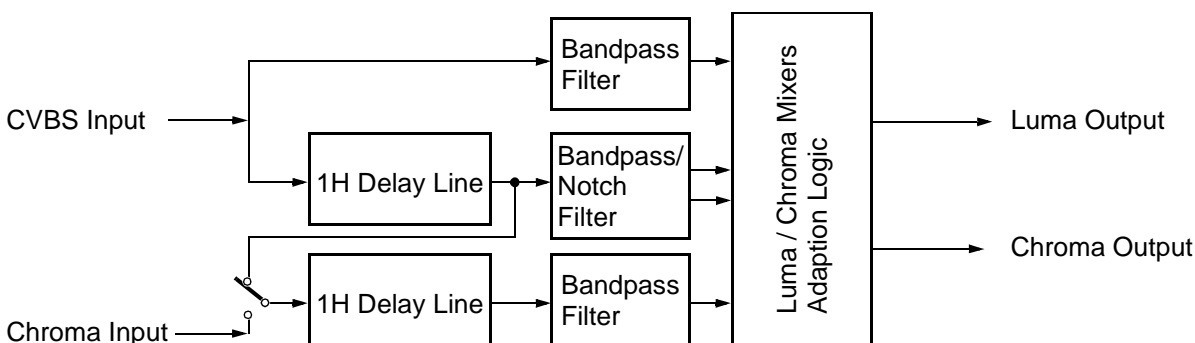


Fig. 2–1: Block diagram of the adaptive comb filter (PAL mode)

2.4. Color Decoder

In this block, the standard luminance/chrominance (luma/chroma) separation and multistandard color demodulation is carried out. The color demodulation uses an asynchronous clock, thus allowing a unified architecture for all color standards.

A block diagram of the color decoder is shown in Fig. 2-3. The luminance as well as the chrominance processing, is shown here. The color decoder provides also some special modes, e.g. wide band chrominance format which is intended for S-VHS wide bandwidth chrominance.

If the adaptive comb filter is used for luminance/chrominance separation, the color decoder uses the S-VHS mode processing. The output of the color decoder is $Y C_R C_B$ in a 4:2:2 format.

2.4.1. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Four different settings of the IF-compensation are possible:

- flat (no compensation)
- 6 dB/octave
- 12 dB/octave
- 10 dB/MHz

The last setting gives a very large boost to high frequencies. It is provided for SECAM signals that are decoded using a SAW filter specified originally for the PAL standard.

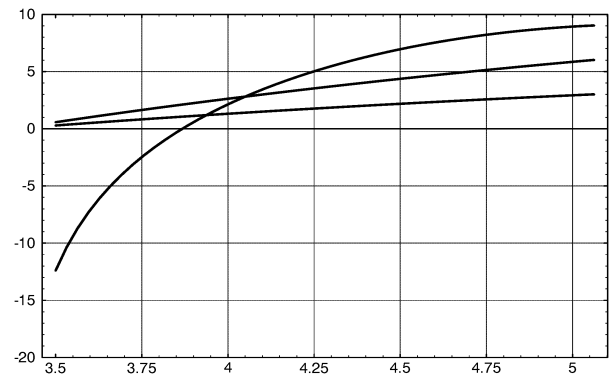


Fig. 2-2: Frequency response of chrominance IF-compensation

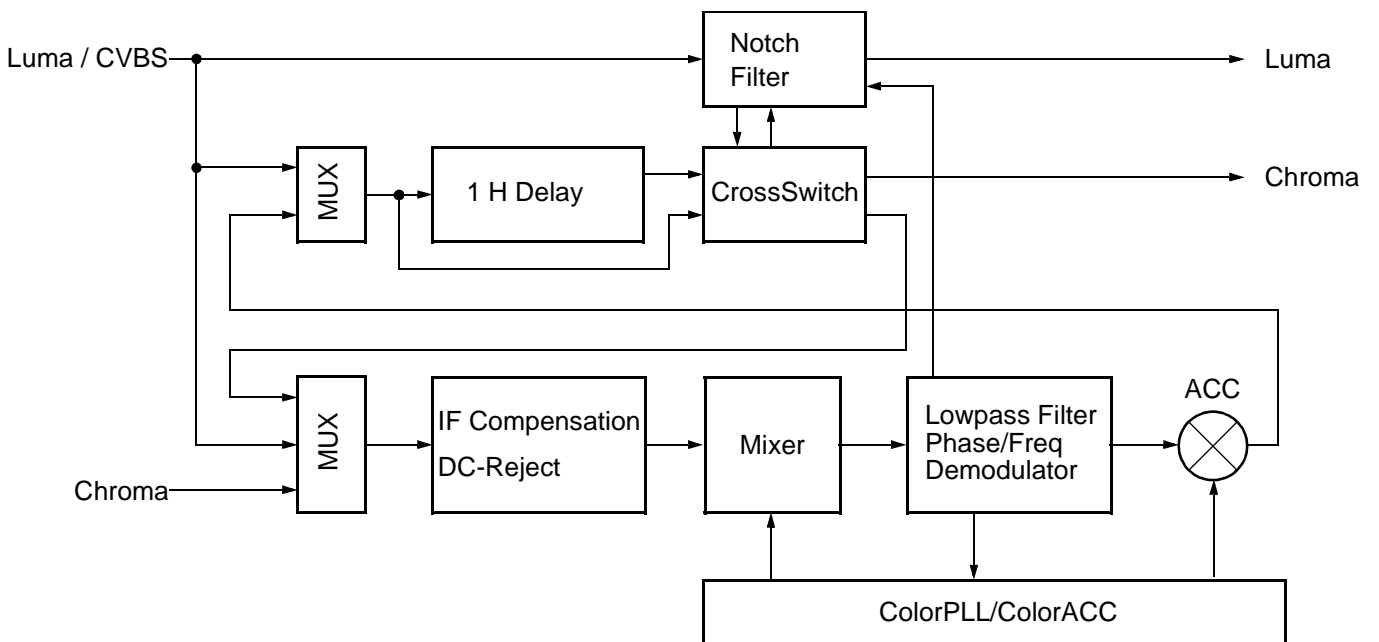


Fig. 2-3: Color decoder

2.4.2. Demodulator

The entire signal (which might still contain luminance) is now quadrature-mixed to the baseband. The mixing frequency is equal to the subcarrier for PAL and NTSC, thus achieving the chrominance demodulation. For SECAM, the mixing frequency is 4.286 MHz giving the quadrature baseband components of the FM modulated chrominance. After the mixer, a lowpass filter selects the chrominance components; a downsampling stage converts the color difference signals to a multiplexed half rate data stream.

The subcarrier frequency in the demodulator is generated by direct digital synthesis; therefore, substandards such as PAL 3.58 or NTSC 4.43 can also be demodulated.

2.4.3. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell-filter characteristic. At the output of the lowpass filter, all luminance information is eliminated.

The lowpass filters are calculated in time multiplex for the two color signals. Three bandwidth settings (narrow, normal, broad) are available for each standard. For PAL/NTSC, a wide band chrominance filter can be selected. This filter is intended for high bandwidth chrominance signals, e.g. a nonstandard wide bandwidth S-VHS signal.

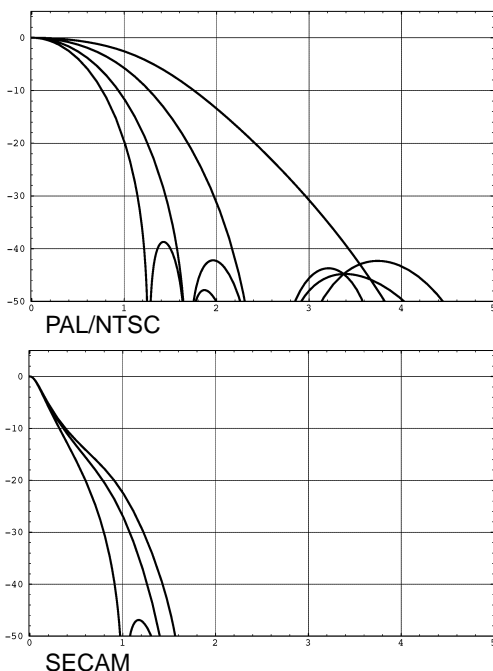


Fig. 2-4: Frequency response of chrominance filters

2.4.4. Frequency Demodulator

The frequency demodulator for demodulating the SECAM signal is implemented as a CORDIC-structure. It calculates the phase and magnitude of the quadrature components by coordinate rotation.

The phase output of the CORDIC processor is differentiated to obtain the demodulated frequency. After the deemphasis filter, the D_r and D_b signals are scaled to standard $C_R C_B$ amplitudes and fed to the cross-over-switch.

2.4.5. Burst Detection / Saturation Control

In the PAL/NTSC-system the burst is the reference for the color signal. The phase and magnitude outputs of the CORDIC are gated with the color key and used for controlling the phase-lock-loop (APC) of the demodulator and the automatic color control (ACC) in PAL/NTSC.

The ACC has a control range of +30...-6 dB.

Color saturation can be selected once for all color standards. In PAL/NTSC it is used as reference for the ACC. In SECAM the necessary gains are calculated automatically.

For SECAM decoding, the frequency of the burst is measured. Thus, the current chrominance carrier frequency can be identified and is used to control the SECAM processing. The burst measurements also control the color killer operation; they are used for automatic standard detection as well.

2.4.6. Color Killer Operation

The color killer uses the burst-phase/burst-frequency measurement to identify a PAL/NTSC or SECAM color signal. For PAL/NTSC, the color is switched off (killed) as long as the color subcarrier PLL is not locked. For SECAM, the killer is controlled by the toggle of the burst frequency. The burst amplitude measurement is used to switch-off the color if the burst amplitude is below a programmable threshold. Thus, color will be killed for very noisy signals. The color amplitude killer has a programmable hysteresis.

2.4.7. Automatic standard recognition

The burst-frequency measurement is also used for automatic standard recognition (together with the status of horizontal and vertical locking) thus allowing a completely independent search of the line and color standard of the input signal. The following standards can be distinguished:

- PAL B,G,H,I
- NTSC M
- SECAM
- NTSC 44
- PAL M
- PAL N
- PAL 60

For a preselection of allowed standards, the recognition can be enabled/disabled via I²C bus for each standard separately.

If at least one standard is enabled, the VDP 313xY checks regularly the horizontal and vertical locking of the input signal and the state of the color killer. If an error exists for several adjacent fields a new standard search is started. Depending on the measured line number and burst frequency the current standard is selected.

For error handling the recognition algorithm delivers the following status information:

- search active (busy)
- search terminated, but failed
- found standard is disabled
- vertical standard invalid
- no color found
- standard switched

2.4.8. PAL Compensation/1-H Comb Filter

The color decoder uses one fully integrated delay line. Only active video is stored.

The delay line application depends on the color standard:

- NTSC: 1-H comb filter **or** color compensation
- PAL: color compensation
- SECAM: crossover-switch

In the NTSC compensated mode, Fig. 2-5 c), the color signal is averaged for two adjacent lines. Thus, cross-color distortion and chrominance noise is reduced. In the NTSC combfilter mode, Fig. 2-5 d), the delay line is in the composite signal path, thus allowing reduction of cross-color components, as well as cross-luminance. The loss of vertical resolution in the luminance channel is compensated by adding the vertical detail signal with removed color information. If the 2-H adaptive comb filter is used, then the 1-H NTSC comb filter should not be used.

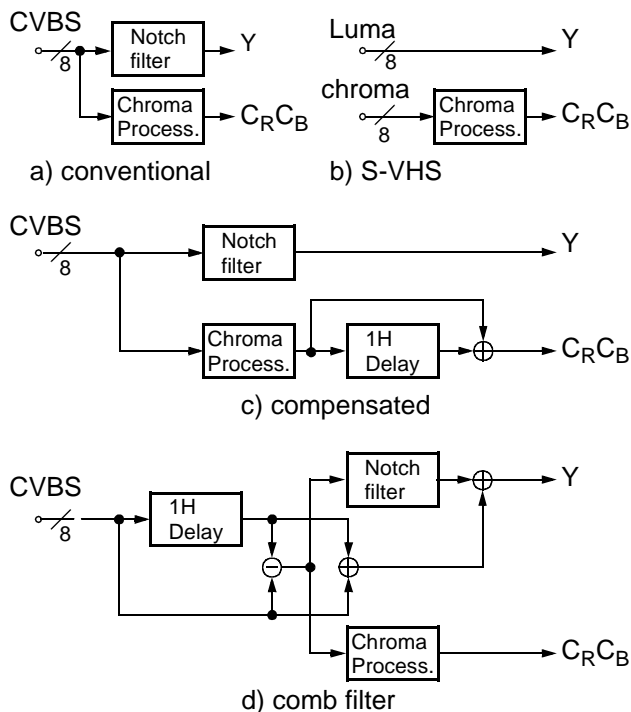


Fig. 2-5: NTSC color decoding options

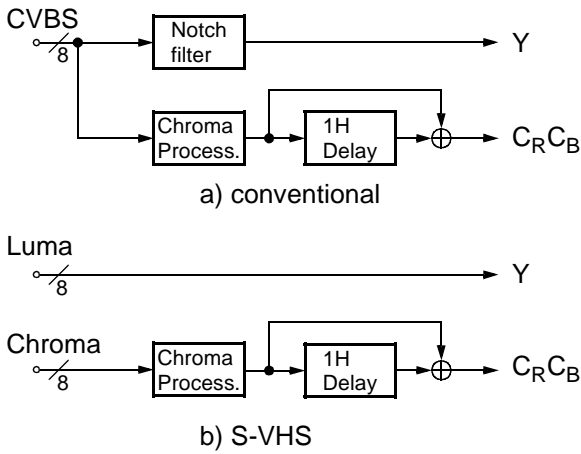


Fig. 2-6: PAL color decoding options

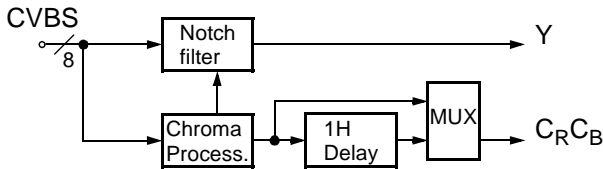
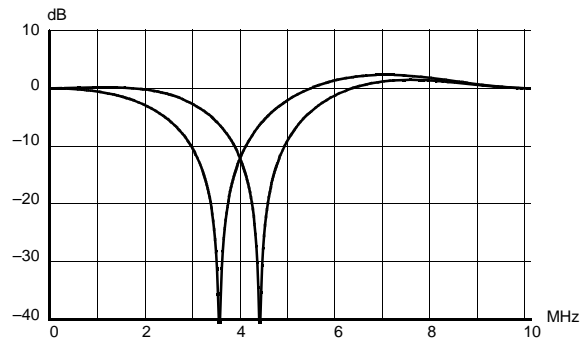


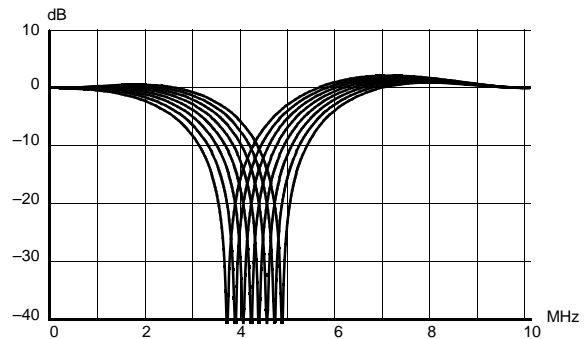
Fig. 2-7: SECAM color decoding

2.4.9. Luminance Notch Filter

If a composite video signal is applied, the color information is suppressed by a programmable notch filter. The position of the filter center frequency depends on the subcarrier frequency for PAL/NTSC. For SECAM, the notch is directly controlled by the chrominance carrier frequency. This considerably reduces the cross-luminance. The frequency responses for all three systems are shown in Fig. 2-8.



PAL/NTSC notch filter



SECAM notch filter

Fig. 2-8: Frequency responses of the luminance notch filter for PAL, NTSC, SECAM

2.4.10. Skew Filtering

The system clock is free-running and not locked to the TV line frequency. Therefore, the ADC sampling pattern is not orthogonal. The decoded $Y C_R C_B$ signals are converted to an orthogonal sampling raster by the skew filters, which are part of the scaler block.

The skew filters allow the application of a group delay to the input signals without introducing waveform or frequency response distortion.

The amount of phase shift of this filter is controlled by the horizontal PLL1. The accuracy of the filters is 1/32 clocks for luminance and 1/4 clocks for chrominance. Thus the 4:2:2 $Y C_R C_B$ data is in an orthogonal pixel format even in the case of nonstandard input signals such as VCR.

2.5. Horizontal Scaler

The 4:2:2 $Y_C_R C_B$ signal from the color decoder is processed by the horizontal scaler. The scaler block allows a linear or nonlinear horizontal scaling of the input video signal in the range of 0.25 to 4. Nonlinear scaling, also called panorama vision, provides a geometrical distortion of the input picture. It is used to fit a picture with 4:3 format on a 16:9 screen by stretching the picture geometry at the borders. Also, the inverse effect can be produced by the scaler. A summary of scaler modes is given in Table 2–1.

The scaler contains a programmable decimation filter, a 1-line FIFO memory, and a programmable interpolation filter. The scaler input filter is also used for pixel skew correction (see Section 2.4.10. on page 12). The decimator/interpolator structure allows optimal use of the FIFO memory. The controlling of the scaler is done by the internal Fast Processor.

Table 2–1: Scaler modes

| Mode | Scale Factor | Description |
|---------------------------|---------------------|--|
| Compression 4:3 → 16:9 | 0.75 linear | 4:3 source displayed on a 16:9 tube, with side panels |
| Panorama 4:3 → 16:9 | non-linear compr | 4:3 source displayed on a 16:9 tube, Borders distorted |
| Zoom 4:3 → 4:3 | 1.33 linear | Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan with cropping of side panels |
| Panorama 4:3 → 4:3 | non-linear zoom | Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan, borders distorted, no cropping |

2.6. Blackline Detector

In case of a letterbox format input video, e.g. Cinemascope, PAL+ etc., black areas at the upper and lower part of the picture are visible. It is suitable to remove or reduce these areas by a vertical zoom and/or shift operation.

The VDP 313xY supports this feature by a letterbox detector. The circuitry detects black video lines by measuring the signal amplitude during active video. For every field the number of black lines at the upper and lower part of the picture are measured, compared to the previous measurement and the minima are stored in the I²C-register BLKLIN. To adjust the picture amplitude, the external controller reads this register, calculates the vertical scaling coefficient and transfers the new settings, e.g. vertical sawtooth parameters, horizontal scaling coefficient etc., to the VDP 313xY.

Letterbox signals containing logos on the left or right side of the black areas are processed as black lines, while subtitles, inserted in the black areas, are processed as non-black lines. Therefore the subtitles are visible on the screen. To suppress the subtitles, the vertical zoom coefficient is calculated by selecting the larger number of black lines only. Dark video scenes with a low contrast level compared to the letterbox area are indicated by the BLKPIC bit.

2.7. Test Pattern Generator

The $Y_C_R C_B$ outputs can be switched to a test mode where $Y_C_R C_B$ data are generated digitally in the VDP 313xY. Test patterns include luminance/chrominance ramps and flat fields.

2.8. Video Sync Processing

Fig. 2–9 shows a block diagram of the front-end sync processing. To extract the sync information from the video signal, a linear phase lowpass filter eliminates all noise and video contents above 1 MHz. The sync is separated by a slicer; the sync phase is measured. A variable window can be selected to improve the noise immunity of the slicer. The phase comparator measures the falling edge of sync, as well as the integrated sync pulse.

The sync phase error is filtered by a phase-locked loop that is computed by the FP. All timing in the front-end is derived from a counter that is part of this PLL, and it thus counts synchronously to the video signal.

A separate hardware block measures the signal back porch and also allows gathering the maximum/minimum of the video signal. This information is processed by the FP and used for gain control and clamping.

For vertical sync separation, the sliced video signal is integrated. The FP uses the integrator value to derive vertical sync and field information.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and is distributed to the rest of the video processing system.

The data for the vertical deflection, the sawtooth, and the East-West correction signal is calculated by the VDP 313xY. The data is buffered in a FIFO and transferred to the back-end by a single wire interface.

Frequency and phase characteristics of the analog video signal are derived from PLL1. The results are fed to the scaler unit for data interpolation and orthogonalization and to the clock synthesizer for line-locked clock generation. Horizontal and vertical syncs are latched with the line-locked clock.

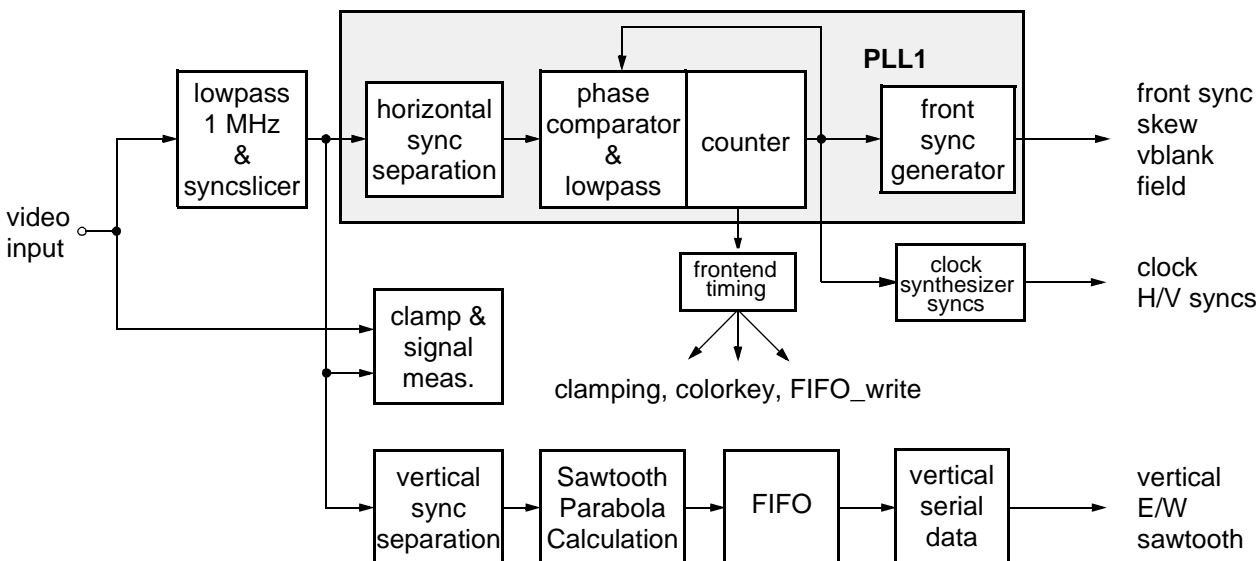


Fig. 2–9: Sync separation block diagram

2.9. Macrovision detection

Video signals from Macrovision encoded VCR tapes are decoded without loss of picture quality. However, it might be necessary in some applications to detect the presence of Macrovision encoded video signals. This is possible by reading the Macrovision status register (MCV_STATUS).

Macrovision encoded video signals typically have AGC pulses and pseudo sync pulses added during VBI. The amplitude of the AGC pulses is modulated in time. The Macrovision detection logic measures the VBI lines and compares the signal against thresholds.

The window in which the video lines are checked for Macrovision pulses can be defined in terms of start and stop line (e.g. 6-15 for NTSC).

2.10.Display Part

In the display part the conversion from digital $YC_R C_B$ to analog RGB is carried out (see Fig. 2-17 on page 20). In the luminance processing path, contrast and brightness adjustments and a variety of features, such as black level expansion, dynamic peaking and soft limiting, are provided. In the chrominance path, the $C_R C_B$ signals are converted to 4:4:4 format and filtered by a color transient improvement circuit. The $YC_R C_B$ signals are converted by a programmable matrix to RGB color space.

The display processor can switch between two separate control settings (main/side) for contrast, brightness and matrix coefficients.

2.10.1.Luminance Contrast Adjustment

The contrast of the luminance signal can be adjusted by multiplication with a 6-bit contrast value. The contrast value corresponds to a gain factor from 0 to 2, where the value 32 is equivalent to a gain of 1.

2.10.2.Black Level Expander

The black level expander enhances the contrast of the picture. Therefore the luminance signal is modified with an adjustable, non-linear function. Dark areas of

the picture are changed to black, while bright areas remain unchanged. The advantage of this black level expander is that the black expansion is performed only if it will be most noticeable to the viewer.

The black level expander works adaptively. Depending on the measured amplitudes L_{min} and L_{max} of the low-pass-filtered luminance (during a programmable vertical window) and an adjustable coefficient BTLT, a tilt point L_t is established by

$$L_t = L_{min} + BTLT \times (L_{max} - L_{min}).$$

Above this value there is no expansion, while all luminance values below this point are expanded according to:

$$L_{out} = L_{in} + BAM \times (L_{in} - L_t)$$

A second threshold, L_{tr} , can be programmed, above which there is no expansion. The characteristics of the black level expander are shown in Fig. 2-10 and Fig. 2-11.

The tilt point L_t is a function of the dynamic range of the video signal. Thus, the black level expansion is only performed when the video signal has a large dynamic range. Otherwise, the expansion to black is zero. This allows the correction of the characteristics of the picture tube.

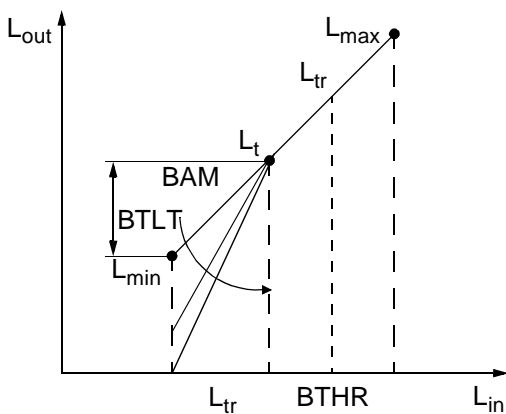


Fig. 2-10: Characteristics of the black level expander

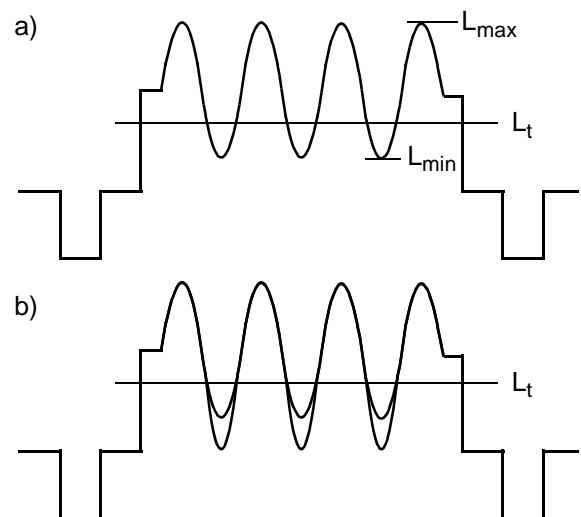


Fig. 2-11: Black-level-expansion
 a) luminance input
 b) luminance input and output

2.10.3. Dynamic Peaking

Especially with decoded composite signals and notch filter luminance separation, as input signals, it is necessary to improve the luminance frequency characteristics. With transparent, high-bandwidth signals, it is sometimes desirable to soften the image.

In the VDP 313xY, the luminance response is improved by dynamic peaking. The algorithm has been optimized regarding step and frequency response. It adapts to the amplitude of the high frequency part. Small AC amplitudes are processed, while large AC amplitudes stay nearly unmodified.

The dynamic range can be adjusted from -14 to +14 dB for small high frequency signals. There is separate adjustment for signal overshoot and for signal undershoot. For large signals, the dynamic range is limited by a non-linear function that does not create any visible alias components. The peaking can be switched over to "softening" by inverting the peaking term by software.

The center frequency of the peaking filter is switchable from 2.5 MHz to 3.2 MHz. For S-VHS and notch filter color decoding, the total system frequency responses for both PAL and NTSC are shown in Fig. 2-13.

Transients, produced by the dynamic peaking when switching to the picture frame can be suppressed optionally

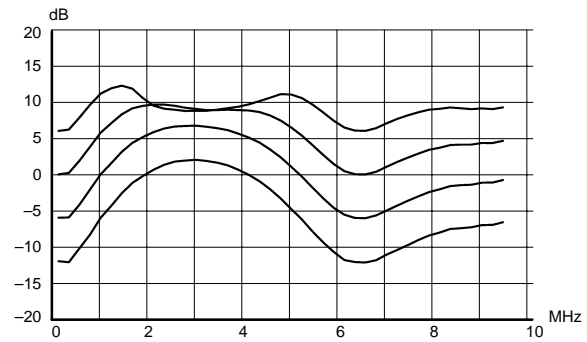


Fig. 2-12: Dynamic peaking frequency response

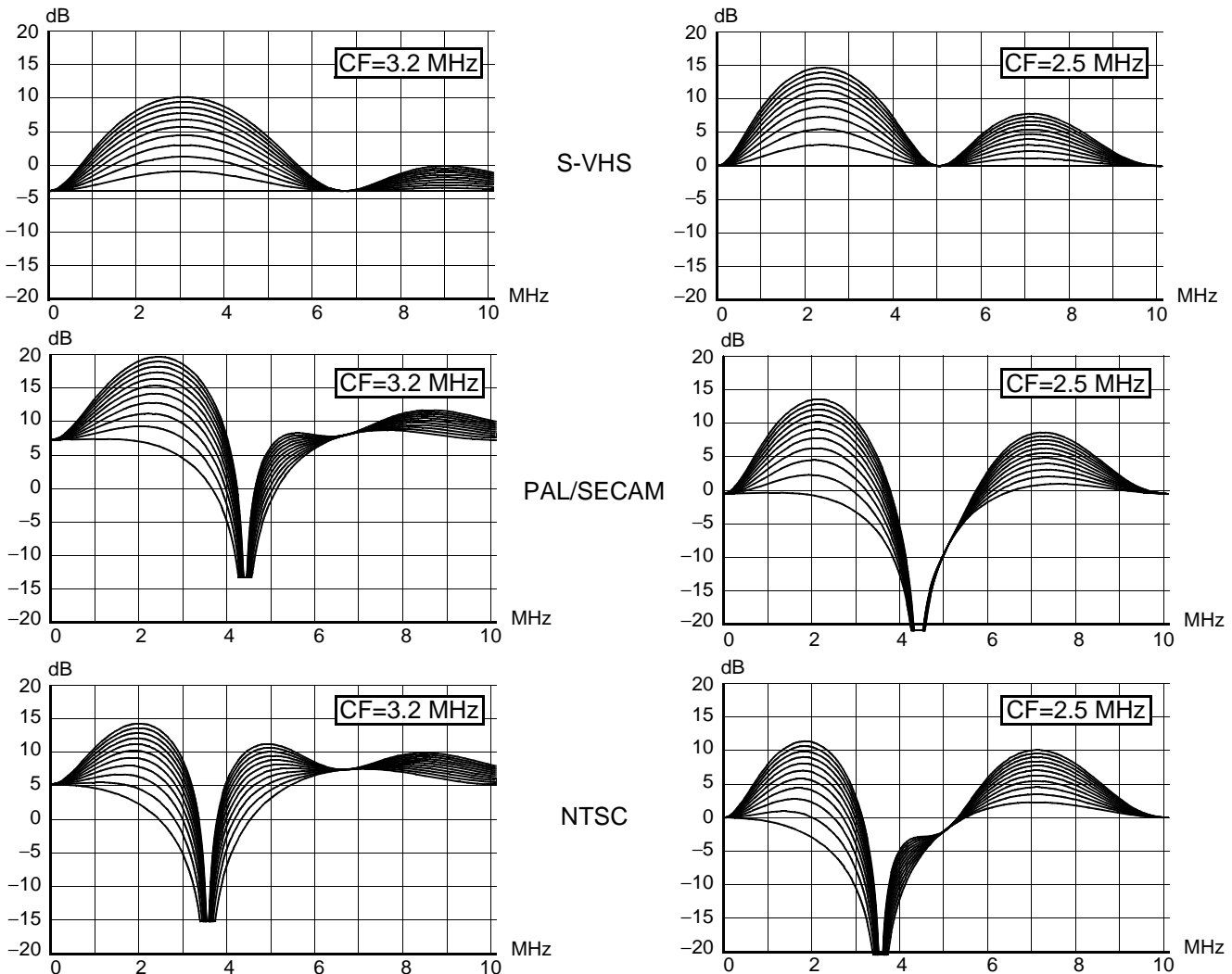


Fig. 2-13: Total frequency response for peaking filter and S-VHS, PAL, NTSC

2.10.4.Digital Brightness Adjustment

The DC-level of the luminance signal can be adjusted by adding/subtracting an 8-bit number in the luminance signal path in front of the softlimiter.

After the brightness addition, the negative going signals are limited to zero. It is desirable to keep a small positive offset with the signal to prevent undershoots produced by the peaking from being cut.

2.10.5.Soft Limiter

The dynamic range of the processed luminance signal must be limited to prevent the CRT from overload. An appropriate headroom for contrast, peaking and brightness can be adjusted by the TV manufacturer according to the CRT characteristics. All signals above this limit will be soft-clipped. A characteristic diagram of the soft limiter is shown in Fig. 2–14. The total limiter consists of three parts:

1. Part 1 includes adjustable tilt point and gain. The gain before the tilt value is 1. Above the tilt value, a part (0...15/16) of the input signal is subtracted from the input signal itself. Therefore the gain is adjustable from 16/16 to 1/16, when the slope value varies from 0 to 15. The tilt value can be adjusted from 0 to 511.
2. Part 2 has the same characteristics as part 1. The subtracting part is also relative to the input signal, so the total differential gain will become negative if the sum of slope 1 and slope 2 is greater than 16 and the input signal is above the both tilt values (see characteristics).
3. Finally, the output signal of the soft limiter will be clipped by a hard limiter adjustable from 256 to 511.

2.10.6.Chrominance Interpolation

A linear phase interpolator is used to convert the chrominance sampling rate from 10.125 MHz (4:2:2) to 20.25 MHz (4:4:4). All further processing is carried out at the full sampling rate.

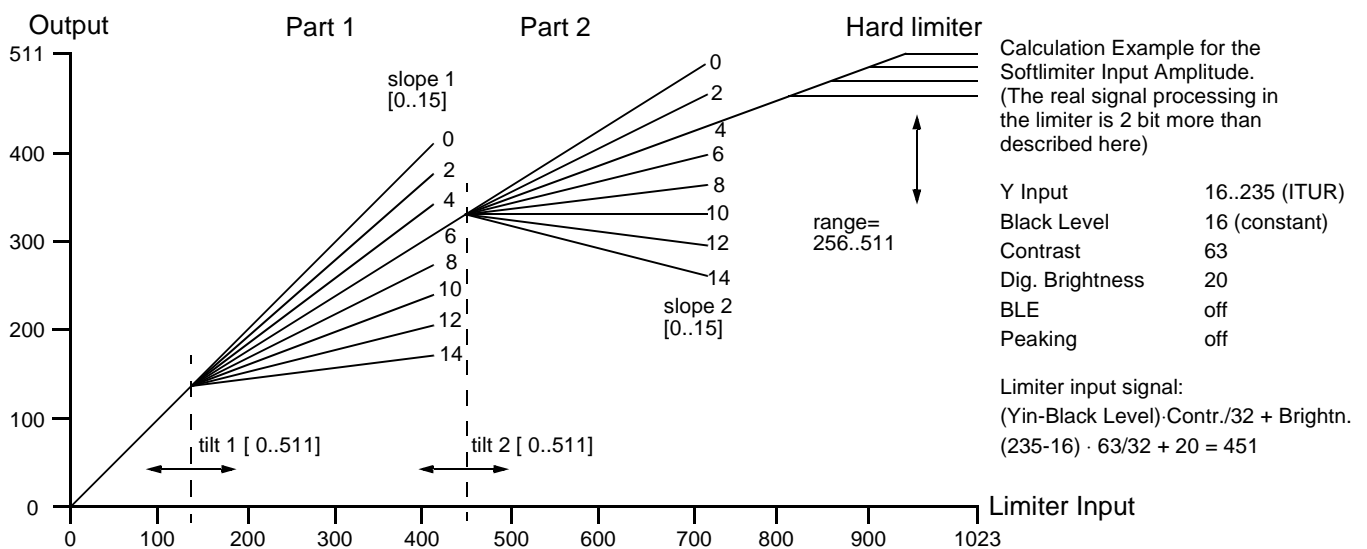


Fig. 2–14: Characteristic of soft limiter a and b and hard limiter

2.10.7. Chrominance Transient Improvement

The intention of this block is to enhance the chrominance resolution. A correction signal is calculated by differentiation of the color difference signals. The differentiation can be selected according to the signal bandwidth, e.g. for PAL/NTSC/SECAM or digital component signals, respectively. The amplitude of the correction signal is adjustable. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate ‘wrong colors’, which are caused by over and undershoots at the chrominance transition, the sharpened chrominance signals are limited to a proper value automatically.

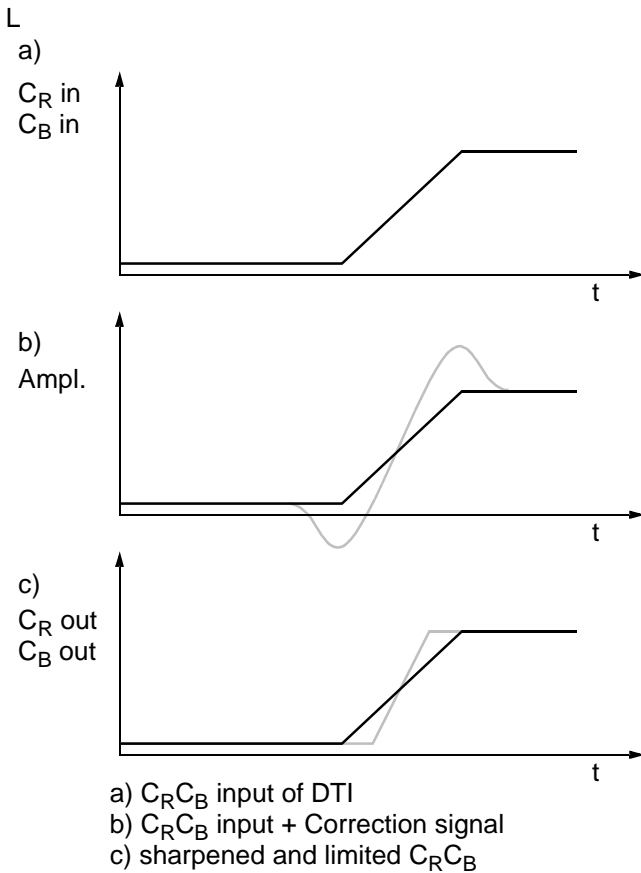


Fig. 2–15: Digital Color Transient Improvement

2.10.8. Inverse Matrix

A 6-multiplier matrix transcodes the C_R and C_B signals to R-Y, B-Y, and G-Y. The multipliers are also used to adjust color saturation in the range of 0 to 2. The coefficients are signed and have a resolution of 9 bits. The matrix computes:

$$\begin{aligned} R-Y &= MR1 \times C_B + MR2 \times C_R \\ G-Y &= MG1 \times C_B + MG2 \times C_R \\ B-Y &= MB1 \times C_B + MB2 \times C_R \end{aligned}$$

The initialization values for the matrix are computed from the standard ITUR (CCIR) matrix:

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.345 & -0.713 \\ 1 & 1.773 & 0 \end{pmatrix} \begin{pmatrix} Y \\ C_B \\ C_R \end{pmatrix}$$

For a contrast setting of CTM+32, the matrix values are scaled by a factor of 64 (see Table 2–5 on page 32).

2.10.9. RGB Processing

After adding the post-processed luminance, the digital RGB signals are limited to 10 bits. Three multipliers are used to digitally adjust the whitedrive. An average beam current limiter using the same multipliers is implemented (see Section 2.11.1. on page 21).

2.10.10. Picture Frame Generator

When the picture does not fill the total screen (height or width too small) it is surrounded with black areas. These areas (and more) can be colored with the picture frame generator. This is done by switching over the RGB signal from the matrix to the signal from the internal picture frame generator.

The width of each area (left, right, upper, lower) can be adjusted separately. The generator starts on the right, respectively lower side of the screen and stops on the left, respectively upper side of the screen. This means, it runs during horizontal, respectively vertical flyback. The color of the complete border can be programmed in the format 3×4 bit RGB. The contrast can be adjusted separately.

2.10.11. Priority Decoder

The priority decoder selects between the sources video, picture frame and analog RGB (OSD). The picture frame and the OSD can be enabled independently. The priority between picture frame and OSD is selectable. The video source always has the lowest priority. At the transitions between video and the picture frame the peaking transients can be suppressed optionally.

For the video source the black level expander can be activated and a fast switch between 2 settings (main/ side) for contrast, brightness and matrix values is possible.

2.10.12. Scan Velocity Modulation

The RGB input signal of the SVM is converted to Y in a simple matrix. Then the Y signal is differentiated by a filter of the transfer function $1-Z^{-N}$, where N is programmable from 1 to 6. With a coring, some noise can be suppressed. This is followed by a gain adjustment and an adjustable limiter. The analog output signal is generated by an 8-bit D/A converter.

The signal delay can be adjusted by ± 3.5 clocks in half- clock steps. For the gain and filter adjustment there are two parameter sets. The switching between these two sets is done with the same RGB switch signal that is used for switching between video-RGB and OSD-RGB for the RGB outputs (see Fig. 2-16).

2.10.13. Display Phase Shifter

A phase shifter is used to partially compensate the phase differences between the video source and the flyback signal. By using the described clock system, this phase shifter works with an accuracy of approximately 1 ns. It has a range of 1 clock period which is equivalent to ± 24.7 ns at 20.25 MHz. The large amount of phase shift (full clock periods) is realized in the front-end circuit.

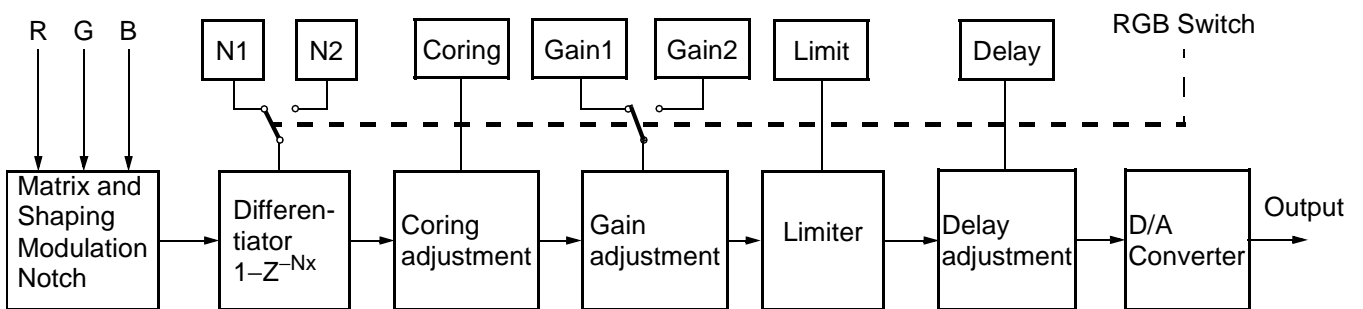


Fig. 2-16: SVM Block diagram

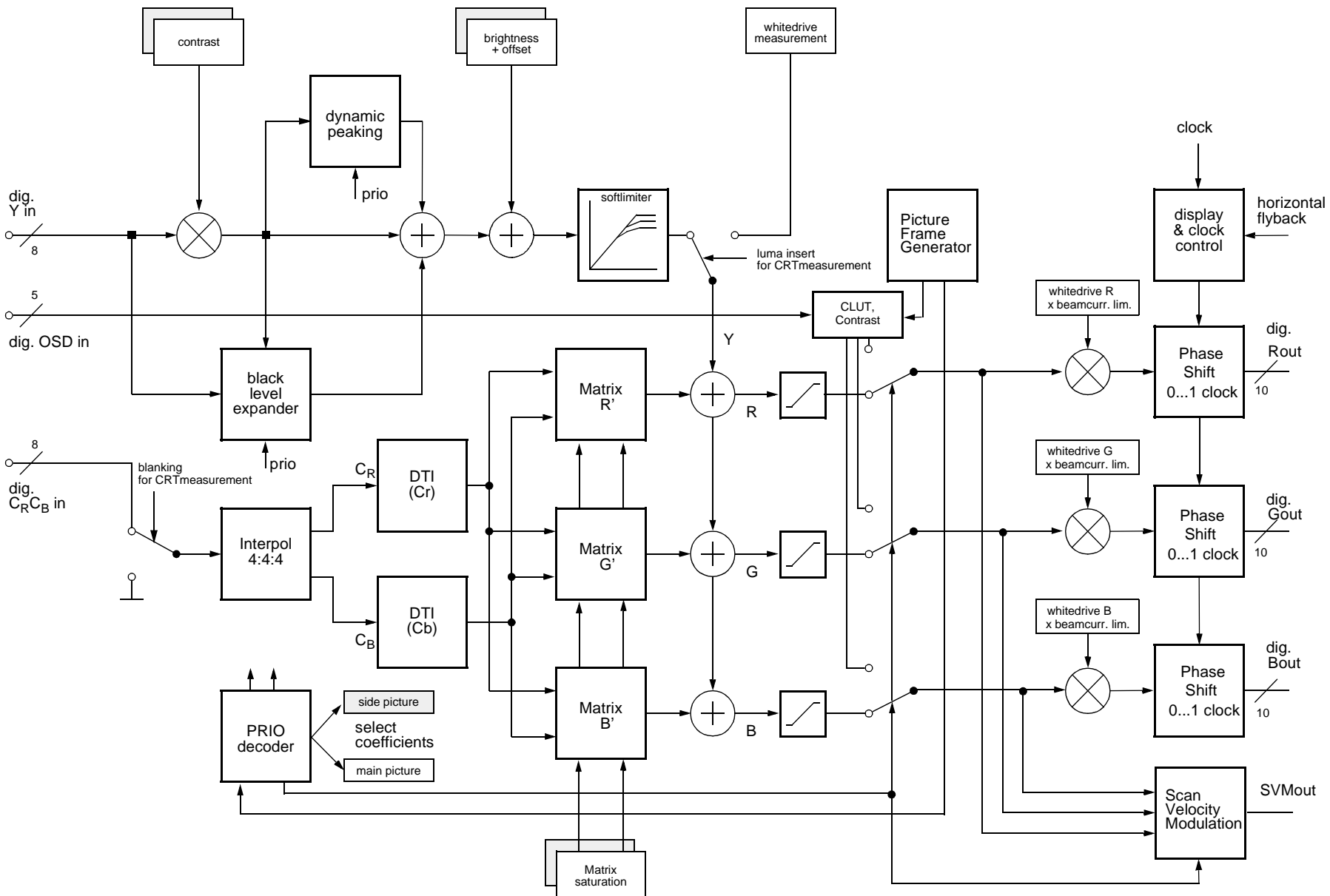


Fig. 2-17: Digital back-end

2.11.Video Back End

The digital RGB signals are converted to analog RGBs using three video digital to analog converters (DAC) with 10-bit resolution. An analog brightness value is provided by three additional DACs. The adjustment range is 40 % of the full RGB range.

Controlling the whitedrive/analog brightness and also the external contrast and brightness adjustments is done via the Fast Processor, located in the front-end. Control of the cutoff DACs is via I²C-bus registers.

Finally cutoff and blanking values are added to the RGB signals. Cutoff (dark current) is provided by three 9-bit DACs. The adjustment range is 60 % of full scale RGB range.

The analog RGB-outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB. An external half contrast signal can be used to reduce the output current of the RGB outputs to 50 %.

2.11.1.CRT Measurement and Control

The display processor is equipped with an 8-bit PDM-ADC for all measuring purposes. The ADC is connected to the sense input pin, the input range is 0 to 1.5 V. The bandwidth of the PDM filter can be selected; it is 40/80 kHz for small/large bandwidth setting. The input impedance is more than 1 MΩ.

Cutoff and whitedrive current measurement are carried out during the vertical blanking interval. They always use the small bandwidth setting. The current range for the cutoff measurement is set by connecting a sense resistor to the MADC input. For the whitedrive measurement, the range is set by using another sense resistor and the range select switch 2 output pin (RSW2). During the active picture, the minimum and maximum beam current is measured. The measurement range can be set by using the range select switch 1 pin (RSW1) as shown in Fig. 2-1 and Fig. 2-18. The timing window of this measurement is programmable. The intention is to automatically detect letterbox transmission or to measure the actual beam current. All control loops are closed via the external control micro-processor.

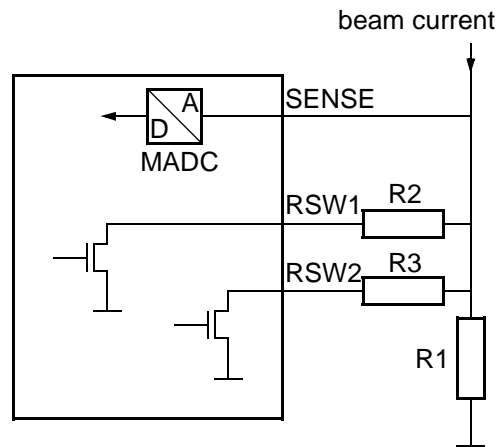


Fig. 2-1: MADC Range Switches

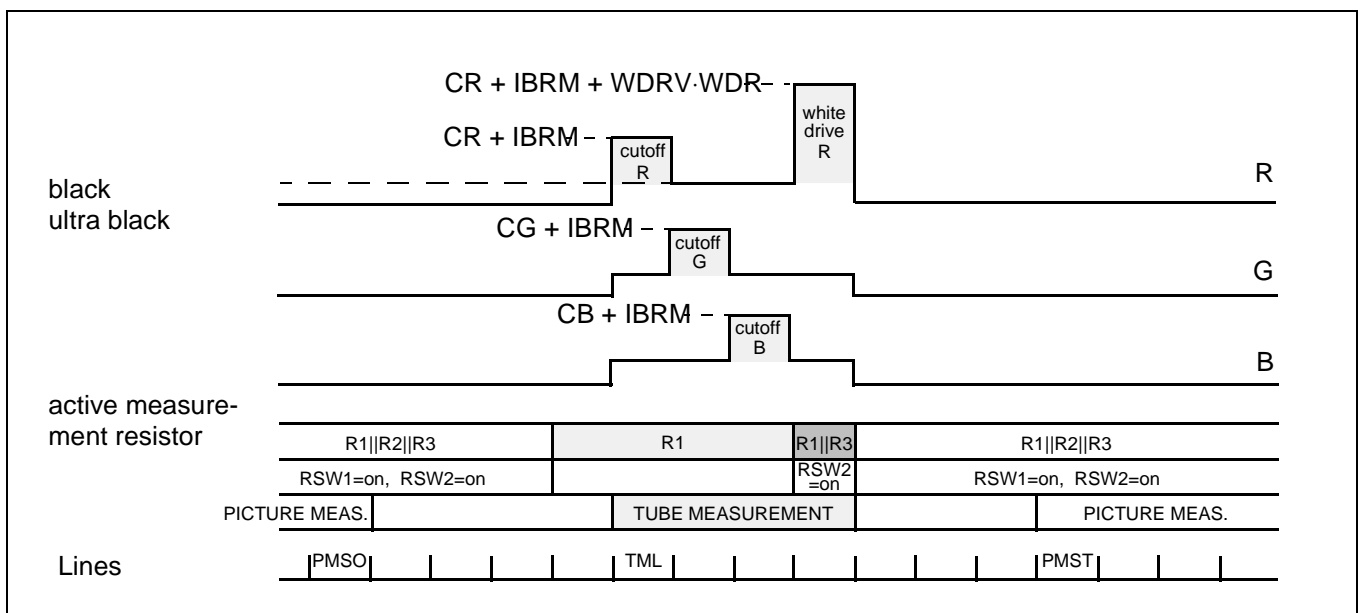


Fig. 2-18: MADC Measurement Timing

In each field two sets of measurements can be taken:

- a) The picture tube measurement returns results for
 - cutoff R
 - cutoff G
 - cutoff B
 - whitedrive R or G or B (sequentially)
- b) The picture measurement returns data on
 - active picture maximum current
 - active picture minimum current

The tube measurement is automatically started when the cutoff blue result register is read. Cutoff control for RGB requires one field only while a complete whitedrive control requires three fields. If the measurement mode is set to 'offset check', a measurement cycle is run with the cutoff/whitedrive signals set to zero. This allows to compensate the MADC offset as well as the input the leakage currents. During cutoff and whitedrive measurements, the average beam current limiter function (see Section 2.11.3. on page 23) is switched off and a programmable value is used for the brightness setting. The start line of the tube measurement can be programmed via I²C-bus, the first line used for the measurement, i.e. measurement of cutoff red, is 2 lines after the programmed start line.

The picture measurement must be enabled by the control microprocessor after reading the min./max. result registers. If a '1' is written into bit 2 in subaddress 25, the measurement runs for one field. For the next measurement a '1' has to be written again. The measurement is always started at the beginning of active video.

The vertical timing for the picture measurement is programmable, and may even be a single line. Also the signal bandwidth is switchable for the picture measurement.

Two horizontal windows are available for the picture measurement. The large window is active for the entire active line. Tube measurement is always carried out with the small window. Measurement windows for picture and tube measurement are shown in Fig. 2–19.

2.11.2. SCART Output Signal

The RGB output of the VDP 313xY can also be used to drive a SCART output. In the case of the SCART signal, the parameter CLMPR (clamping reference) has to be set to 1. Then, during blanking, the RGB outputs are automatically set to 50 % of the maximum brightness. The DC offset values can be adjusted with the cutoff parameters C_R , C_G , and C_B . The amplitudes can be adjusted with the drive parameters WDR, WDG, and WDB.

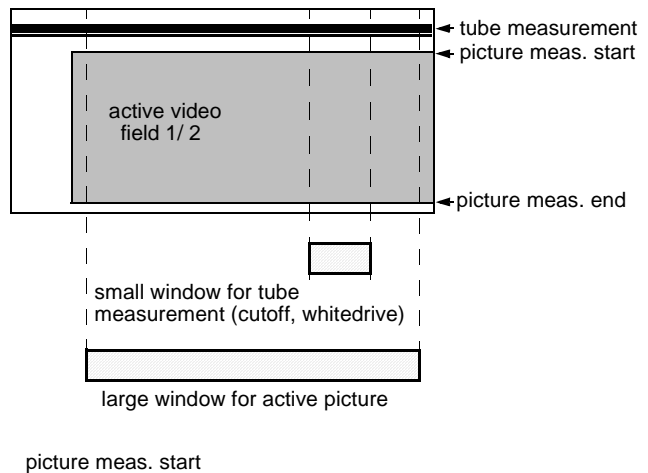


Fig. 2–19: Windows for tube and picture measurements

2.11.3. Average Beam Current Limiter

The average beam current limiter (BCL) uses the sense input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture. The filter bandwidth is approx. 2 kHz. The beam current limiter has an automatic offset adjustment that is active two lines before the first cutoff measurement line.

The beam current limiter function is located in the front-end. The data exchange between the front-end and the back-end is done via a single-wire serial interface.

The beam current limiter allows the setting of a threshold current. If the beam current is above the threshold, the excess current is lowpass filtered and used to attenuate the RGB outputs by adjusting the whitedrive multipliers for the internal (digital) RGB signals, and the analog contrast multipliers for the analog RGB inputs, respectively. The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. During the tube measurement, the ABL attenuation is switched off. After the whitedrive measurement line it takes 3 lines to switch back to BCL limited drives and brightness.

Typical characteristics of the ABL for different loop gains are shown in Fig. 2–20; for this example the tube has been assumed to have square law characteristics.

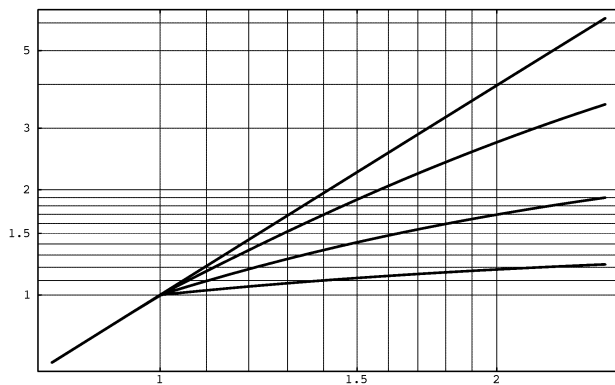


Fig. 2–20: Beam current limiter characteristics: beam current output vs. drive
BCL threshold: 1

2.11.4. Analog RGB Insertion

The VDP 313xY allows insertion of 2 external analog RGB signals. Each RGB signal is key-clamped and inserted into the main RGB by the fast blank switch. The selected external RGB input is virtually handled as a priority bus signal. Thus, it can be overlaid or underlaid to the digital picture. The external RGB signals can be adjusted independently as regards DC-level (brightness) and magnitude (contrast).

Which analog RGB input is selected depends on the fast blank input signals and the programming of a number of I²C-bus register settings (see Table 2–2 and Fig. 2–21). Both fast blank inputs must be either active-low or active-high.

All signals for analog RGB insertion (RIN1/2, GIN1/2, BIN1/2, FBLIN1/2, HCS) must be synchronized to the horizontal flyback, otherwise a horizontal jitter will be visible. The VDP 313xY has no means for timing correction of the analog RGB input signals.

Table 2–2: RGB Input Selection
FBFOH1=0, FBFOH2=0, FBFOL1=0, FBFOL2=0

| FBLIN1 | FBLIN2 | FBPOL | FBPRIO | RGB output |
|--------|--------|-------|--------|-------------|
| 0 | 0 | 0 | x | Video |
| 0 | 1 | 0 | x | RGB input 2 |
| 1 | 0 | 0 | x | RGB input 1 |
| 1 | 1 | 0 | 0 | RGB input 1 |
| 1 | 1 | 0 | 1 | RGB input 2 |
| 0 | 0 | 1 | 0 | RGB input 1 |
| 0 | 0 | 1 | 1 | RGB input 2 |
| 0 | 1 | 1 | x | RGB input 1 |
| 1 | 0 | 1 | x | RGB input 2 |
| 1 | 1 | 1 | x | Video |

2.11.5. Fast Blank Monitor

The presence of external analog RGB sources can be detected by means of a fast blank monitor. The status of the selected fast blank input can be monitored via an I²C bus register. There is a 2 bit information, giving static and dynamic indication of a fast blank signal. The static bit is directly reading the fast blank input line, whereas the dynamic bit is reading the status of a flip-flop triggered by the negative edge of the fast blank signal.

With this monitor logic it is possible to detect if there is an external RGB source active and if it is a full screen insertion or only a box. The monitor logic is connected directly to the FBLIN1 or FBLIN2 pin. Selection is done via I²C bus register.

2.11.6. Half Contrast Control

Insertion of transparent text pages or OSD onto the video picture is often difficult to read, especially if the video contrast is high. The VDP 313xY allows contrast reduction of the video background by means of a half contrast input (HCS pin). This input can be supplied with a fast switching signal (similar to the fast blank input), typically defining a rectangular box in which the video picture is displayed with reduced contrast. The analog RGB inputs are still displayed with full contrast.

2.11.7. IO Port Expander

The VDP 313xY provides a general purpose IO port to control and monitor up to seven external signals. The port direction is programmable for each bit individually. Via I²C bus register it is possible to write or read each port pin. Because of the relatively low I²C bus speed, only slow or static signals can be handled.

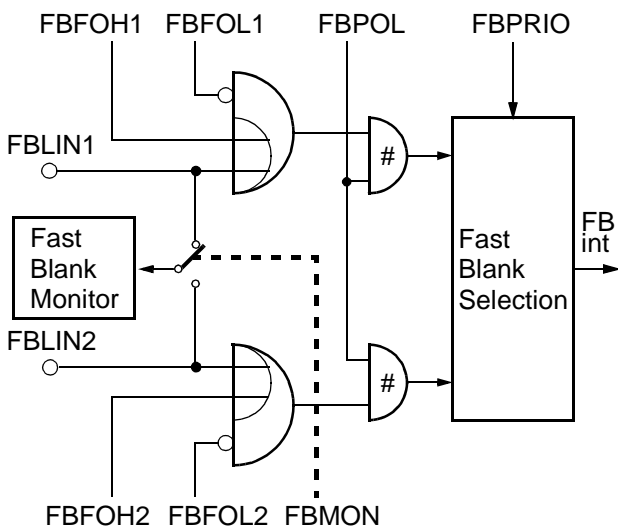


Fig. 2-21: Fast Blank Selection Logic

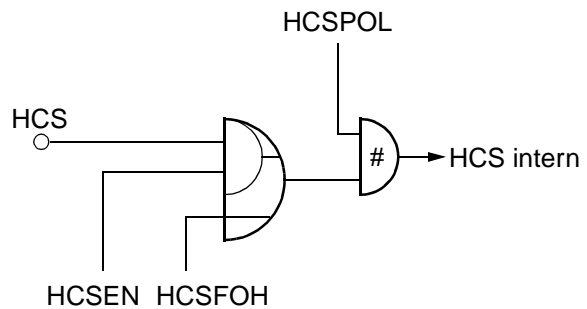


Fig. 2-22: Half Contrast Switch Logic

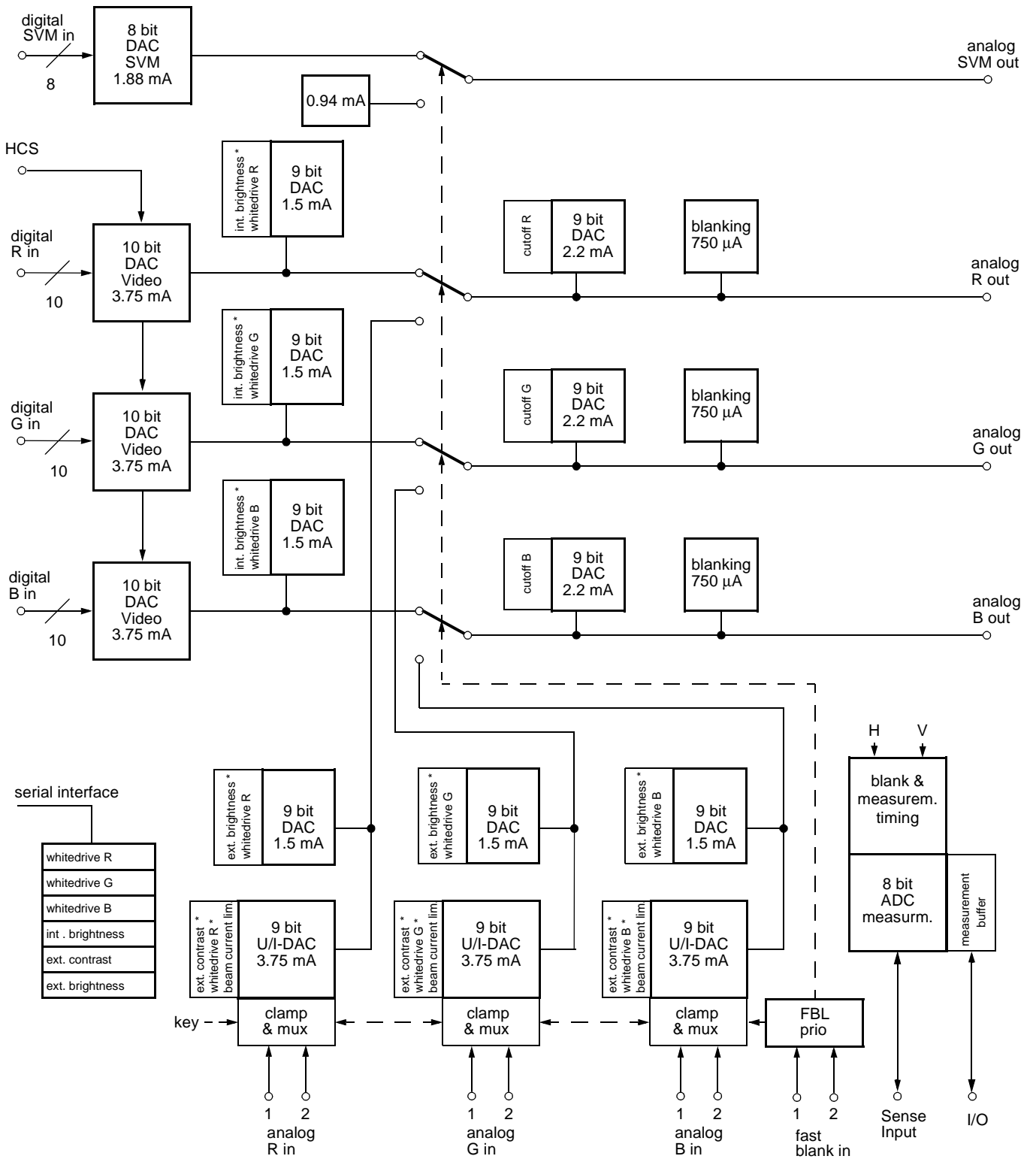


Fig. 2-23: Video back-end

2.12. Synchronization and Deflection

The synchronization and deflection processing is distributed over front-end and back-end. The video clamping, horizontal and vertical sync separation and all video related timing information are processed in the front-end. Most of the processing that runs at the horizontal frequency is programmed on the internal Fast Processor (FP). Also the values for vertical and East/West deflection are calculated by the FP software.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and distributed internally to the rest of the video processing system.

The data for the vertical deflection, the sawtooth and the East/West correction signal is calculated in the front end. The data is transferred to the back-end by a single wire interface.

The display related synchronization, i.e. generation of horizontal and vertical drive and synchronization of horizontal and vertical drive to the video timing

extracted in the front-end, are implemented in hardware in the back-end.

2.12.1. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (see Fig. 2–24). This block contains two phase-locked loops:

- PLL2 generates the horizontal and vertical timing, e.g. blanking, clamping and composite sync. Phase and frequency are synchronized by the front sync signal.
- PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage. Phase and frequency are synchronized by the oscillator signal of PLL2.

The horizontal drive circuitry uses a digital sine wave generator to produce the exact (subclock) timing for the drive pulse. The generator runs at 1 MHz; in the output stage the frequency is divided down to give drive-pulse period and width. The horizontal drive uses an open drain output transistor.

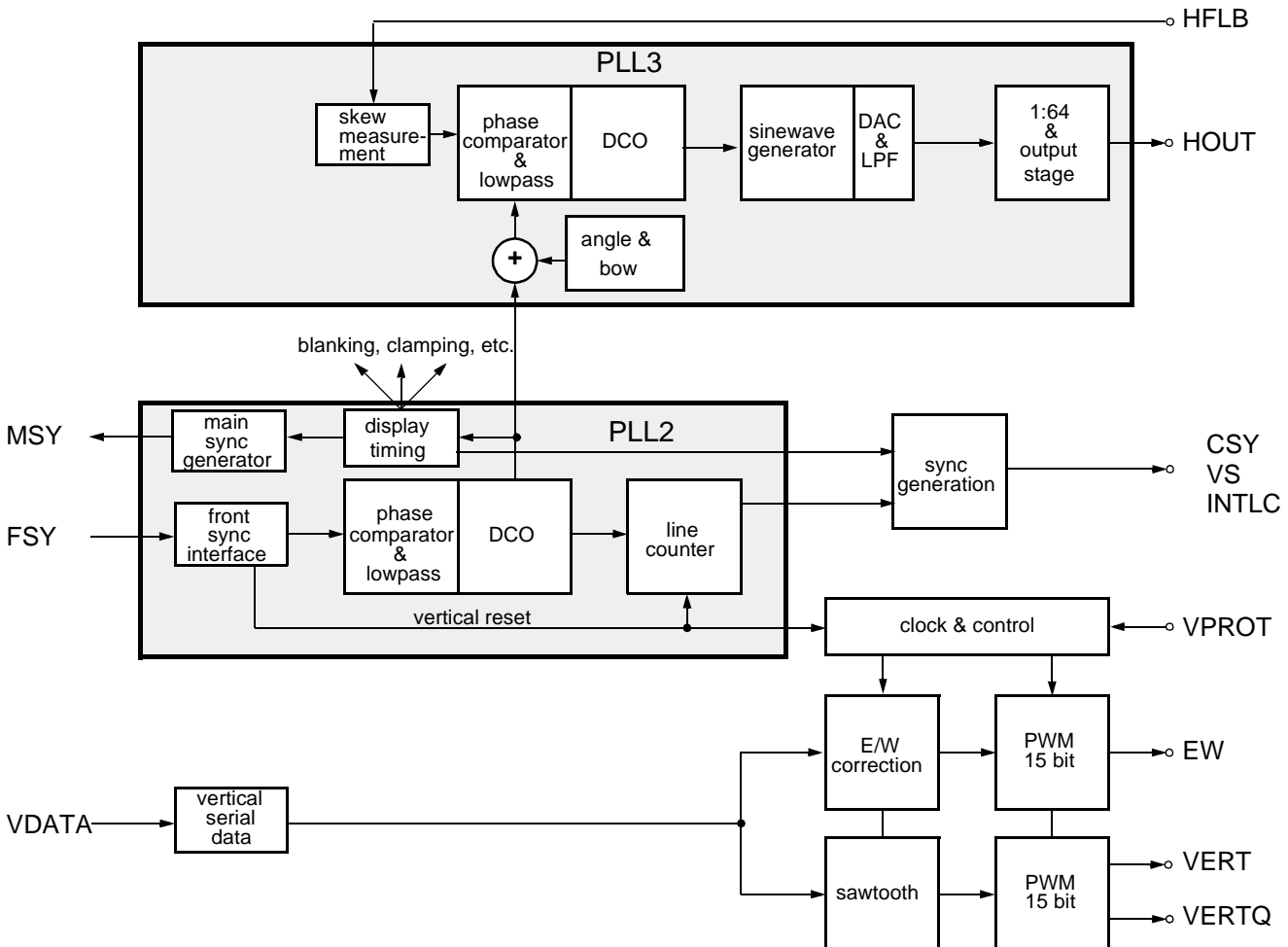


Fig. 2–24: Deflection processing block diagram

2.12.2.Angle & Bow Correction

The Angle & Bow correction is part of the horizontal drive PLL. This feature allows a shift of the horizontal drive pulse phase depending on the vertical position on the screen. The phase correction has a linear (angle) and a quadratic term (bow).

2.12.3.Horizontal Phase Adjustment

This section describes a simple way to align PLL phases and the horizontal frame position.

1. With HDRV the duration of the horizontal drive pulse has to be adjusted
2. With POFS2 the delay between input video and display timing (e.g. clamping pulse for analog RGB) has to be adjusted
3. With CSYDEL the delay between video and analog RGB (OSD) has to be adjusted.
4. With CSYDEL and HPOS the horizontal position of both, the digital and analog RGB signal (from SCART) relative to the clamping pulse has to be adjusted to the correct position, e.g. the pedestal of the generator signal.
5. With POFS3 the position of horizontal drive/flyback relative to RGB has to be adjusted
6. With NEWLIN the position of a scaled video picture can be adjusted (left, middle, center, etc; versions with panorama scaler only).
7. With HBST and HBSO, the start and stop values for the horizontal blanking have to be adjusted.

Note: The processing delay of the internal digital video path differs depending on the comb filter option of the VDP 313xY. The versions with comb filter have an additional delay of 34 clock cycles.

2.12.4.Vertical and East/West Deflection

The calculations of the vertical and East/West deflection waveforms is done by the internal Fast Processor (FP). The algorithm uses a chain of accumulators to generate the required polynomial waveforms. To produce the deflection waveforms, the accumulators are initialized at the beginning of each field. The initialization values must be computed by the TV control processor and are written to the front-end once. The waveforms are described as polynomials in x, where x varies from 0 to 1 for one field.

$$P: a + b(x-0.5) + c(x-0.5)^2 + d(x-0.5)^3 + e(x-0.5)^4$$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for East/West deflection are 12-bit values.

Fig. 2–25 shows several vertical and East/West deflection waveforms. The polynomial coefficients are also stated.

In order to get a faster vertical retrace timing, the output impedance of the vertical D/A-converter is reduced during the retrace.

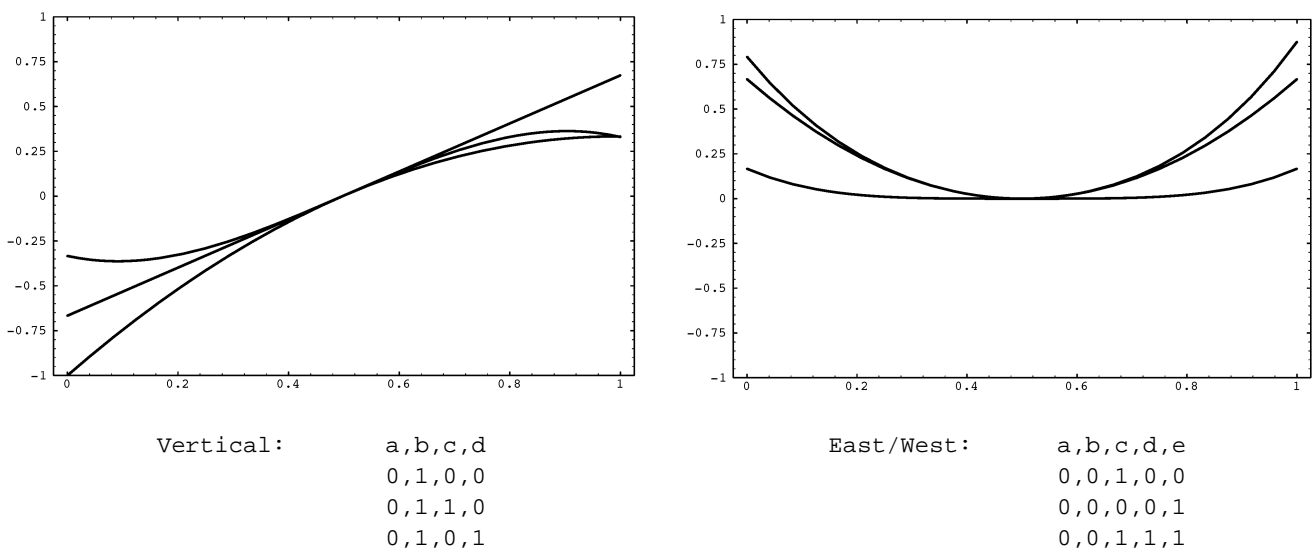


Fig. 2–25: Vertical and East/West Deflection Waveforms

2.12.5.EHT Compensation

The vertical waveform can be scaled according the average beam current. This is used to compensate the effects of electric high tension changes due to beam current variations. EHT compensation for East/West deflection is done with an offset corresponding to the average beam current.

2.12.6.Protection Circuitry

- Picture tube and drive stage protection is provided through the following measures:
- Vertical flyback protection input: this pin searches for a negative edge in every field, otherwise the RGB drive signals are blanked.
- Drive shutoff during flyback: this feature can be selected by software.
- Safety input pin: this input has two thresholds. Between zero and the lower threshold, normal functioning takes place. Between the lower and the higher threshold, the RGB signals are blanked. Above the higher threshold, the RGB signals are blanked and the horizontal drive is shut off. Both thresholds have a small hysteresis.
- The main oscillator and the horizontal drive circuitry are run from a separate (standby) power supply and are already active while the TV set is powering up.

2.13.Reset and Power On

Reset of most VDP 313xY functions is performed by the RESQ pin. When this pin becomes active all internal registers and counters are lost. When the RESQ pin is released, the internal reset is still active for 4 μ s. After that time, the initialization of all required registers is performed by the internal Fast Processor.

The VDP 313xY has clock and voltage supervision circuits to generate a stable HOUT signal. The voltage supervision activates an internal reset signal when the supply for the digital circuits ($VSUP_D$) goes below ~ 2.5 V for more than 50 ns. This reset signal is extended by 50 μ s after $VSUP_D$ is back again.

After power on or reset the HOUT generation is switched to a freerunning mode with a fix duty cycle of 50 %. For normal operation the EHPLL bit has to be set first. During the switch the actual period of HOUT can vary by up to 1 μ s.

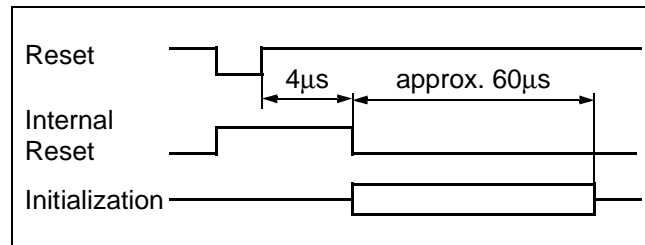


Fig. 2–26: External Reset

2.14. Serial Interface

2.14.1. I²C-Bus Interface

Communication between the VDP and the external controller is done via I²C-bus. The VDP has two I²C-bus slave interfaces (for compatibility with VPC/DDP applications) - one in the front-end and one in the back-end. Both I²C-bus interfaces use I²C clock synchronization to slow down the interface if required. Both I²C-bus interfaces use one level of subaddress: the I²C-bus chip address is used to address the IC and a subaddress selects one of the internal registers. The I²C-bus chip addresses are given below:

Table 2-3: I²C Chip Addresses

| Chip Address | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|--------------|----|----|----|----|----|----|----|-----|
| front-end | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1/0 |
| back-end | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1/0 |

The registers of the VDP have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

Fig. 2-27 shows I²C-bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

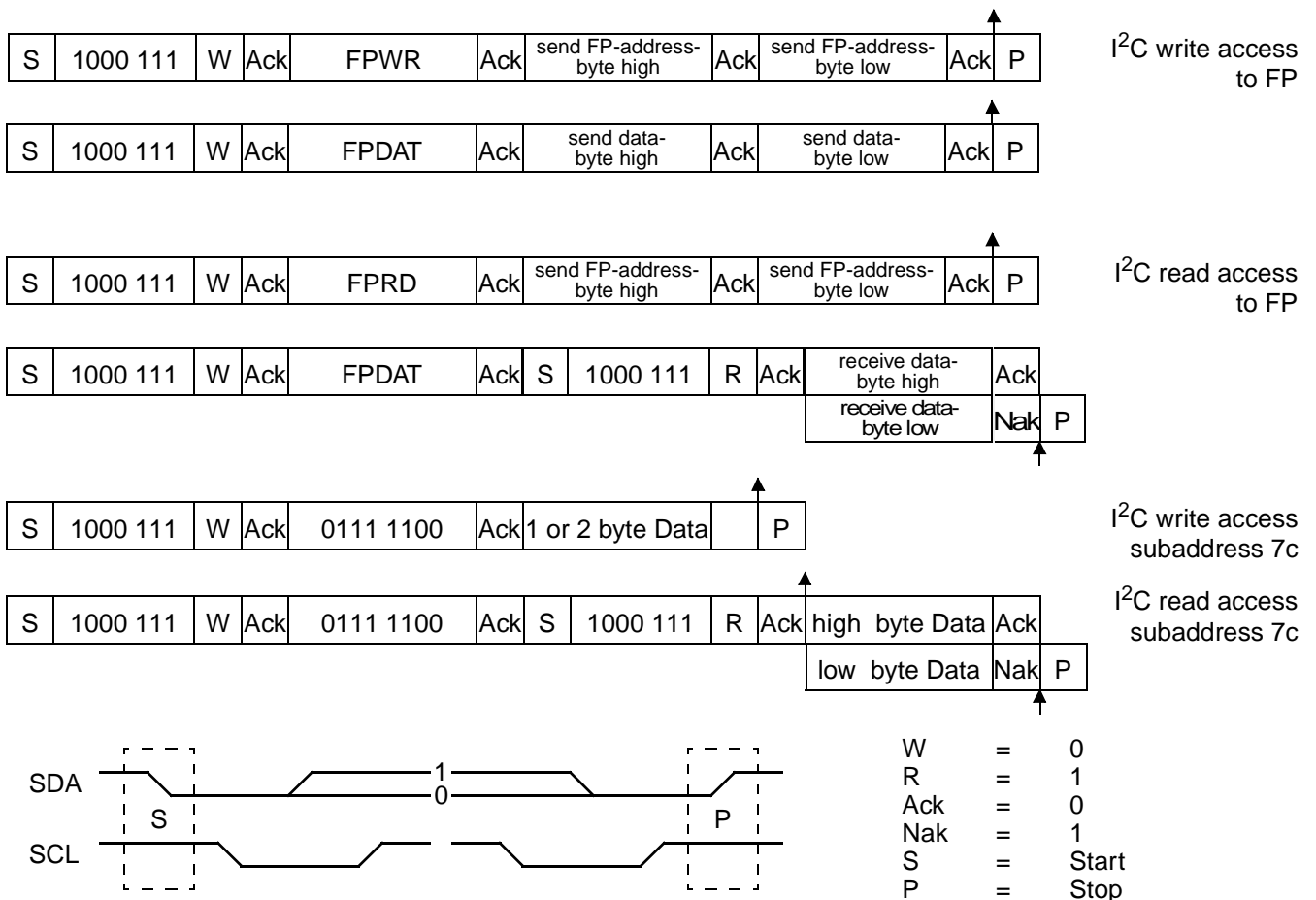


Fig. 2-27: I²C-bus protocols

2.14.2. Control and Status Registers

Table 2–4 gives definitions of the VDP control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware, i.e. a 9-bit register must always be accessed using two data bytes but the 7 MSB will be 'don't care' on write operations and '0' on read operations. Write registers that can be read back are indicated in Table 2–4.

Functions implemented by software in the on-chip control microprocessor (FP) are explained in Table 2–6.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 2–4.

The register modes given in Table 2–4 are

- w: write only register
- w/r: write/read data register
- r: read data from VPC
- v: register is latched with vertical sync
- h: register is latched with horizontal sync

Table 2–4: I²C control and status registers of the video frontend

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|--|---------------|-------------------------------------|
| FP Interface | | | | | |
| 35 | 8 | r | FP status bit[0] write request bit[1] read request bit[2] busy | | FPSTA |
| 36 | 16 | w | bit[8:0] 9-bit FP read address bit[11:9] reserved, set to zero | | FPRD |
| 37 | 16 | w | bit[8:0] 9-bit FP write address bit[11:9] reserved, set to zero | | FPWR |
| 38 | 16 | w/r | bit[11:0] FP data register, reading/writing to this register will autoincrement the FP read/write address. Only 16 bit of data are transferred per I ² C teleamm. | | FPDAT |
| Black Line Detector | | | | | |
| 12 | 16 | r | read only register, do not write to this register! after reading, LOWLIN and UPLIN are reset to 127 to start a new measurement bit[6:0] number of lower black lines bit[7] always 0 bit[14:8] number of upper black lines bit[15] normal/black picture | – | BLKLIN LOWLIN UPLIN BLKPIC |

Table 2–4: I²C control and status registers of the video frontend

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|---|------------------|-------------------------|
| Miscellaneous | | | | | |
| 29 | 16 | w/r | Test pattern generator: bit[10:0] reserved (set to 0) bit[11] 0/1 disable/enable test pattern generator bit[13:12] output mode: 00 Y/C = ramp (240 ... 17) 01 Y/C = 16 10 Y/C = 90 11 Y/C = 240 bit[15:14] 0/1 reserved (set to 0) | 0 0 0 0 | TPG TPGEN TPGMODE |
| 22 | 16 | w/r | NEWLINE (available for versions with panorama scaler only): bit[10:0] NEWLINE register This register defines the readout start of the next line in respect to the value of the sync counter. Value of this register must be greater than 31 for correct operation. bit[15:11] reserved (set to 0) | 50 | NEWLIN |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|--|---------------|------------------------------|
| Luminance Channel | | | | | |
| 61 | 9 | w v | bit[5:0] 0..63/32 main contrast setting | 32 | CTM |
| 65 | 9 | w v | bit[5:0] 0..63/32 side contrast setting | 32 | CTS |
| 51 | 9 | w v | bit[8:0] –256..255 main brightness setting | 0 | BRM |
| 55 | 9 | w v | bit[8:0] –256..255 side brightness setting | 0 | BRS |
| 7D | 9 | w v | bit[7] 0/1 enable/disable black level expander | 0 | BLE |
| 59 | 9 | w v | black level expander: bit[3:0] 0..15 tilt coefficient bit[8:4] 0..31 amount | 8 12 | BLE1 BTLT BAM |
| 5D | 9 | w v | black level expander: bit[8:0] 0..511 disable expansion, threshold value | 200 | BLE2 BTHR |
| 73 | 9 | w v | black level expander measurement bit[7:0] 0..255 vstart bit[8] 0/1 50/60 Hz measurement windowlength start line = vstart stop line = 336/283 – vstart (or vertical sync) | 0 15 | BLE3 BWL BVST |
| 69 | 9 | w v | luma peaking filter, the gain at high frequencies and small signal amplitudes is: $1 + (k1+k2)/8$ bit[3:0] 0..15 k1: peaking level undershoot bit[7:4] 0..15 k2: peaking level overshoot bit[8] 0/1 peaking value normal/inverted (peaking/softening) | 4 4 0 | PK1 PKUN PKOV PKINV |
| 6D | 9 | w v | luma peaking filter, coring bit[4:0] 0..31 coring level bit[7:5] reserved bit[8] 0/1 peaking filter center frequency high/low | 3 0 | PK2 COR PFS |
| 41 | 9 | w v | luma soft limiter, slope A and B bit[3:0] slope segment A bit[7:4] slope segment B | 0 0 | LSL1 LSLSA LSLSB |
| 45 | 9 | w v | luma soft limiter, absolute limit bit[7:0] luma soft limiter absolute limit (unsigned) bit[8] 0/1 modulation off/on | 255 1 | LSL2 LSLAL LSLM |
| 4D | 9 | w v | bit[8:0] luma soft limiter segment A tilt point (unsigned) | 250 | LSLTA |
| 49 | 9 | w v | bit[8:0] luma soft limiter segment B tilt point (unsigned) | 300 | LSLTB |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|--|---------------|--------------------------------|
| Chrominance Channel | | | | | |
| 14 | 8 | w/r | luma/chroma matching delay bit[2:0] –3...3 variable chroma delay bit[7:3] reserved, set to 0 | 0 | LCM CDEL |
| 5E | 9 | w v | digital transient improvement bit[3:0] 0..15 coring value bit[7:4] 0..15 DTI gain bit[8] 0/1 narrow/wide bandwidth mode | 1 5 1 | DTI DTICO DTIGA DTIMO |
| Inverse Matrix | | | | | |
| 7C | 9 | w v | main matrix coefficient R–Y = MR1M×C _B +MR2M×C _R bit[8:0] –256/128 ... 255/128 | 0 | MR1M, |
| 74 | 9 | w v | bit[8:0] –256/128 ... 255/128 | 86 | MR2M |
| 6C | 9 | w v | main matrix coefficient G–Y = MG1M×C _B +MG2M×C _R bit[8:0] –256/128 ... 255/128 | –22 | MG1M, |
| 64 | 9 | w v | bit[8:0] –256/128 ... 255/128 | –44 | MG2M |
| 5C | 9 | w v | main matrix coefficient B–Y = MB1M×C _B + MB2M×C _R bit[8:0] –256/128 ... 255/128 | 113 | MB1M, |
| 54 | 9 | w v | bit[8:0] –256/128 ... 255/128 | 0 | MB2M |
| 78 | 9 | w v | side matrix coefficient R–Y = MR1S×C _B + MR2S×C _R bit[8:0] –256/128 ... 255/128 | 0 | MR1S, |
| 70 | 9 | w v | bit[8:0] –256/128 ... 255/128 | 73 | MR2S |
| 68 | 9 | w v | side matrix coefficient G–Y = MG1S×C _B + MG2S×C _R bit[8:0] –256/128 ... 255/128 | –19 | MG1S, |
| 60 | 9 | w v | bit[8:0] –256/128 ... 255/128 | –37 | MG2S |
| 58 | 9 | w v | side matrix coefficient B–Y = MB1S×C _B + MB2S×C _R bit[8:0] –256/128 ... 255/128 | 97 | MB1S, |
| 50 | 9 | w v | bit[8:0] –256/128 ... 255/128 | 0 | MB2S |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|---|---------------|-----------------------------|
| Picture Frame Generator | | | | | |
| 47 | 9 | w v | bit[7:0] reserved, set to zero bit[8] 1 enable picture frame generator | 0 | PFGEN |
| 11 | 16 | w h | picture frame color 12 bit wide, bit[3:0] 0..15 blue amplitude bit[7:4] 0..15 green amplitude bit[11:8] 0..15 red amplitude | 0 0 0 | PFC PFCB PFCG PFCR |
| 4C | 9 | w v | picture frame insertion contrast for R (ampl. range: 0 to 255) bit[3:0] reserved, set to zero bit[7:4] 0..13 R amplitude = PFCR × (PFRCT + 4) 14,15 invalid | 8 | PFRCT |
| 48 | 9 | w v | picture frame insertion contrast for G (ampl. range: 0 to 255) bit[3:0] reserved, set to zero bit[7:4] 0..13 G amplitude = PFCG × (PFGCT + 4) 14,15 invalid | 8 | PFGCT |
| 44 | 9 | w v | picture frame insertion contrast for B (ampl. range: 0 to 255) bit[3:0] reserved, set to zero bit[7:4] 0..13 B amplitude = PFCB × (PFBCT + 4) 14,15 invalid | 8 | PFBCT |
| 4F | 9 | w v | bit[8:0] horizontal picture frame begin code 0 = picture frame generator horizontally disabled code 1FF = full frame | 0 | PFGHB |
| 53 | 9 | w v | bit[8:0] horizontal picture frame end | 0 | PFGHE |
| 63 | 9 | w v | bit[8:0] vertical picture frame begin code 0 = picture frame generator vertically disabled | 270 | PFGVB |
| 6F | 9 | w v | bit[8:0] vertical picture frame end | 56 | PFGVE |
| Priority Decoder | | | | | |
| 75 | 9 | w v | bit[7] 0/1 select main/side setting for contrast,brightness,matrix | 0 | SIDE |
| 79 | 9 | w v | bit[7] 0/1 disable/enable peaking transient suppression when signal is switched to the picture frame | 0 | PKTRNS |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|--|---------------|------------------------|
| Scan Velocity Modulation | | | | | |
| 5A | 9 | w v | video mode coefficients bit[5:0] gain1 bit[8:6] differentiator delay 1 (0= filter off, 1...6= delay) | 60 4 | SVM1 SVG1 SVD1 |
| 52 | 9 | w v | limiter bit[6:0] limit value bit[8:5] not used, set to "0" | 100 0 | SVM3 SVLIM |
| 4E | 9 | w v | delay and coring bit[3:0] adjustable delay, in 1/2 display clock steps, bit[7:4] coring value bit[8] not used, set to "0" | 7 0 | SVM4 SVDEL SVCOR |
| Display Controls | | | | | |
| 4A | 9 | w v | cutoff Red | 0 | CR |
| 46 | 9 | w v | cutoff Green | 0 | CG |
| 42 | 9 | w v | cutoff Blue | 0 | CB |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|---------------------------------------|----------------|------|---|---------------|---|
| Tube- and Picture-Measurements | | | | | |
| 7B | 9 | w v | picture measurement start line bit[8:0] (TML+9)..511 first line of picture measurement | 23 | PMST |
| 6B | 9 | w v | picture measurement stop line bit[8:0] (PMST+1)..511 last line of picture measurement | 308 | PMSO |
| 7F | 9 | w v | tube measurement line bit[8:0] 0..511 start line for tube measurement | 15 | TML |
| 25 | 8 | w/r | tube and picture measurement control bit[0] 0/1 disable/enable tube measurement bit[1] 0/1 80/40 kHz bandwidth for picture measurement bit[2] 0/1 disable/enable picture measurement (writing a '1' starts one measurement cycle) bit[3] 0/1 large/small picture measurement window, will be disabled from bit[3] in address h'32 bit[4] 0/1 measure / offset check for adc bit[7:5] reserved | 0 | PMC TMEN PMBW PMEN PMWIN OFSEN |
| 13 | 16 | w/r | white drive measurement control bit[9:0] 0..1023 RGB values for white drive beam current measurement bit[10] reserved bit[11] 0/1 RGB values for white drive beam current measurement disabled/enabled | 512 0 | WDM WDRV EWDM |
| 18 19 1A 1D 1C 1B | 8 | r | measurement result registers minimum in active picture maximum in active picture white drive cutoff/leakage red cutoff/leakage green cutoff/leakage blue, read pulse starts tube measurement | – | MRMIN MRMAX MRWDR MRCR MRCG MRCB |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|---|----------------|------|---|---------------|-------|
| 1E | 8 | r | measurement adc status and fast blank input status measurement status register bit[0] 0/1 tube measurement active / complete bit[2:1] white drive measurement cycle 00 red 01 green 10 blue 11 reserved bit[3] 0/1 picture measurement active / complete bit[4] 0/1 fast blank input low / high (static) bit[5] 1 fast blank input negative transition since last read (bit reset at read) bit[7:6] reserved | – | PMS |
| Vertical Timing | | | | | |
| 67 | 9 | w v | vertical blanking start bit[8:0] 0..511 first line of vertical blanking | 305 | VBST |
| 77 | 9 | w v | vertical blanking stop bit[8:0] 0..511 last line of vertical blanking | 25 | VBSO |
| 5F | 9 | w v | free running field period bit[8:0] period = (value+4) lines | 309 | VPER |
| Horizontal Deflection and Timing | | | | | |
| 76 | 9 | w v | linear term of angle & bow correction bit[8:0] –256..+255 ± 500 ns | 0 | ANGLE |
| 7A | 9 | w v | quadratic term of angle & bow correction bit[8:0] –256..+255 ± 500 ns | 0 | BOW |
| 6E | 9 | w v | adjustable delay of PLL2, clamping, and blanking (relative to front sync) bit[8:0] –256..+255 ± 8 μs | –141 | POFS2 |
| 72 | 9 | w v | adjustable delay of horizontal drive & flyback (relative to PLL2) bit[8:0] –256..+255 ± 8 μs | 0 | POFS3 |
| 7E | 9 | w v | adjustable delay of main sync (relative to PLL2) adjust horizontal position for digital picture bit[8:0] 20 steps=1 μs | 120 | HPOS |
| 5B | 9 | w v | start of horizontal blanking bit[8:0] 0..511 | 1 | HBST |
| 57 | 9 | w v | end of horizontal blanking bit[8:0] 0..511 | 48 | HBSO |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|--|--|--|
| 62 | 9 | w v | PLL2/3 filter coefficients, 1of5 bit code (n+ set bit number) bit[5:0] proportional coefficient PLL3, 2^{-n-1} | 2 | PKP3 |
| 66 | 9 | w v | bit[5:0] proportional coefficient PLL2, 2^{-n-1} | 1 | PKP2 |
| 6A | 9 | w v | bit[5:0] integral coefficient PLL2, 2^{-n-5} | 2 | PKI2 |
| 15 | 16 | w/r | horizontal drive and vertical signal control register bit[5:0] 0..63 horizontal drive pulse duration in μ s (internally limited to 4..61) bit[6] 0/1 disable/enable horizontal PLL2 and PLL3 bit[7] 0/1 1: disable horizontal drive pulse during flyback bit[8] 0/1 reserved, set to '0' bit[9] 0/1 enable/disable ultra black blanking bit[10] 0/1 0: all outputs blanked 1: normal mode bit[11] 0/1 enable/disable clamping for analog RGB input bit[12] 0/1 disable/enable vertical free running mode (FIELD is set to field2, no interlace) bit[13] 0/1 enable/disable vertical protection bit[14] reserved (set to 0) bit[15] 0/1 disable/enable phase shift of display clock | 32 0 0 0 0 1 0 0 0 0 1 | HVC HDRV EHPLL EFLB DUBL EBL DCRGB SELFT DVPR DISKA |
| 9D | 8 | w/r | sync output control bit[0] invert INTLC bit[1] disable INTLC (tristateINTLC output) bit[2] invert VS bit[3] disable VS bit[4] disable CSY bit[5] force INTLC to polarity defined in 'INTLCINV' | 0 | SYCTRL |
| 9E | 8 | w/r | delay of CSY output (relative to PLL2) bit[7:0] $-128..127 \pm 8 \mu$ s | 0 | CSYDEL |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|---|---------------|--|
| Analog RGB Insertion | | | | | |
| 4B | 9 | w v | bit[7] 0/1 disable/enable analog fast blank input for RGB inserion | 0 | ERGB |
| 4B | 9 | w v | bit[0] 0 Picture frame overOSD 1 OSD over picture frame | 0 | OSDPRI0 |
| 32 | 8 | w/r | fast blank interface mode bit[0] 0 internal fast blank 1 from FBLIN1 pin 1 force internal fast blank 1 signal to high bit[1] 0/1 internal fast blank active high/low bit[2] 0/1 disable/enable clamping reference for RGB outputs bit[3] 1 full line MADC measurement window, disables bit [3] in address 25 bit[4] 0/1 horizontal flyback input active high/low bit[6:5] reserved (set to 0) bit[7] 0 internal fast blank 1 from FBLIN1 pin 1 force internal fast blank 1 signal to low | 0 | FBMOD FBFOH1 FBPOL CLMPR FLMW FLPOL FBFOL1 |
| 31 | 8 | w/r | fast blank interface mode 2 bit[0] 0 internal fast blank 2 from FBLIN2 pin 1 force internal fast blank 2 signal to high bit[1] 0 internal fast blank 2 from FBLIN2 pin 1 force internal fast blank 2signal to low bit[2] fast blank input priority 0 FBLIN1>FBLIN2 1 FBLIN2>FBLIN1 bit[3] fast blank monitor input select 0 monitor connected to FBLIN1 pin 1 monitor connected to FBLIN2 pin bit[4] half contrast switch enable 0/1 HCS disable/enable bit[5] 0 half contrast from HCS pin 1 force half contrast signal to high bit[6] 0/1 half contrast active high/low at HCS pin bit[7] reserved (set to 0) | 0 | FBMOD2 FBFOH2 FBFOL2 FBPRIO FBMON HCSEN HCSFOH HCSPOL |

Table 2–5: I²C control and status registers of the video backend
(Registers are set to '0' at reset, default values are recommendations)

| I ² C Sub address (hex) | Number of bits | Mode | Function | Default (hex) | Name |
|------------------------------------|----------------|------|---|---------------|-------------------------------|
| 10 | 8 | w/r | Sync Output bit[5:0] reserved (set to 0) bit[7:6] function of CSY pin 00 composite sync signal output 01 25 Hz output (field1/field2 signal) 10 horizontal sync signal output 11 1 MHz horizontal drive clock | 0 | CSYM |
| Ports | | | | | |
| 34 | 16 | w/r | IO Port bit[6:0] data to/from PORT[6:0] bit[7] reserved (set to 0) bit[14:8] port direction 0 switch PORT[bit–8] to input 1 switch PORT[bit–8] to output bit[15] reserved (set to 0) | 0 | IOPORT IODATA IODIR |
| Hardware ID | | | | | |
| 9F | 16 | r | Hardware version number bit[7:0] hardware id (A3 = 13, B1 = 21 a.s.o.) bit[15:8] product code VDP 31xx Y (e.g. 32 for VDP 3132 Y) | read only | HWID |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|----------------------|---|---------------|--|
| 148 | <p>Enable automatic standard recognition (ASR)</p> <p>bit[0] 0/1 PAL B,G,H,I (50 Hz) 4.433618</p> <p>bit[1] 0/1 NTSC M (60 Hz) 3.579545</p> <p>bit[2] 0/1 SECAM (50 Hz) 4.286</p> <p>bit[3] 0/1 NTSC44 (60 Hz) 4.433618</p> <p>bit[4] 0/1 PAL M (60 Hz) 3.575611</p> <p>bit[5] 0/1 PAL N (50 Hz) 3.582056</p> <p>bit[6] 0/1 PAL 60 (60 Hz) 4.433618</p> <p>bit[10:7] reserved set to 0</p> <p>bit[11] 1 reset status information 'switch' in asr_status (cleared automatically)</p> <p>0: disable recognition; 1: enable recognition</p> <p>Note: For correct operation don't change FP reg. 20h and 21h, while ASR is enabled!</p> | 0 | ASR_ENA |
| 14E | <p>Status of automatic standard recognition</p> <p>bit[0] 1 error of the vertical standard (neither 50 nor 60 Hz)</p> <p>bit[1] 1 detected standard is disabled</p> <p>bit[2] 1 search active</p> <p>bit[3] 1 search terminated, but failed</p> <p>bit[4] 1 no color found</p> <p>bit[5] 1 standard has been switched (since last reset of this flag with bit[11] of asr_enable)</p> <p>bit[4:0]</p> <p>00000 all ok</p> <p>00001 search not started, because vwin error detected (no input or SECAM L)</p> <p>00010 search not started, because detected vert. standard not enabled</p> <p>0x1x0 search started and still active</p> <p>01x00 search failed (found standard not correct)</p> <p>01x10 search failed, (detected color standard not enabled)</p> <p>1000 no color found (monochrome input or switch betw. CVBS/SVHS necessary)</p> | 0 | ASR_STATUS VWINERR DISABLED BUSY FAILED NOCOLOR SWITCH |
| 22 | <p>picture start position, this register sets the start point of active video, this can be used e.g. for panning. The setting is updated when 'sdt' register is updated.</p> | 0 | SFIF |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|----------------------|---|---------------------|--|
| 23 | luma/chroma delay adjust. The setting is updated when 'sdt' register is updated. bit[5:0] reserved, set to zero bit[11:6] luma delay in clocks, allowed range is +1...–7 | 0 | LDLY |
| 21 | Input select: writing to this register will also initialize the standard bit[1:0] luma selector 00 VIN1 01 VIN2 10 VIN3 11 VIN4 bit[2] chroma selector 0 CIN1 1 CIN2 bit[4:3] IF compensation 00 off 01 6 dB/Okt 10 12 dB/Okt 11 10 dB/MHz only for SECAM bit[6:5] chroma bandwidth selector 00 narrow 01 normal 10 broad 11 wide bit[7] 0/1 adaptive/fixed SECAM notch filter bit[8] 0/1 enable luma lowpass filter bit[10:9] hpll speed 00 no change 01 terrestrial 10 vcr 11 mixed bit[11] status bit, write 0, this bit is set to 1 to indicate operation complete. | 00 0 00 01 | INSEL VIS CIS IFC CBW FNTCH LOWP HPLLMD |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|----------------------|---|---------------|--|
| 2F | <p>YC_RC_B mode control register</p> <p>bit[6:0] reserved (set to 0)</p> <p>bit[7] 1 ADC over-/underflow (has to be reset after read if used)</p> <p>bit[8] 0 disable YC_RC_B 1 enable YC_RC_B</p> <p>bit[9] ADC range 0 nominal input amplitude (±350 mV) 1 extended input amplitude (±500 mV)</p> <p>bit[11:10] reserved (set to 0)</p> <p>Note: Activate the YC_RC_B mode by</p> <ul style="list-style-type: none"> - enabling YC_RC_B - selecting simple PAL or NTSC M, svhs=1, comb=0 in the std register - setting cbw=2 in the insel register | 0 | YCRCB |
| Comb Filter | | | |
| 27 | <p>comb filter control register</p> <p>bit[0] 0 comb coefficients are calculated for luma/ chroma 1 comb coefficients for luma are used for luma and chroma</p> <p>bit[1] 0 luma comb strength depends on signal amplitude 1 luma comb strength is independent of amplitude</p> <p>bit[2] 0 max comb booster 1 reduced comb booster</p> <p>bit[4:3] 0..3 comb strength for chroma signal</p> <p>bit[6:5] 0..3 comb strength for luma signal</p> <p>bit[11:7] 0..31 overall limitation of the calculated comb coefficients 0 no limitation 31 max limitation (1/2)</p> | 0 | <p>CMB_UC</p> <p>CC</p> <p>DAA</p> <p>KB</p> <p>KC</p> <p>KY</p> <p>CLIM</p> |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|-------------------------|---|---------------|----------------------|
| Color Processing | | | |
| 30 | Saturation control bit[11:0] 0...4094 (2070 corresponds to 100% saturation) 4095 disabled (test mode only) | 2070 | ACC_SAT |
| 17A | bit[10:0] 0...2047 CR-attenuation bit[11] 0/1 disable/enable CR-attenuation | 1591 0 | CR_ATT CR_ATT_ENA |
| 39 | bit[10:0] 0...2047 amplitude killer level (0: killer disabled) bit[11] 0/1 disable/enable chroma ADC | 25 0 | KILVL |
| 3A | amplitude killer hysteresis | 5 | KILHY |
| DC | NTSC tint angle, $\pm 512 = \pm \pi/4$ | 0 | TINT |
| DVCO | | | |
| F8 | crystal oscillator center frequency adjust, –2048...2047 | –720 | DVCO |
| F9 | crystal oscillator center frequency adjustment value for line lock mode, true adjust value is DVCO - ADJUST. For factory crystal alignment, using standard video signal: set DVCO = 0, set lock mode, read crystal offset from ADJUST register and use negative value for initial center frequency adjustment via DVCO. | read only | ADJUST |
| F7 | crystal oscillator line-locked mode, lock command/status write: 100 enable lock 0 disable lock read: 0 unlocked >2047 locked | 0 | XLCK |
| B5 | crystal oscillator line-locked mode, autolock feature. If autolock is enabled, crystal oscillator locking is started automatically. bit[11:0] threshold; 0: autolock off | 400 | AUTOLOCK |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|---------------------------|---|---------------|-----------------------------|
| FP Status Register | | | |
| 12 | general purpose control bits bit[2:0] reserved, do not change bit[3] vertical standard force bit[8:4] reserved, do not change bit[9] disable flywheel interlace bit[11:10] reserved, do not change to enable vertical free run mode set vfrc to 1 and dflw to 0 | 0 1 | GPC VFRC DFLW |
| 13 | standard recognition status (see also: 'automatic standard recognition') bit[0] 1 vertical lock bit[1] 1 horizontally locked bit[2] no signal detected bit[3] 1 color amplitude killer active bit[4] 1 disable amplitude killer bit[5] 1 color ident killer active bit[6] 1 disable ident killer bit[7] 1 interlace detected bit[8] 1 no vertical sync detection bit[9] 1 spurious vertical sync detection bit[11:10] reserved | – | ASR |
| 14 | input noise level | read only | NOISE |
| CB | number of lines per field, P/S: 312, N: 262 | read only | NLPF |
| 15 | vertical field counter, incremented per field | | VCNT |
| 74 | measured sync amplitude value, nominal: 768 (PAL), 732 (NTSC) | read only | SAMPL |
| 36 | measured burst amplitude | read only | BAMPL |
| F0 | firmware version number bit[7:0] internal revision number bit[11:8] firmware release | read only | SW_VERSION |
| 170 | status of macrovision detection bit[0] AGC pulse detected bit[1] pseudo sync detected | read only | MCV_STATUS |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|--------------------------------|--|---------------|----------------------------|
| 171 | bit[11:0] first line of macrovision detection window (relative to vsync) | 6 | MCV_START |
| 172 | bit[11:0] last line of macrovision detection window (relative to vsync) | 15 | MCV_STOP |
| Scaler Control Register | | | |
| 40 | <p>scaler mode register</p> <p>bit[1:0] scaler mode</p> <p>0 linear scaling mode</p> <p>1 nonlinear scaling mode, 'panorama'</p> <p>2 nonlinear scaling mode, 'waterglass'</p> <p>3 reserved</p> <p>bit[10:2] reserved, set to 0</p> <p>bit[11] scaler update</p> <p>0 start scaler update command, when the registers are updated the bit is set to 1</p> | 0 | SCMODE MODE SCUP |
| 41 | <p>luma offset register</p> <p>bit[6:0] luma offset 0..127</p> <p>ITU-R output format: 57</p> <p>CVBS output format: 4</p> <p>this register is updated when the scaler mode register is written</p> | 57 | YOFFS |
| 42 | <p>active video length for 1-h FIFO</p> <p>bit[11:0] length in pixels</p> <p>this register is updated when the scaler mode register is written</p> | 1080 | FFLIM |
| 43 | <p>scaler1 coefficient, this scaler is compressing the signal.</p> <p>For compression by a factor c the value $c*1024$ is required.</p> <p>bit[11:0] allowed values from 1024..4095</p> <p>this register is updated when the scaler mode register is written</p> | 1024 | SCINC1 |
| 44 | <p>scaler2 coefficient, this scaler is expanding the signal.</p> <p>For expansion by a factor c the value $1/c*1024$ is required.</p> <p>bit[11:0] allowed values from 256..1024</p> <p>this register is updated when the scaler mode register is written</p> | 1024 | SCINC2 |
| 45 | <p>scaler1/2 nonlinear scaling coefficient</p> <p>this register is updated when the scaler mode register is written</p> | 0 | SCINC |
| 47 - 4B | <p>scaler1 window controls, see table</p> <p>5 12-bit registers for control of the nonlinear scaling</p> <p>this register is updated when the scaler mode register is written</p> | 0 | SCW1_0 - 4 |

Table 2–6: Control Registers of the Fast Processor for control of the video frontend functions
–default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|----------------------|---|---------------|------------|
| 4C - 50 | scaler2 window controls see table 5 12-bit registers for control of the nonlinear scaling this register is updated when the scaler mode register is written | 0 | SCW2_0 - 4 |

2.14.2.1. Scaler Adjustment

In case of linear scaling, most of the scaler registers need not be set. Only the scaler mode, active video length, and the fixed scaler increments (scinc1/scinc2) must be written.

The adjustment of the scaler for nonlinear scaling modes should use the parameters given in Table 2–7.

Table 2–7: Set-up values for nonlinear scaler modes

| Register | Scaler Modes | | | |
|----------|-------------------------|------|-----------------------|------|
| | 'waterglass' border 35% | | 'panorama' border 30% | |
| | center compression | | | |
| | 3/4 | 5/6 | 4/3 | 6/5 |
| scinc1 | 1643 | 1427 | 1024 | 1024 |
| scinc2 | 1024 | 1024 | 376 | 611 |
| scinc | 90 | 56 | 85 | 56 |
| fflim | 945 | 985 | 921 | 983 |
| scw1 - 0 | 110 | 115 | 83 | 94 |
| scw1 - 1 | 156 | 166 | 147 | 153 |
| scw1 - 2 | 317 | 327 | 314 | 339 |
| scw1 - 3 | 363 | 378 | 378 | 398 |
| scw1 - 4 | 473 | 493 | 461 | 492 |
| scw2 - 0 | 110 | 115 | 122 | 118 |
| scw2 - 1 | 156 | 166 | 186 | 177 |
| scw2 - 2 | 384 | 374 | 354 | 363 |
| scw2 - 3 | 430 | 425 | 418 | 422 |
| scw2 - 4 | 540 | 540 | 540 | 540 |

Table 2–8: Control Registers of the Fast Processor for control of the video backend functions—default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|---|--|---------------|-------------------|
| FP Display Control Register | | | |
| 130 | White Drive Red (0...1023) | 700 | WDR ¹⁾ |
| 131 | White Drive Green (0...1023) | 700 | WDG ¹⁾ |
| 132 | White Drive Blue (0...1023) | 700 | WDB ¹⁾ |
| 139 | Internal Brightness, Picture (0...511), the center value is 256, the range allows for both increase and reduction of brightness. | 256 | IBR |
| 13C | Internal Brightness, Measurement (0...511), the center value is 256, the brightness for measurement can be set to measure at higher cutoff current. The measurement brightness is independent of the drive values. | 256 | IBRM |
| 13A | Analog Brightness for external RGB (0...511), the center value is 256, the range allows for both increase and reduction of brightness. | 256 | ABR |
| 13B | Analog Contrast for external RGB (0...511) | 350 | ACT |
| ¹⁾ The white drive values will become active only after writing the blue value WDB, latching of new values is indicated by setting the MSB of WDB. | | | |
| FP Display Control Register, BCL | | | |
| 144 | BCL threshold current, 0...2047 (max ADC output ~1152) | 1000 | BCLTHR |
| 142 | BCL time constant 0...15 → 13 ... 1700 ms | 15 | BCLTM |
| 143 | BCL loop gain. 0..15 | 0 | BCLG |
| 145 | BCL minimum contrast 0...1023 | 307 | BCLMIN |
| 105 | Test register for BCL/EHT comp. function, register value: 0 normal operation 1 stop ADC offset compensation x>1 use x in place of input from Measurement ADC | 0 | BCLTST |
| 60 | Current BCL reduction (0...1023; read only) | 1023 | BCLREDUC |
| FP Display Control Register, Deflection | | | |
| 103 | interlace offset, -2048..2047 This value is added to the SAWTOOTH output during one field. | 0 | INTLC |
| 102 | discharge sample count for deflection retrace, SAWTOOTH DAC output impedance is reduced for DSCC lines after vertical retrace. | 7 | DSCC |
| 11F | vertical discharge value, SAWTOOTH output value during discharge operation, typically same as A0 init value for sawtooth. | -1365 | DSCV |
| 10B | EHT compensation vertical gain coefficient, 0...511 | 0 | EHTV |

Table 2–8: Control Registers of the Fast Processor for control of the video backend functions—default values are initialized at reset

| FP Sub-address (hex) | Function | Default (hex) | Name |
|--|---|---------------|-------|
| 10A | EHT compensation time constant, 0...15 → 3.2..410 ms | 15 | EHTTM |
| 10F | EHT compensation east/west gain coefficient, –512...511 | 0 | EHTEW |
| FP Display Control Register, Vertical Sawtooth | | | |
| 110 | DC offset of SAWTOOTH output This offset is independent of EHT compensation. | 0 | OFS |
| 11B | accu0 init value | –1365 | A0 |
| 11C | accu1 init value | 900 | A1 |
| 11D | accu2 init value | 0 | A2 |
| 11E | accu3 init value | 0 | A3 |
| FP Display Control Register, East-West Parabola | | | |
| 12B | accu0 init value | –1121 | A0 |
| 12C | accu1 init value | 219 | A1 |
| 12D | accu2 init value | 479 | A2 |
| 12E | accu3 init value | –1416 | A3 |
| 12F | accu4 init value | 1052 | A4 |

2.14.2.2. Calculation of Vertical and East-West Deflection Coefficients

In Table 2–9 and Table 2–10 the formula for the calculation of the deflection initialization parameters from the polynomial coefficients a,b,c,d,e is given for the vertical and East-West deflection. Let the polynomial be

$$P : a + b(x - 0.5) + c(x - 0.5)^2 + d(x - 0.5)^3 + e(x - 0.5)^4$$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for East-West deflection are 12-bit values. The coefficients that should be used to calculate the initialization values for different field frequencies are given below, the values must be scaled by 128, i.e. the value for a0 of the 50 Hz vertical deflection is:

$$a0 = (a \cdot 128 - b \cdot 1365.3 + c \cdot 682.7 - d \cdot 682.7) / 128$$

Table 2–9: Calculation of Initialization values for Vertical Sawtooth

| Vertical Deflection 50 Hz | | | | |
|---------------------------|-----|---------|---------|---------|
| | a | b | c | d |
| a0 | 128 | -1365.3 | 682.7 | -682.7 |
| a1 | | 899.6 | -904.3 | 1363.4 |
| a2 | | | 296.4 | -898.4 |
| a3 | | | | 585.9 |
| Vertical Deflection 60 Hz | | | | |
| | a | b | c | d |
| a0 | 128 | -1365.3 | 682.7 | -682.7 |
| a1 | | 1083.5 | -1090.2 | 1645.5 |
| a2 | | | 429.9 | -1305.8 |
| a3 | | | | 1023.5 |

Table 2–10: Calculation of Initialization values for East-West Parabola

| East-West Deflection 50 Hz | | | | | |
|----------------------------|-----|--------|---------|--------|---------|
| | a | b | c | d | e |
| a0 | 128 | -341.3 | 1365.3 | -85.3 | 341.3 |
| a1 | | 111.9 | -899.6 | 84.8 | -454.5 |
| a2 | | | 586.8 | -111.1 | 898.3 |
| a3 | | | | 72.1 | -1171.7 |
| a4 | | | | | 756.5 |
| East-West Deflection 60 Hz | | | | | |
| | a | b | c | d | e |
| a0 | 128 | -341.3 | 1365.3 | -85.3 | 341.3 |
| a1 | | 134.6 | -1083.5 | 102.2 | -548.4 |
| a2 | | | 849.3 | -161.2 | 1305.5 |
| a3 | | | | 125.6 | -2046.6 |
| a4 | | | | | 1584.8 |

3. Specifications

3.1. Outline Dimensions

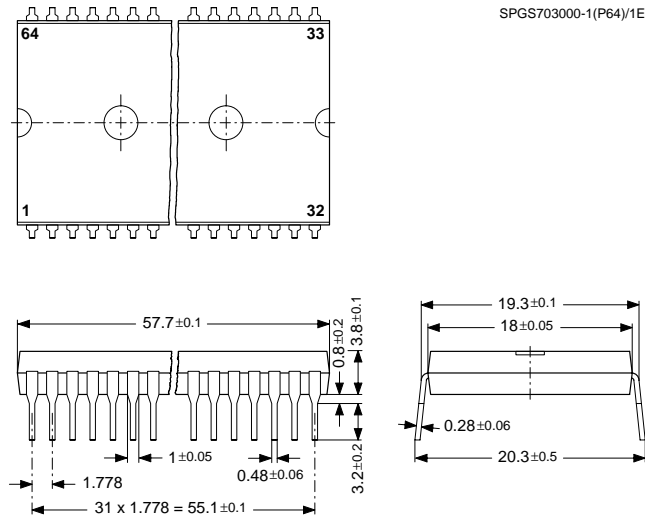


Fig. 3-1:
 64-Pin Plastic Shrink Dual-Inline Package
(PSDIP64)
 Weight approximately 9.0 g
 Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected
 LV = if not used, leave vacant
 X = obligatory; connect as described in circuit diagram

IN = Input
 OUT = Output
 SUPPLY = Supply Pin

| Pin No. PSDIP 64-pin | Pin Name | Type | Connection (If not used) | Short Description |
|----------------------------|----------|--------|-----------------------------|---|
| 1 | TEST | IN | GNDD | Test Input |
| 2 | RESQ | IN | X | Reset Input |
| 3 | SCL | IN/OUT | X | I ² C Bus Clock |
| 4 | SDA | IN/OUT | X | I ² C Bus Data |
| 5 | GNDD | SUPPLY | X | Digital Ground |
| 6 | HCS | IN | LV | Half Contrast Switch Input |
| 7 | FSY | OUT | LV | Front Sync Output |
| 8 | CSY | OUT | LV | Composite Sync Output |
| 9 | VS | OUT | LV | Vertical Sync Output (= VS Bit of MSY for TPU) |
| 10 | INTLC | OUT | LV | Interlace Control Output |
| 11 | VPROT | IN | GNDAB | Vertical Protection Input |

| Pin No. PSDIP 64-pin | Pin Name | Type | Connection (If not used) | Short Description |
|----------------------------|----------|--------|-----------------------------|--|
| 12 | SAFETY | IN | GNDAB | Safety Input |
| 13 | HFLB | IN | HOUT | Horizontal Flyback Input |
| 14 | GNDD | SUPPLY | X | Digital Ground |
| 15 | VSUPD | SUPPLY | X | Digital Supply Voltage (3.3 V) |
| 16 | GNDD | SUPPLY | X | Digital Ground |
| 17 | VSUPD | SUPPLY | LV | Digital Supply Voltage (3.3 V) |
| 18 | P0 | IN/OUT | LV | Port 1, Bit 0 |
| 19 | P1 | IN/OUT | LV | Port 1, Bit 1 |
| 20 | P2 | IN/OUT | GNDD | Port 1, Bit 2 |
| 21 | P3 | IN/OUT | GNDD | Port 1, Bit 3 |
| 22 | P4 | IN/OUT | GNDD | Port 1, Bit 4 |
| 23 | P5 | IN/OUT | GNDD | Port 1, Bit 5 |
| 24 | P6 | IN/OUT | GNDD | Port 1, Bit 6 |
| 25 | GNDD | SUPPLY | X | Digital Ground |
| 26 | RSW2 | OUT | GNDAB | Range Switch 2 for Measurement ADC |
| 27 | RSW1 | OUT | GNDAB | Range Switch 1 for Measurement ADC |
| 28 | SENSE | IN | GNDAB | Sense ADC Input |
| 29 | GNDM | SUPPLY | X | Ground, MADC Input |
| 30 | VERTQ | OUT | LV | Inverted Vertical Sawtooth Output |
| 31 | VERT | OUT | LV | Vertical Sawtooth Output |
| 32 | E/W | OUT | LV | Vertical Parabola Output |
| 33 | XREF | IN | X | Reference Input for RGB DACs |
| 34 | SVMOUT | OUT | VSUPAB | Analog Scan Velocity Modulation Output |
| 35 | GNDAB | SUPPLY | X | Analog Ground Backend |
| 36 | VSUPAB | SUPPLY | X | Analog Supply Voltage (5.0 V) Backend |
| 37 | ROUT | OUT | VSUPAB | Analog Red Output |
| 38 | GOUT | OUT | VSUPAB | Analog Green Output |
| 39 | BOUT | OUT | VSUPAB | Analog Blue Output |
| 40 | VRD | IN | X | DAC Reference |
| 41 | RIN | IN | GNDAB | Analog Red Input |
| 42 | GIN | IN | GNDAB | Analog Green Input |

| Pin No. PSDIP 64-pin | Pin Name | Type | Connection (If not used) | Short Description |
|----------------------------|------------|--------|-----------------------------|--|
| 43 | BIN | IN | GNDAB | Analog Blue Input |
| 44 | FBLIN | IN | GNDAB | Fast Blank Input |
| 45 | RIN2 | IN | GNDAB | Analog Red Input2 |
| 46 | GIN2 | IN | GNDAB | Analog Green Input2 |
| 47 | BIN2 | IN | GNDAB | Analog Blue Input2 |
| 48 | FBLIN2 | IN | GNDAB | Fast Blank Input2 |
| 49 | CLK20 | OUT | LV | 20.25 MHz System Clock Output |
| 50 | HOUT | OUT | X | Horizontal Drive Output |
| 51 | XTAL 1 | IN | X | Analog Crystal Input |
| 52 | XTAL 2 | OUT | X | Analog Crystal Output |
| 53 | CIN 2/CRIN | IN | LV | Analog Chroma 2/Component C _R Input |
| 54 | CBIN | IN | LV | Component C _B Input |
| 55 | GNDAF | SUPPLY | X | Analog Ground Frontend |
| 56 | SGND | IN | GNDAF | Signal Ground for Analog Input |
| 57 | VRT | IN | X | Reference Voltage Top, Video ADC |
| 58 | VSUPAF | SUPPLY | X | Analog Supply Voltage (5.0 V) Frontend |
| 59 | VOUT | OUT | LV | Analog Video Output |
| 60 | CIN1 | IN | VRT | Analog Chroma 1 Input |
| 61 | VIN1 | IN | VRT | Analog Video 1 Input |
| 62 | VIN2 | IN | VRT | Analog Video 2 Input |
| 63 | VIN3 | IN | VRT | Analog Video 3 Input |
| 64 | VIN4 | IN | VRT | Analog Video 4 Input |

3.3. Pin Descriptions

Pin 1 – Test Input, **TEST** (Fig. 3–3)

This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 2 – Reset Input, **RESQ** (Fig. 3–4)

A low level on this pin resets the VDP31xxY.

Pin 3 – I²C Bus Clock, **SCL** (Fig. 3–4)

This pin connects to the I²C bus clock line.

Pin 4 – I²C Bus Data, **SDA** (Fig. 3–4)

This pin connects to the I²C bus data line.

Pin 5 – Ground (Digital Shield), **GNDD**

Pin 6 – Half Contrast Switch Input, **HCS** (Fig. 3–22)

Via this input pin the output level of the analog RGB output pins can be reduced by 6 dB.

Pin 7 – Front Sync Output, **FSY** (Fig. 3–21)

This pin supplies the front sync information

Pin 8 – Composite Sync Output, **CSY** (Fig. 3–21)

This output supplies a standard composite sync signal that is compatible to the analog RGB output signals.

Pin 9 – Vertical Sync Output, **VS** (Fig. 3–21)

This pin supplies the vertical sync information.

Pin 10 – Interlace Output, **INTLC** (Fig. 3–21)

This pin supplies the interlace information, with programmable polarity.

Pin 11 – Vertical Protection Input, **VPROT** (Fig. 3–14)

The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. During vertical blanking, a signal level of 2.5 V is sensed. If a negative edge cannot be detected, the RGB output signals are blanked.

Pin 12 – Safety Input, **SAFETY** (Fig. 3–14)

This is a three-level input. Low level means normal function. At the medium level RGB signals are blanked and at high level RGB signals are blanked and horizontal drive is shut off.

Pin 13 – Horizontal Flyback Input, **HFLB** (Fig. 3–14)

Via this pin the horizontal flyback pulse is supplied to the VDP 313xY.

Pin 14 – Ground (Digital Circuitry Front-end), **GNDD**

Pin 15, 17– Supply Voltage (Digital Circuitry), **VSUPD**

Pin 16 – Ground (Digital Circuitry Back-end), **GNDD**

Pin 18–24 – IO Port Expander, **PORT[6:0]** (Fig. 3–21, Fig. 3–22)

These pins provide an I²C programmable I/O port, which can be used to read and write slow external signals.

Pin 25 – Ground (Digital Shield), **GNDD**.

Pin 26, 27 – Range Switch for Measurement ADC, **RSW1, RSW2** (Fig. 3–18)

These pins are open drain pull-down outputs. RSW1 is switched off during cutoff and whitedrive measurement. RSW2 is switched off during cutoff measurement only.

Pin 28 – Measurement ADC Input, **SENSE** (Fig. 3–19)

This is the input of the analog digital converter for the picture and tube measurement.

Pin 29 – Ground (Measurement ADC Reference Input), **GNDM**

This is the ground reference for the measurement A/D converter.

Pin 30 – Vertical Sawtooth Output Q, **VERTQ** (Fig. 3–16)

This pin supplies the drive signal for the vertical output stage. The drive signal is generated with 15-bit precision by the Fast Processor in the front-end. The analog voltage is generated by a 4-bit current-DAC with external resistor and uses digital noise shaping.

Pin 31 – Vertical Sawtooth Output, **VERT** (Fig. 3–16)

This pin supplies the inverted signal of pin 30. Together with pin 30 it can be used to drive symmetrical deflection amplifiers.

Pin 32 – East–West Parabola Output, **EW** (Fig. 3–17)

This pin supplies the parabola signal for the East–West correction. The drive signal is generated with 15 bit precision by the Fast Processor in the front-end. The analog voltage is generated by a 4-bit current-DAC with external resistor and uses digital noise shaping.

Pin 33 – DAC Current Reference, **XREF** (Fig. 3–20)

External reference resistor for DAC output currents, typical 10 k Ω to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to analog ground as closely as possible to the pin without any capacitor.

Pin 34 – Scan Velocity Modulation Output, **SVMOUT** (Fig. 3–12)

This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50 % of the maximum output current.

Pin 35 – Ground (Analog Back-end), **GNDAB**

Pin 36 – Supply Voltage (Analog Back-end), **VSUPAB**

Pin 37, 38, 39 – Analog RGB Outputs, **ROUT**, **GOUT**, **BOUT** (Fig. 3–12)

This are the analog Red/Green/Blue outputs of the backend. The outputs sink a current of max. 8 mA.

Pin 40 – DAC Reference Decoupling, **VRD** (Fig. 3–20)

Via this pin the DAC reference voltage is decoupled by an external capacitance. The DAC output currents depend on this voltage, therefore a pull-down transistor can be used to shut off all beam currents. A decoupling capacitor of 3.3 μ F/100 nF is required.

Pin 41, 42, 43, 45, 46, 47 – Analog RGB Inputs, **RIN1/2**, **GIN1/2**, **BIN1/2** (Fig. 3–11)

These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can be switched to the analog RGB outputs with the fast blank signal. The analog backend provides separate brightness and contrast settings for the external analog RGB signals.

Pin 44, 48 – Fast Blank Inputs, **FBLIN1/2** (Fig. 3–15)

These pins are used to switch the RGB outputs to the external analog RGB inputs.

Pin 49 – Main Clock Output, **CLK20** (Fig. 3–6)

This is the 20.25 MHz main system clock, that is used by all circuits in a high-end VDP system. All external timing is derived from this clock.

Pin 50 – Horizontal Drive Output, **HOUT** (Fig. 3–13)

This open drain output supplies the the drive pulse for the horizontal output stage. The polarity and gating with the flyback pulse are selectable by software.

Pin 51, 52 – Crystal Input and Output, **XTAL1**, **XTAL2** (Fig. 3–5)

These pins are connected to an 20.25 MHz crystal oscillator is digitally tuned by integrated shunt capacitances. The Clk20 signal is derived from this oscillator.

Pin 53, 54, 60– Analog Chroma Inputs, **CIN1**, **CIN2/CRIN**, **CBIN** (Fig. 3–7, Fig. 3–8)

CIN1, CIN2 are the analog chroma inputs for S-VHS. A S-VHS chroma signal is converted using the chroma (Video2) AD converter. A resistive divider is used to BIAS the input signal to middle of converter range. The input signal must be AC coupled. Together with the CBIN pin CIN2 can alternatively be used as chroma component input for the analog YC_RC_B interface.

Pin 55 – Ground (Analog Front-end), **GNDAF**

Pin 56 – Ground (Analog Signal Input), **SGND** (Fig. 3–10)

This is the high quality ground reference for the video input signals.

Pin 57 – Reference Voltage Top, **VRT** (Fig. 3–10)

Via this pin, the reference voltage for the A/D converters is decoupled. The pin is connected with 10 μ F/47 nF to the Signal Ground Pin.

Pin 58 – Supply Voltage (Analog Front-end), **VSUPAF**

Pin 59 – Analog Video Output, **VOUT** (Fig. 3–9)

The analog video signal that is selected for the main (luma, cvbs) adc is output at this pin. An emitter follower is required at this pin.

Pin 61...64 – Analog Video Input 1–4, **VIN1–4** (Fig. 3–7)

These are the analog video inputs. A CVBS or S-VHS luma signal is converted using the luma (Video 1) AD converter. The input signal must be AC-coupled.

3.4. Pin Configuration

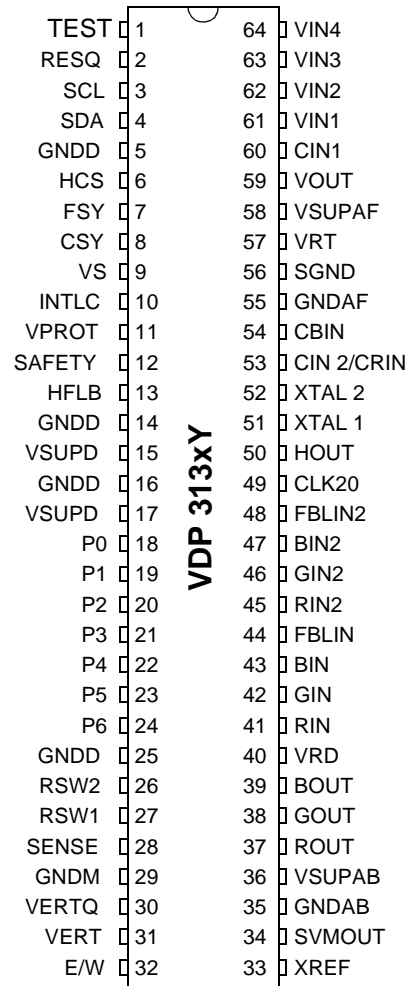


Fig. 3–2: 64-pin PSDIP package

3.5. Pin Circuits

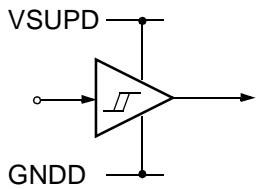


Fig. 3-3: Input pin TEST, RESQ

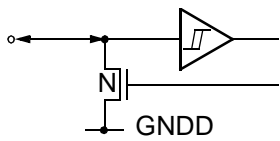


Fig. 3-4: Input/Output pins SDA, SCL

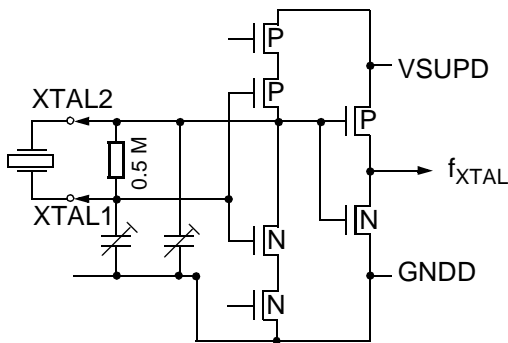


Fig. 3-5: Input/Output pins XTAL1, XTAL2

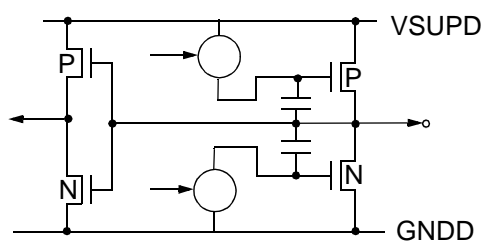


Fig. 3-6: Output pin CLK20

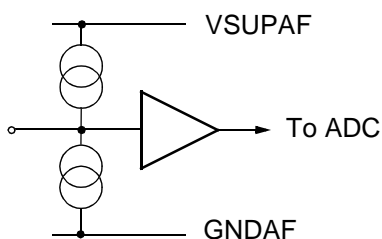


Fig. 3-7: Input pins VIN1-VIN4, CBIN, CRIN

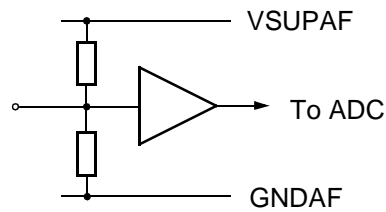


Fig. 3-8: Input pins CIN1, CIN2

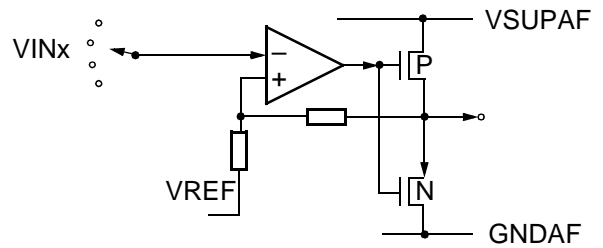


Fig. 3-9: Output pin VOUT

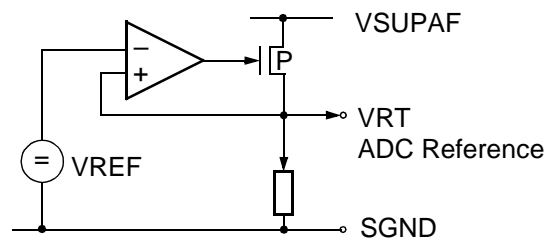


Fig. 3-10: Supply pins VRT, SGND

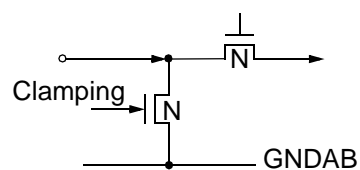


Fig. 3-11: Input pins RIN, GIN, BIN

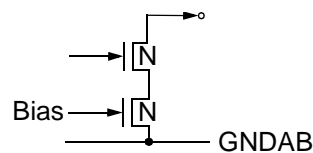


Fig. 3-12: Output pins ROUT, GOUT, BOUT, SVMOUT

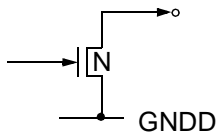


Fig. 3-13: Output pin HOUT

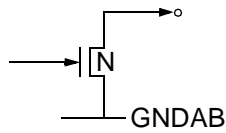


Fig. 3-18: Output pins RSW1, RSW2

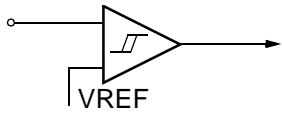


Fig. 3-14: Input pins SAFETY, HFLB, VPROT

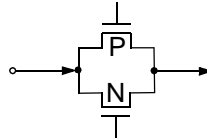


Fig. 3-19: Input pin SENSE

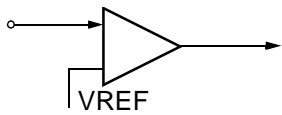


Fig. 3-15: Input pins FBLIN

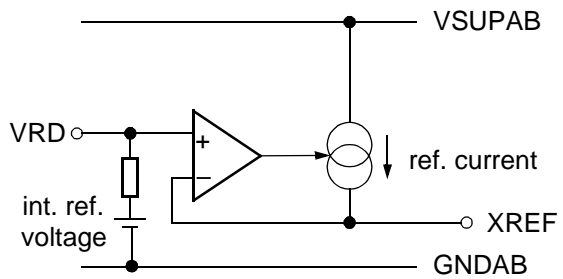


Fig. 3-20: Supply pins XREF, VRD

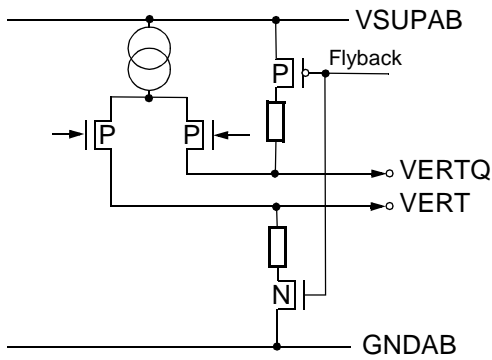


Fig. 3-16: Output pins VERT, VERTQ

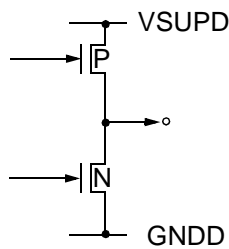


Fig. 3-21: Output pins FSY, VS, CSY, INTLC, PORT[6:0]

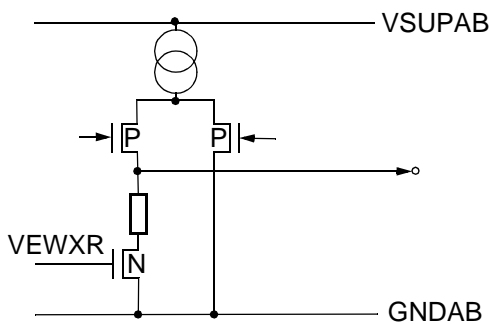


Fig. 3-17: Output pin EW

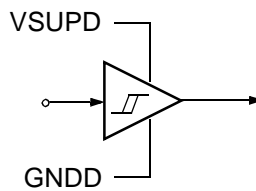


Fig. 3-22: Input pins HCS, PORT[6:0]

3.6. Electrical Characteristics

3.6.1. Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Min. | Max. | Unit |
|---|--|-------------|-------|----------------------|------|
| T_J | Junction Temperature | | 0 | 125 | °C |
| T_S | Storage Temperature | | -40 | 125 | °C |
| P_{TOT} | Total Power Dissipation | | - | 1400 | mW |
| V_{SUP_x} | Supply Voltage | V_{SUP_x} | -0.3 | 6 | V |
| V_I | Input Voltage, all Inputs | | -0.3 | $V_{SUP_x}+0.3^{1)}$ | V |
| V_O | Output Voltage, all Outputs | | -0.3 | $V_{SUP_x}+0.3^{1)}$ | V |
| V_{IO} | Input/Output Voltage, all Open Drain Outputs | | -0.3 | 6 | V |
| V_{ES} | Electrostatic Handling, HBM ²⁾ | | -2000 | +2000 | V |
| ¹⁾ Refer to Pin Circuits (chapter 3.5. on page 57) ²⁾ Human Body Model (HBM): R=1.5 kΩ, C=100 pF | | | | | |

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operat-

ing Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Operating Conditions

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|-------------|-------------------------------|----------------------------------|------|-------|------|------|
| T_A | Ambient Operating Temperature | | 0 | - | 65 | °C |
| f_{XTAL} | Clock Frequency | XTAL1/2 | - | 20.25 | - | MHz |
| V_{SUP_A} | Analog Supply Voltage | $V_{SUP_{AF}}$ $V_{SUP_{AB}}$ | 4.75 | 5.0 | 5.25 | V |
| V_{SUP_D} | Digital Supply Voltage | V_{SUP_D} | 3.15 | 3.3 | 3.45 | V |

3.6.2.1. Analog Input and Output Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|-------------------|--|-----------------------|------|------|------|-----------|
| Video | | | | | | |
| V_{VIN} | Video Input Level | VIN1-4, CIN1-2 | 0.5 | 1.0 | 3.5 | V_{PP} |
| V_{CIN} | Chroma Input Level | CRIN, CBIN | – | 700 | – | mV |
| C_{VIN} | Input Coupling Capacitor Video Inputs | VIN1-4 | – | 680 | – | nF |
| C_{CIN} | Input Coupling Capacitor Chroma Inputs | CIN1-2 | – | 1 | – | nF |
| C_{CCIN} | Input Coupling Capacitor Component Inputs | CRIN, CBIN | – | 220 | – | nF |
| RGB | | | | | | |
| R_{xref} | RGB-DAC Current defining Resistor | XREF | 9.5 | 10 | 10.5 | $k\Omega$ |
| C_{RGBIN} | RGB Input Coupling Capacitor | RIN GIN BIN | – | 15 | – | nF |
| Deflection | | | | | | |
| R_{load} | Deflection Load Resistance | EW, VERT, VERTQ | – | 6.8 | – | $k\Omega$ |
| C_{load} | Deflection Load Capacitance | | – | 68 | – | nF |

3.6.3. Recommended Crystal Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------------------|---|------|-----------|------|------|
| T _A | Operating Ambient Temperature | 0 | – | 65 | °C |
| f _P | Parallel Resonance Frequency with Load Capacitance C_L = 13 pF | – | 20.250000 | – | MHz |
| Δf _P /f _P | Accuracy of Adjustment | – | – | ±20 | ppm |
| Δf _P /f _P | Frequency Temperature Drift | – | – | ±30 | ppm |
| R _R | Series Resistance | – | – | 25 | Ω |
| C ₀ | Shunt Capacitance | 3 | – | 7 | pF |
| C ₁ | Motional Capacitance | 20 | – | 30 | fF |

Load Capacitance Recommendation

| | | | | | |
|-------------------|--|---|-----|---|----|
| C _{Lext} | External Load Capacitance ¹⁾ from pins to Ground (pin names: Xtal1 Xtal2) | – | 3.3 | – | pF |
|-------------------|--|---|-----|---|----|

DCO Characteristics ^{2,3)}

| | | | | | |
|------------------------|--|----|------|-----|----|
| C _{ICLoadmin} | Effective Load Capacitance @ min. DCO–Position, Code 0, package: 64PSDIP | 3 | 4.3 | 5.5 | pF |
| C _{ICLoadrng} | Effective Load Capacitance Range, DCO Codes from 0..255 | 11 | 12.7 | 15 | pF |

1) Remarks on defining the External Load Capacitance:

External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance of the PCBs to the required load capacitance C_L of the crystal. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match f_P MHz. Due to different layouts of customer PCBs the matching capacitor size should be determined in the application. The suggested value is a figure based on experience with various PCB layouts.

Tuning condition: Code DVCO Register = –720

2) Remarks on Pulling Range of DCO:

The pulling range of the DCO is a function of the used crystal and effective load capacitance of the IC (C_{ICLoad} + C_{LoadBoard}). The resulting frequency f_L with an effective load capacitance of C_{Leff} = C_{ICLoad} + C_{LoadBoard} is:

$$f_L = f_P \times \frac{1 + 0.5 \times [C_1 / (C_0 + C_{Leff})]}{1 + 0.5 \times [C_1 / (C_0 + C_L)]}$$

3) Remarks on DCO codes

The DCO hardware register has 8 bits, the fp control register uses a range of –2048...2047

3.6.4. Characteristics

If not otherwise designated under test conditions, all characteristics are specified for recommended operating conditions (see Section 3.6.2. on page 59).

3.6.4.1. General Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------|---------------------------------------|--------------|------|------|------|---------|---|
| P_{TOT} | Total Power Dissipation | | – | 900 | 1400 | mW | |
| I_{VSUPD} | Current Consumption Digital Circuitry | $VSUP_D$ | – | 118 | – | mA | |
| I_{VSUPAF} | Current Consumption Analog Frontend | $VSUP_{AF}$ | – | 35 | – | mA | |
| I_{VSUPAB} | Current Consumption Analog Backend | $VSUP_{AB}$ | – | 58 | – | mA | depends on contrast and brightness settings |
| I_L | Input and Output Leakage Current | All I/O Pins | –1 | – | 1 | μ A | |

3.6.4.2. I²C Bus Interface

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|------------------------------|----------|------|------|------------|---------|------------------------------|
| V_{IL} | Input Low Voltage | SDA, SCL | – | – | 0.3 | $VSUPD$ | |
| V_{IH} | Input High Voltage | | 0.6 | – | – | $VSUPD$ | |
| V_{OL} | Output Low Voltage | | – | – | 0.4 0.6 | V V | $I_I = 3$ mA $I_I = 6$ mA |
| V_{IH} | Input Capacitance | | – | – | 5 | pF | |
| t_F | Signal Fall Time | | – | – | 300 | ns | $C_L = 400$ pF |
| t_R | Signal Rise Time | | – | – | 300 | ns | $C_L = 400$ pF |
| f_{SCL} | Clock Frequency | SCL | 0 | – | 400 | kHz | |
| t_{LOW} | Low Period of SCL | | 1.3 | – | – | μ s | |
| t_{HIGH} | High Period of SCL | | 0.6 | – | – | μ s | |
| $t_{SU\ Data}$ | Data Set Up Time to SCL high | SDA | 100 | – | – | ns | |
| $t_{HD\ Data}$ | DATA Hold Time to SCL low | | 0 | – | 0.9 | μ s | |

3.6.4.3. Reset Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|----------|--------------------|----------|------|------|------|------|-----------------|
| V_{IL} | Input Low Voltage | RESQ | – | – | 0.8 | V | |
| V_{IH} | Input High Voltage | RESQ | 2 | – | – | V | |

3.6.4.4. Power-up Sequence

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|------------|--------------------------------|----------|------|------|---------|------|-----------------|
| t_{Vdel} | Ramp Up Difference of Supplies | | 0 | - | ± 1 | s | |
| t_{Vrmp} | Transition Time of Supplies | | - | - | 50 | ms | |

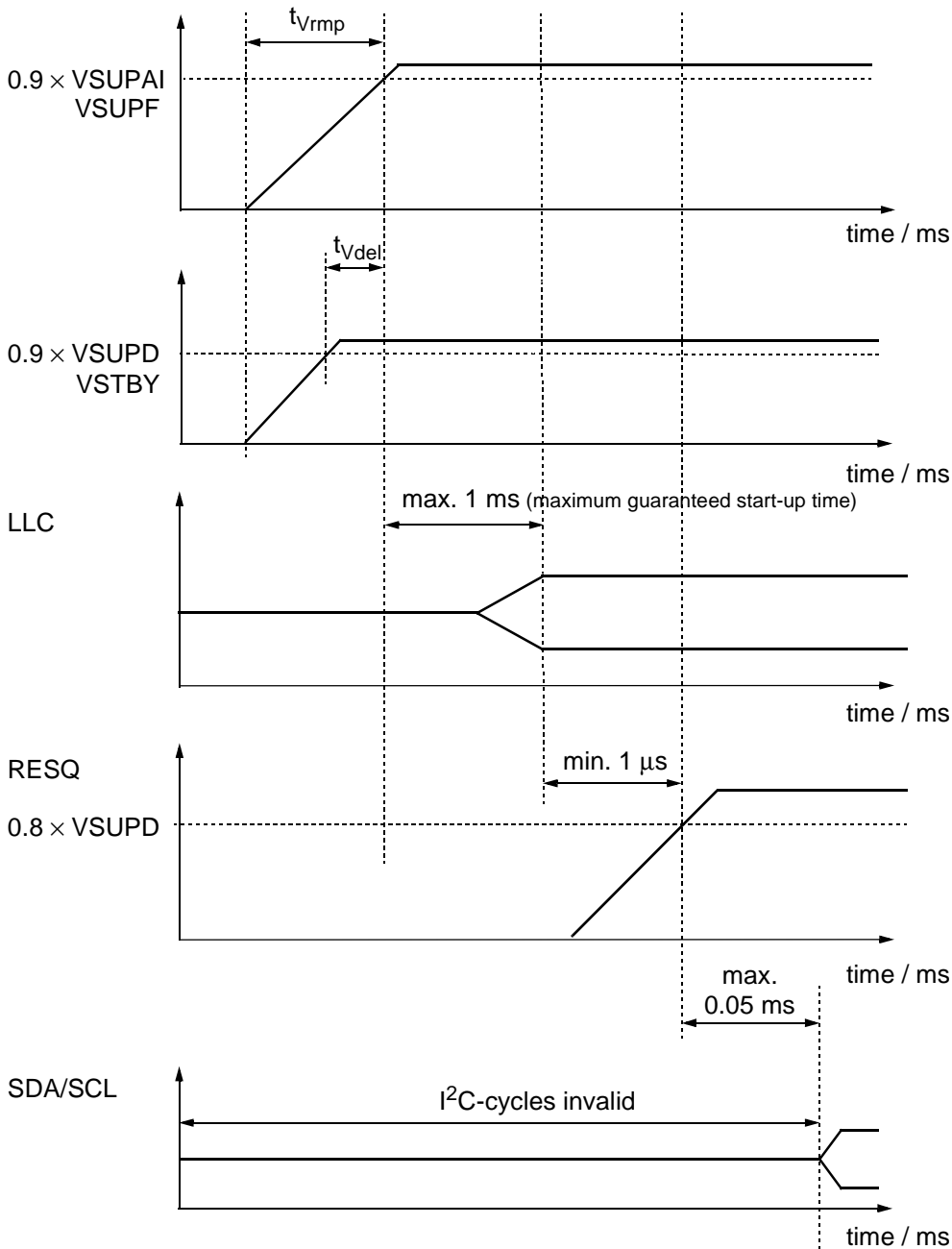


Fig. 3–23: Power-Up sequence

3.6.4.5. Test Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------|-------------------------|----------|------|------|------|------|------------------------------------|
| V _{IL} | Input Low Voltage | TEST | – | – | 0.8 | V | |
| V _{IH} | Input High Voltage | | 2.0 | – | – | V | |
| I _{pd} | Input Pull-Down Current | | 25 | 80 | 170 | μA | V _i = V _{SUPD} |

3.6.4.6. Analog Video Front-End and A/D Converters

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------|-----------------------------|----------|------|------|------|------------------|-------------------------|
| V _{VRT} | Reference Voltage Top | VRT | 2.5 | 2.6 | 2.8 | V | 10 μF/10 nF, 1 GΩ Probe |
| V _{VRTN} | Reference Voltage Top Noise | | – | – | 100 | mV _{PP} | |

Luma – Path

| | | | | | | | |
|---------------------|---|--------|-----|-------|------|-----------------|---|
| R _{VIN} | Input Resistance | VIN1-4 | 1 | – | – | MΩ | Code Clamp–DAC=0 |
| C _{VIN} | Input Capacitance | | – | 5 | – | pF | |
| V _{VIN} | Full Scale Input Voltage | | 1.8 | 2.0 | 2.2 | V _{PP} | min. AGC Gain |
| V _{VIN} | Full Scale Input Voltage | | 0.5 | 0.6 | 0.7 | V _{PP} | max. AGC Gain |
| AGC | AGC step width | | – | 0.166 | – | dB | 6-Bit Resolution= 64 Steps f _{sig} = 1 MHz, – 2 dBr of max. AGC–Gain |
| DNL _{AGC} | AGC Differential Non-Linearity | | – | – | ±0.5 | LSB | |
| V _{VINCL} | Input Clamping Level, CVBS | | – | 1.0 | – | V | Binary Level = 64 LSB min. AGC Gain |
| Q _{CL} | Clamping DAC Resolution | | –16 | – | 15 | steps | 5 Bit – I–DAC, bipolar V _{VIN} =1.5 V |
| I _{CL–LSB} | Input Clamping Current per step | | 0.7 | 1.0 | 1.3 | mA | |
| DNL _{ICL} | Clamping DAC Differential Non-Linearity | | – | – | ±0.5 | LSB | |

Chroma – Path (composite)

| | | | | | | | |
|--------------------|-----------------------------------|--------------|------|-----|------|-----------------|--|
| R _{CIN} | Input Resistance SVHS Chroma | CIN1 CIN2 | 1.4 | 2.0 | 2.6 | kΩ | |
| V _{CIN} | Full Scale Input Voltage, Chroma | | 1.08 | 1.2 | 1.32 | V _{PP} | |
| V _{CINDC} | Input Bias Level, SVHS Chroma | | – | 1.5 | – | V | |
| | Binary Code for Open Chroma Input | | – | 128 | – | – | |

Chroma – Path (component)

| | | | | | | | |
|------------------|--------------------------|---------------|------|------|------|-----------------|--------------------|
| R _{VIN} | Input Resistance | CBIN, CRIN | 1 | | | MΩ | Code Clamp–DAC = 0 |
| C _{VIN} | Input Capacitance | | | | 4.5 | pF | |
| V _{VIN} | Full Scale Input Voltage | | 0.76 | 0.84 | 0.92 | V _{PP} | minimal range |
| V _{VIN} | Full Scale Input Voltage | | 1.08 | 1.2 | 1.32 | V _{PP} | extended range |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--|--------------------------|------|------|------|-------|--|
| V _{INCL} | Input Clamping Level C _R , C _B | | | 1.5 | | V | Binary Level = 128 LSB |
| Q _{CL} | Clamping DAC Resolution | | -32 | | 31 | steps | 6 Bit – I-DAC, bipolar V _{VIN} = 1.5 V |
| I _{CL-LSB} | Input Clamping Current per step | | 0.59 | 0.85 | 1.11 | μA | |
| DNL _{ICL} | Clamping DAC Differential Non-Linearity | | | | ±0.5 | LSB | |
| Dynamic Characteristics for all Video-Paths (Luma + Chroma) | | | | | | | |
| BW | Bandwidth | VIN1-4 CIN1-2 CBIN | 8 | 10 | – | MHz | -2 dBr input signal level |
| XTALK | Crosstalk, any Two Video Inputs | | – | -56 | – | dB | 1 MHz, -2 dBr signal level |
| THD | Total Harmonic Distortion | | – | 50 | – | dB | 1 MHz, 5 harmonics, -2 dBr signal level |
| SINAD | Signal to Noise and Distortion Ratio | | – | 45 | – | dB | 1 MHz, all outputs, -2 dBr signal level |
| INL | Integral Non-Linearity | | – | – | ±1 | LSB | Code Density, DC-ramp |
| DNL | Differential Non-Linearity | | – | – | ±0.8 | LSB | |
| DG | Differential Gain | | – | – | ±3 | % | -12 dBr, 4.4 MHz signal on DC-ramp |
| DP | Differential Phase | | – | – | 1.5 | deg | |

3.6.4.7. Horizontal Flyback Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------|---|----------|------|------|------|------|----------------------|
| V_{IL} | Input Low Voltage | HFLB | – | – | 1.8 | V | |
| V_{IH} | Input High Voltage | | 2.6 | – | – | V | |
| V_{IHST} | Input Hysteresis | | 0.1 | – | – | V | |
| $PSRR_{HF}$ | Power Supply Rejection Ratio of Trigger Level | | 0 | – | – | dB | $f = 20 \text{ MHz}$ |
| $PSRR_{MF}$ | Power Supply Rejection Ratio of Trigger Level | | –20 | – | – | dB | $f < 15 \text{ kHz}$ |
| $PSRR_{LF}$ | Power Supply Rejection Ratio of Trigger Level | | –40 | – | – | dB | $f < 100 \text{ Hz}$ |

3.6.4.8. Horizontal Drive Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|----------|--|----------|------|------|------|------|----------------------------|
| V_{OL} | Output Low Voltage | HOUT | – | – | 0.4 | V | $I_{OL} = 10 \text{ mA}$ |
| V_{OH} | Output High Voltage (Open Drain Stage) | | – | – | 5 | V | external pull-up resistor |
| t_{OF} | Output Fall Time | | – | 8 | 20 | ns | $C_{LOAD} = 30 \text{ pF}$ |
| I_{OL} | Output Low Current | | – | – | 10 | mA | |

3.6.4.9. Vertical Protection Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|------------|--------------------|----------|------|------|------|------|-----------------|
| V_{IL} | Input Low Voltage | VPROT | – | – | 1.8 | V | |
| V_{IH} | Input High Voltage | | 2.6 | – | – | V | |
| V_{IHST} | Input Hysteresis | | 0.1 | – | – | V | |

3.6.4.10. Vertical Safety Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|------------|--------------------------|----------|------|------|------|------|-----------------|
| V_{ILA} | Input Low Voltage A | SAFETY | – | – | 1.8 | V | |
| V_{IHA} | Input High Voltage A | | 2.6 | – | – | V | |
| V_{ILB} | Input Low Voltage B | | – | – | 3.0 | V | |
| V_{IHB} | Input High Voltage B | | 3.8 | – | – | V | |
| V_{IHST} | Input Hysteresis A and B | | 0.1 | – | – | V | |
| t_{PID} | Internal Delay | | – | – | 100 | ns | |

3.6.4.11. Vertical and East/West D/A Converter Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------|-------------------------------|---------------------|------|------|------|------|---|
| V _{OMIN} | Minimum Output Voltage | EW VERT VERTQ | – | 0 | – | V | R _{load} = 6.8 kΩ R _{xref} = 10 kΩ |
| V _{OMAX} | Maximum Output Voltage | | 2.82 | 3 | 3.2 | V | R _{load} = 6.8 kΩ R _{xref} = 10 kΩ |
| I _{DACN} | Full scale DAC Output Current | | 415 | 440 | 465 | μA | R _{xref} = 10 kΩ |
| PSRR | Power Supply Rejection Ratio | | – | 20 | – | dB | |

3.6.4.12. Combined Sync, Vertical Sync, Interlace and Front Sync Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------|---------------------|--------------|----------------------------|------|-------------------|------|---------------------------|
| V _{OL} | Output Low Voltage | CSY VS | – | 0.2 | 0.4 | V | I _{OL} = 1.6 mA |
| V _{OH} | Output High Voltage | INTLC FSY | V _{SUPD} – 0.4 | – | V _{SUPD} | V | –I _{OL} = 1.6 mA |

3.6.4.13. CLK20 Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------|---------------------|----------|----------------------------|------|-------------------|------|--|
| V _{OL} | Output Low Voltage | CLK20 | – | 0.2 | 0.4 | V | I _{OL} = TBD; strenght = TBD |
| V _{OH} | Output High Voltage | | V _{SUPD} – 0.4 | – | V _{SUPD} | V | I _{OL} = TBD; strenght = TBD |

3.6.4.14. Sense A/D Converter Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------|-------------------------------|----------|------|------|--------------------|------|---|
| V _I | Input Voltage Range | SENSE | 0 | – | V _{SUPAB} | V | |
| V _{I255} | Input Voltage for code 255 | | 1.4 | 1.54 | 1.7 | V | Read cutoff blue register |
| C ₀ | Digital Output for zero Input | | – | – | 16 | LSB | Offset check, read cutoff blue register |
| R _I | Input Impedance | | 1 | – | – | MΩ | |

3.6.4.15. Range Switch Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------|----------------------|--------------|------|------|------|------|-------------------------|
| R _{ON} | Output On Resistance | RSW1 RSW2 | – | – | 50 | Ω | I _{OL} = 10 mA |
| I _{Max} | Maximum Current | | – | – | 15 | mA | |
| I _{LEAK} | Leakage Current | | – | – | 600 | nA | RSW High Impedance |

3.6.4.16. Scan Velocity Modulation Output

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------|---------------------------|----------|------|-------|------|------|---|
| | Resolution | SVMOUT | – | 8 | – | bit | |
| I_{OUT} | Full Scale Output Current | | 1.55 | 1.875 | 2.25 | mA | |
| I_{OUT} | Differential Nonlinearity | | – | – | 0.5 | LSB | |
| I_{OUT} | Integral Nonlinearity | | – | – | 1 | LSB | |
| I_{OUT} | Glitch Pulse Charge | | – | 0.5 | – | pAs | Ramp, output line is terminated on both ends with 50 Ω |
| I_{OUT} | Rise and Fall Time | | – | 3 | – | ns | 10 % to 90 %, 90 % to 10 % |

3.6.4.17. D/A Converter Reference

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------|--|----------|------|------|------|------------|---------------------------------|
| V_{DACREF} | DAC-Ref. Voltage | VRD | 2.38 | 2.50 | 2.63 | V | |
| V_{DACR} | DAC-Ref. Output resistance | | 18 | 25 | 32 | k Ω | |
| V_{XREF} | DAC-Ref. Voltage Bias Current Generation | XREF | 2.38 | 2.5 | 2.63 | V | $R_{xref} = 10 \text{ k}\Omega$ |

3.6.4.18. Analog RGB and FB Inputs

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|----------------------------|------|------|----------|---|--|
| RGB Input Characteristics | | | | | | | |
| V_{RGBIN} | External RGB Inputs Voltage Range | RIN1/2 GIN1/2 BIN1/2 | -0.3 | - | 1.1 | V | |
| V_{RGBIN} | nominal RGB Input Voltage peak-to-peak | | 0.5 | 0.7 | 1.0 | V_{PP} | SCART Spec: 0.7 V \pm 3 dB |
| V_{RGBIN} | RGB Inputs Voltage for Maximum Output Current | | - | 0.44 | - | V | Contrast setting: 511 |
| | | | - | 0.7 | - | V | Contrast setting: 323 |
| | | | - | 1.1 | - | V | Contrast setting: 204 |
| t_{CLP} | Clamp Pulse Width | | 1.6 | - | - | μ s | |
| C_{IN} | Input Capacitance | | - | - | 13 | pF | |
| I_{IL} | Input Leakage Current | | -0.5 | - | 0.5 | μ A | Clamping OFF, $V_{IN} = -0.3...3$ V |
| V_{CLIP} | RGB Input Voltage for Clipping Current | | - | 2 | - | V | |
| V_{CLAMP} | Clamp Level at Input | | 40 | 60 | 80 | mV | Clamping ON |
| V_{INOFF} | Offset Level at Input | | -10 | - | 10 | mV | Extrapolated from $V_{IN} = 100$ and 200 mV |
| V_{INOFF} | Offset Level Match at Input | | -10 | - | 10 | mV | Extrapolated from $V_{IN} = 100$ and 200 mV |
| R_{CLAMP} | Clamping-ON-Resistance | - | 140 | - | Ω | | |
| Fast Blank Input Characteristics | | | | | | | |
| V_{FBLOFF} | FBLIN Low Level | FBLIN1/2 | - | - | 0.5 | V | |
| V_{FBLON} | FBLIN High Level | | 0.9 | - | - | V | |
| $V_{FBLTRIG}$ | Fast Blanking Trigger Level typical | | - | 0.7 | - | V | |
| t_{PID} | Delay Fast Blanking to RGB_{OUT} from midst of FBLIN-transition to 90 % of RGB_{OUT} transition | | - | 8 | 15 | ns | Internal RGB = 3.75 mA Full Scale Int. Brightness = 0 External Brightness = 1.5 mA (Full Scale) RGBin = 0 $V_{FBLOFF} = 0.4$ V $V_{FBLON} = 1.0$ V Rise and fall time = 2 ns |
| | Difference of Internal Delay to External RGBin Delay | | -5 | - | +5 | ns | |
| | Switch-Over-Glitch | - | 0.5 | - | pAs | Switch from 3.75 mA (int) to 1.5 mA (ext) | |

3.6.4.19. Half Contrast Switch Input

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------|---|----------|------|------|------|------|---|
| V_{IL} | Input Low Voltage | HCS | – | – | 0.8 | V | |
| V_{IH} | Input High Voltage | | 1.5 | – | – | V | |
| t_{HCS} | Delay HCS to RGB_{OUT} from 50 % of HCS-transition to 90 % of RGB_{OUT} -transition | | | 80 | 120 | ns | Internal GRB = 3.75 mA $V_{HCSL} = 0.4$ V $V_{HCSH} = 1.0$ V Rise and fall time = 2 ns |

3.6.4.20. Analog RGB Outputs, D/A Converters

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---|----------------------|------|------|------|------|---|
| Internal RGB Signal D/A Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 10 | – | bit | |
| I_{OUT} | Full Scale Output Current | | 3.6 | 3.75 | 3.9 | mA | $R_{ref} = 10$ k Ω |
| I_{OUT} | Differential Nonlinearity | | – | – | 0.5 | LSB | |
| I_{OUT} | Integral Nonlinearity | | – | – | 1 | LSB | |
| I_{OUT} | Glitch Pulse Charge | | – | 0.5 | – | pAs | Ramp signal, 25 Ω output termination |
| I_{OUT} | Rise and Fall Time | | – | 3 | – | ns | 10 % to 90 %, 90 % to 10 % |
| I_{OUT} | Intermodulation | | – | – | –50 | dB | 2/2.5 MHz full scale |
| I_{OUT} | Signal to Noise | | +50 | – | – | dB | Signal: 1 MHz full scale Bandwidth: 10 MHz |
| I_{OUT} | Matching R-G, R-B, G-B | | –2 | – | 2 | % | |
| | R/B/G Crosstalk one channel talks two channels talk | | – | – | –46 | dB | Passive channel: $I_{OUT} = 1.88$ mA Crosstalk-Signal: 1.25 MHz, 3.75 mA _{PP} |
| | RGB Input Crosstalk from external RGB one channel talks two channels talk three channels talk | – | – | –50 | dB | | |
| | | – | – | –50 | dB | | |
| Internal RGB Brightness D/A Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 9 | – | bit | |
| I_{BR} | Full Scale Output Current relative | | 39.2 | 40 | 40.8 | % | Ref to max. digital RGB |
| I_{BR} | Full Scale Output Current absolute | | – | 1.5 | – | mA | |
| I_{BR} | Differential Nonlinearity | | – | – | 1 | LSB | |
| I_{BR} | Integral Nonlinearity | | – | – | 2 | LSB | |
| I_{BR} | Match R-G, R-B, G-B | | –2 | – | 2 | % | |
| I_{BR} | Match to digital RGB R-R, G-G, B-B | | –2 | – | 2 | % | |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|----------------------|--------|------------|--------|----------|---|
| External RGB Voltage/Current Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 9 | – | bit | |
| I _{EXOUT} | Full Scale Output Current relative | | 96 | 100 | 104 | % | Ref. to max. Digital RGB V _{IN} = 0.7 V _{PP} contrast = 323 |
| | Full Scale Output Current absolute | | – | 3.75 | – | mA | Same as Digital RGB |
| CR | Contrast Adjust Range | | – | 16:511 | – | | |
| | Gain Match R-G, R-B, G-B | | –2 | – | 2 | % | Measured at RGB Outputs V _{IN} = 0.7 V, contrast = 323 |
| | Gain Match to RGB-DACs R-R, G-G, B-B | | –3 | – | 3 | % | Measured at RGB Outputs V _{IN} = 0.7 V, contrast = 323 |
| | R/B/G Input Crosstalk one channel talks two channels talk | | – | – | –46 | dB | Passive channel: V _{IN} = 0.7 V, contrast = 323 Crosstalk signal: 1.25 MHz, 3.75 mA _{PP} |
| | RGB Input Crosstalk from Internal RGB one channel talks two channels talk tree channels talk | | – | – | –50 | dB | |
| | RGB Input Noise and Distortion | | – | – | –50 | dB | V _{IN} =0.7 V _{PP} at 1 MHz contrast = 323 Bandwidth: 10 MHz |
| | RGB Input Bandwidth –3dB | | | 15 | – | MHz | V _{IN} = 0.7 V _{PP} contrast =323 |
| | RGB Input THD | | – – | –50 –40 | – – | dB dB | Input signal 1 MHz Input signal 6 MHz V _{IN} = 0.7 V _{PP} contrast =323 |
| | Differential Nonlinearity of Contrast Adjust | | – | – | 1 | LSB | V _{IN} = 0.44 V |
| | Integral Nonlinearity of Contrast Adjust | | – | – | 2 | LSB | |
| V _{RGBO} | R,G,B Output Voltage | | –1.0 | – | 0.3 | V | Referred to V _{SUPO} |
| | R,G,B Output Load Resistance | | – | – | 100 | Ω | Ref. to V _{SUPO} |
| V _{OUTC} | RGB Output Compliance | | –1.5 | –1.3 | –1.2 | V | Ref. to V _{SUPO} Sum of max. Current of RGB- DACs and max. Current of Int. Brightness DACs is 2 % degraded |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---------------------------------------|----------------------|------|------|------|------|-------------------------|
| External RGB Brightness D/A Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 9 | – | bit | |
| I _{EXBR} | Full Scale Output Current relative | | 39.2 | 40 | 40.8 | % | Ref to max. digital RGB |
| | Full Scale Output Current absolute | | – | 1.5 | – | mA | |
| | Differential Nonlinearity | | – | – | 1 | LSB | |
| | Integral Nonlinearity | | – | – | 2 | LSB | |
| | Matching R-G, R-B, G-B | | –2 | – | 2 | % | |
| | Matching to digital RGB R-R, G-G, B-B | | –2 | – | 2 | % | |
| RGB Output Cutoff D/A Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 9 | – | bit | |
| I _{CUT} | Full Scale Output Current relative | | 58.8 | 60 | 61.2 | % | Ref to max. digital RGB |
| | Full Scale Output Current absolute | | – | 2.25 | – | mA | |
| | Differential nonlinearity | | – | – | 1 | LSB | |
| | Integral nonlinearity | | – | – | 2 | LSB | |
| | Matching to digital RGB R-R, G-G, B-B | | –2 | – | 2 | % | |
| RGB Output Ultrablack D/A Converter Characteristics | | | | | | | |
| | Resolution | ROUT GOUT BOUT | – | 1 | – | bit | |
| I _{UB} | Full Scale Output Current relative | | 19.6 | 20 | 20.4 | % | Ref to max. digital RGB |
| | Full Scale Output Current absolute | | – | 0.75 | – | mA | |
| | Match to digital RGB R-R, G-G, B-B | | –2 | – | 2 | % | |

3.6.4.21. IO Ports

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|----------|-----------------------|-----------|--------------------------|------|------|---------------|------------------------|
| V_{ol} | Output Low Voltage | PORT[6:0] | – | – | 0.4 | V | $I_o = 3 \text{ mA}$ |
| V_{oh} | Output High Voltage | | $V_{SUPD} - 0.4$ | – | – | V | $I_o = -3 \text{ mA}$ |
| V_{ol} | Output Low Voltage | | | | 1 | V | $I_o = 10 \text{ mA}$ |
| V_{oh} | Output High Voltage | | $V_{SUPD} - 1 \text{ V}$ | | | | $I_o = -10 \text{ mA}$ |
| V_{IL} | Input Low Voltage | | – | – | 0.8 | V | |
| V_{IH} | Input High Voltage | | 2.0 | – | – | V | |
| I_i | Input Leakage Current | | –0.1 | – | 0.1 | μA | $0 < V_i < V_{SUPP}$ |

4. Application Circuit

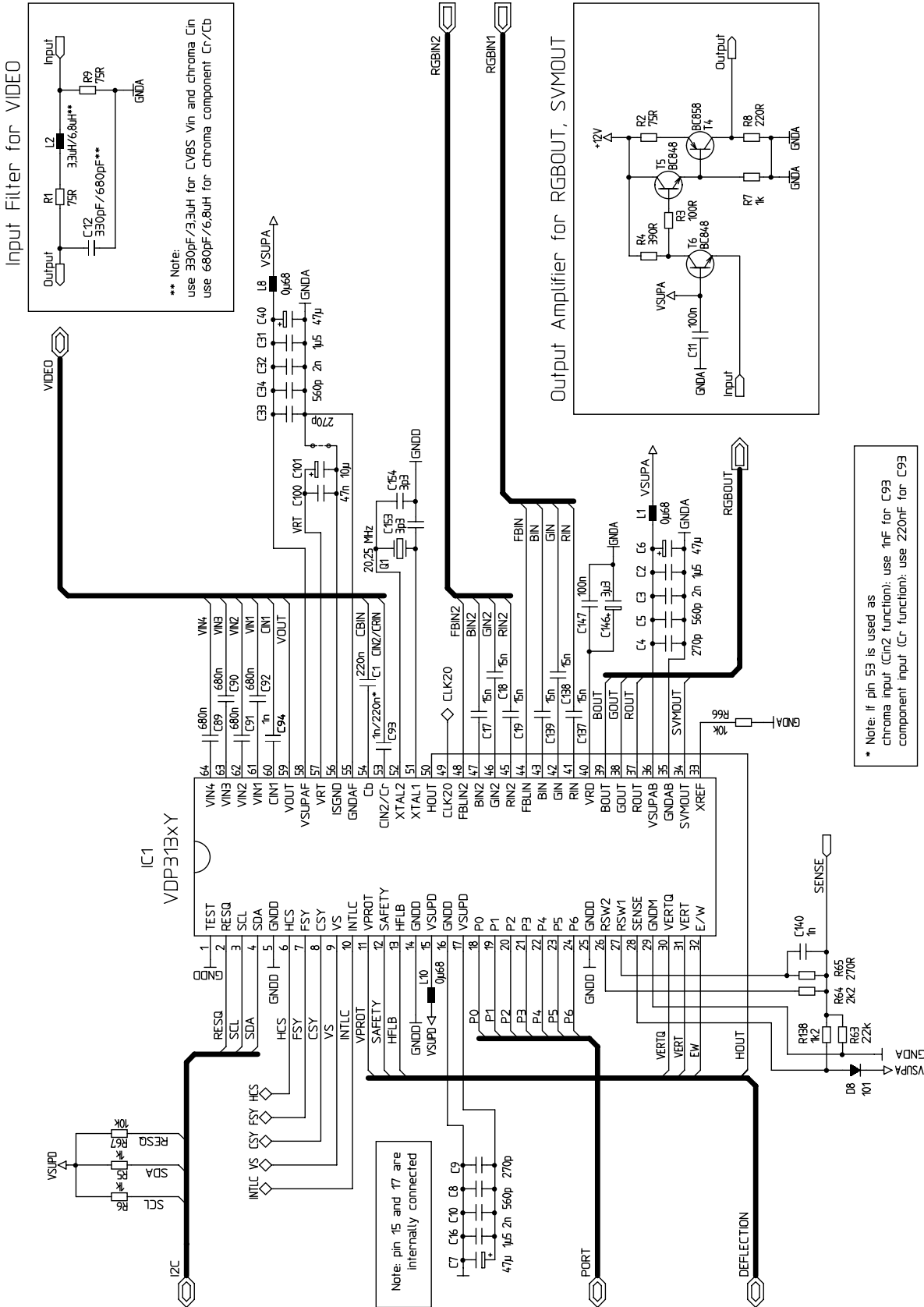


Fig. 4-1: VDP 313xY Application Circuit

5. Data Sheet History

1. Advance Information: "VDP 313xY Video Processor Family", August 15, 2000, 6251-519-1AI. First release of the advance information.

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