



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package		
			TO-39	TO-92	TO-220
30V	1.2Ω	2.0A	VN0300B	VN0300L	VN0300D

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

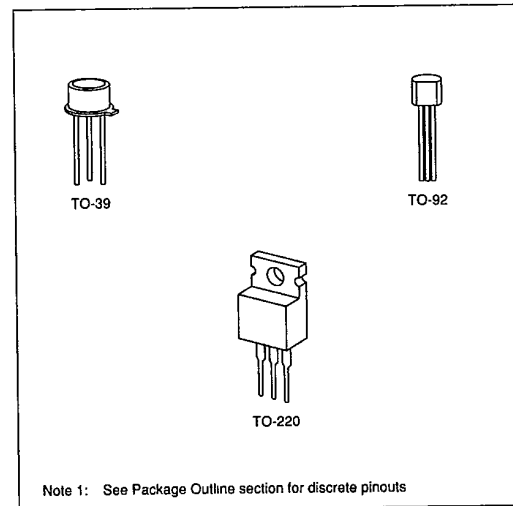
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

T-39-09

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{JA} °C/W	θ_{JC} °C/W
TO-39	1.2A	3A	6.25W	170	20
TO-92	.4A	3A	.4W	312.5	43.5
TO-220	2.11A	6A	20W	80	6.25

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30			V	$I_D = 10\mu A, V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	.8		2.5	V	$V_{GS} = V_{DS}, I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 30V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				500		$V_{GS} = 0V, V_{DS} = \text{Max Rating}$ $T_A = 125^\circ C$
$I_{D(ON)}$	ON-State Drain Current	2			A	$V_{GS} = .10V, V_{DS} \geq 2 V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.3	Ω	$V_{GS} = 5V, I_D = .3A$
				1.2		$V_{GS} = 10V, I_D = 1A$
G_{FS}	Forward Transconductance	200			m Ω	$V_{DS} \geq 2 V_{DS(ON)}, I_D = 0.5A$
C_{ISS}	Input Capacitance			100	pF	$V_{GS} = 0, V_{DS} = 15V$ $f = 1MHz$
C_{OSS}	Common Source Output Capacitance			95		
C_{RSS}	Reverse Transfer Capacitance			25		
$t_{(ON)}$	Turn-ON Time			30	ns	$V_{DD} = 25V, I_D = 1.0$ $R_S = 50\Omega$
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		-0.9		V	$I_{SD} = 0.63A, V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
 Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

