Supertex inc.

VN6035L

T-35-25

Objective

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package
			TO-92
600V	35Ω	2.8V	VN6035L

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Telecom Switching
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-92	110mA	500mA	1W	125	170	110mA	500mA

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	600			V	V_{GS} = 0, I_D = 100µA
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.8	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			50	µA	V_{GS} = 0, V_{DS} = Max Rating
				200		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$V_{DS(ON)}$	Static Drain-Source ON-State Voltage			1.75	V	V_{GS} = 10V, I_D = 50mA
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			35	Ω	V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward Transconductance	0.100			℧	V_{DS} = 25V, I_D = 50mA
C_{ISS}	Input Capacitance			80	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 25V, I_D = 50mA, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time			100	ns	V_{DD} = 25V, I_D = 50mA, R_S = 50Ω
V_{SD}	Diode Forward Voltage Drop			1.2	V	V_{GS} = 0, I_S = 110mA, T_A = 25°C

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit