TOPAZ SEMICONDUCTOR

VP0535, VP0540

P-CHANNEL ENHANCEMENT-MODE D-MOS FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	VP0535ND	VP0540ND
TO-92 Plastic Package	VP0535N3	VP0540N3
Description	-350V, 75Ω	-400V, 75Ω

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Low Output and Transfer Capacitances
- N-Channel Complements Available
- High Drain-Source Breakdown

APPLICATIONS

- Motor Controls
- Logic Interfaces
- Pulse Amplifiers
- Level Translators

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage
- VP0535 ..... -350V
- VP0540 ..... -400V

Drain-Gate Voltage (R_{GS} = 1MΩ)
- VP0535 ..... -350V
- VP0540 ..... -400V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_C = +100°C	T_C = -25°C
TO-92 Pkg.	-.05A	-.14A

Peak Pulsed Drain Current ..... -0.2A

Maximum Power Dissipation

	T_C = +100°C	T_C = +25°C
TO-92 Pkg.	0.4W	3.0W

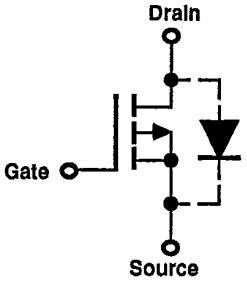
Linear Derating Factor

	Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
TO-92 Pkg.	3.0	24

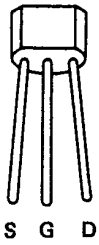
Operating Junction and Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 10 Sec) ..... +300°C

PIN CONFIGURATION

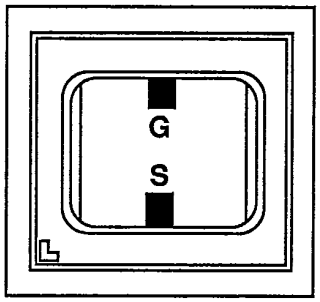


TO-226A (TO-92)



See Package 5

CHIP CONFIGURATION



Dimensions: 0.054 x 0.051 x 0.020 inches
Drain is backside contact

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ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTICS		VP0535 MIN	VP0535 TYP	VP0535 MAX	VP0540 MIN	VP0540 TYP	VP0540 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-350			-400			V	I_D = -1.0mA, V_{GS} = 0	
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2.0		-4.5	-2.0		-4.5	V	V_{DS} = V_{GS} I_D = -1.0mA	
3		I_{GSS}	Gate-Body Leakage Current			-100			-100	nA	V_{GS} = -30V, V_{DS} = 0	
4						100			100		V_{GS} = +30V, V_{DS} = 0	
5		I_{DSS}	Drain-Source OFF Leakage Current		-.01	-10				µA	V_{DS} = -350V V_{GS} = 0	
6					-.03	-500					V_{DS} = -280V V_{GS} = 0	T_C=+125°C
7								-.01	-10		V_{DS} = -400V V_{GS} = 0	
8								-.03	-500		V_{DS} = -320V V_{GS} = 0	T_C=+125°C
9		$I_{D(on)}$	ON Drain Current(1)	-25	-120		-25	-120		mA	V_{DS} = -25V	V_{GS}=-5V
10				-200	-400		-200	-400				V_{GS} = -10V
11		$r_{DS(on)}$	Drain-Source(1) ON Resistance		55	100		55	100	ohms	V_{GS} = -5V	
12					78	170		78	170		I_D = -10mA	T_C=+125°C
13					48	75		48	75		V_{GS} = -10V	
14					73	125		73	125		I_D = -50mA	T_C=+125°C
15	DYNAMIC	g_{fs}	Common-Source(1) Forward Transcond.	50	110		50	100		mS	V_{DS} = -25V, I_D = -50mA, f = 1KHz	
16		C_{iss}	Common-Source Input Capacitance			60			60	pF	V_{DS} = -25V, V_{GS} = 0 f = 1MHz	
17		C_{rss}	Common-Source Reverse Transfer Capacitance			5.0			5.0			
18		C_{oss}	Common-Source Output Capacitance			20			20			
19		$t_{d(on)}$	Turn-ON Delay Time			10			10	nsec	V_{DD} = -25V R_L = 100Ω R_G = 51Ω $V_{GS(on)}$ = -10V	
20		t_r	Rise Time			15			15			
21		$t_{d(off)}$	Turn-OFF Delay Time			15			15			
22		t_f	Fall Time			10			10			
23	DIODE	I_S	Continuous Source Current	-.05			-.05			A		
24		I_{SM}	Peak Source Current(1)			-0.2			-0.2			
25		V_{DS}	Source-Drain(1) Forward Voltage		1.2			1.2		V	V_{GS} = 0, I = .14A	

Note 1: Pulse Test 80µSec, 1% Duty Cycle

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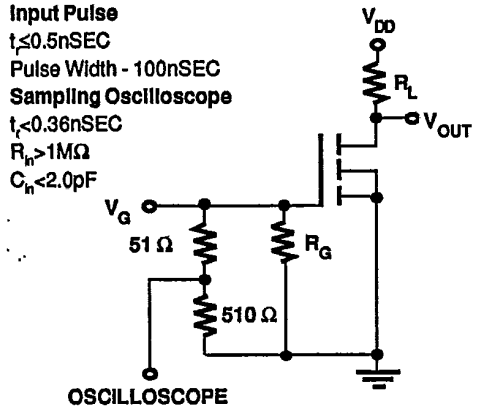
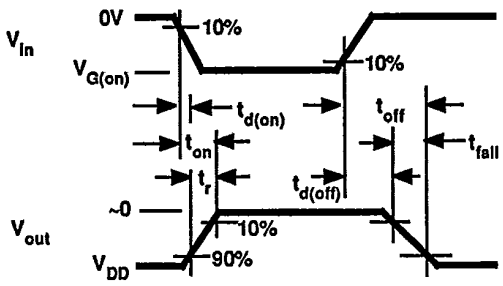
SWITCHING TIMES TEST CIRCUIT

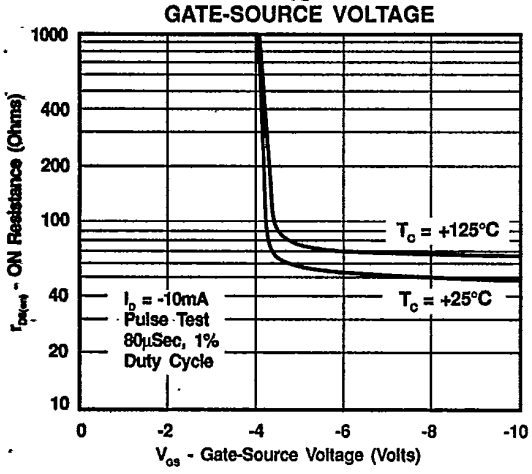


TEST WAVEFORMS

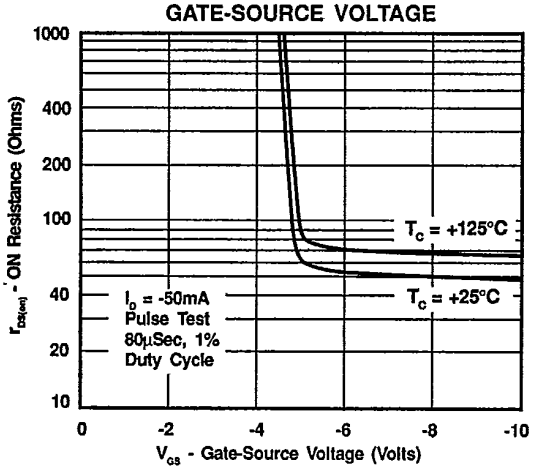


TYPICAL PERFORMANCE CHARACTERISTICS (T_C = +25°C unless otherwise noted)

ON RESISTANCE -vs- GATE-SOURCE VOLTAGE



ON RESISTANCE -vs- GATE-SOURCE VOLTAGE



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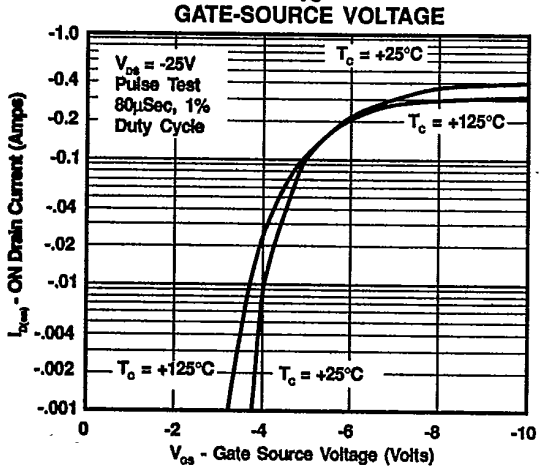
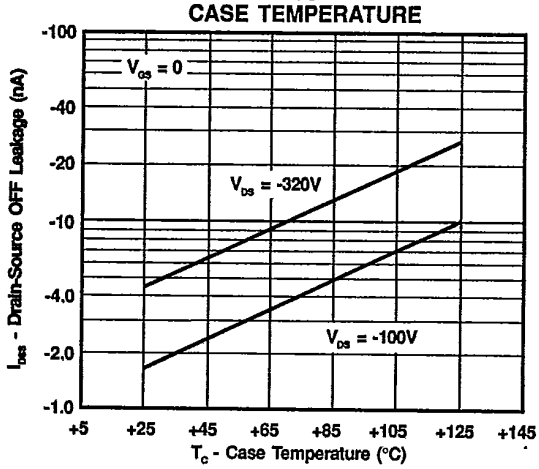
TYPICAL PERFORMANCE CHARACTERISTICS (T_C = +25°C unless otherwise noted)

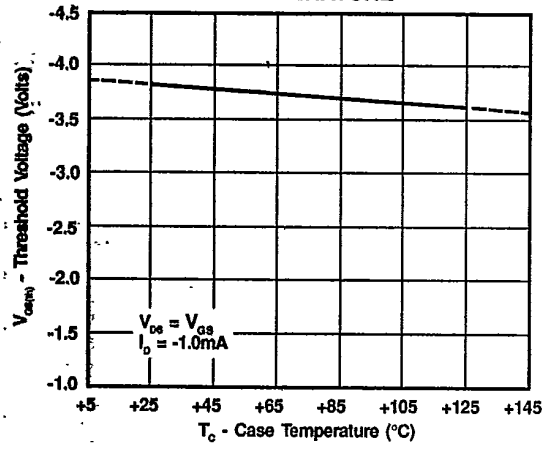
ON DRAIN CURRENT
-VS-
GATE-SOURCE VOLTAGE



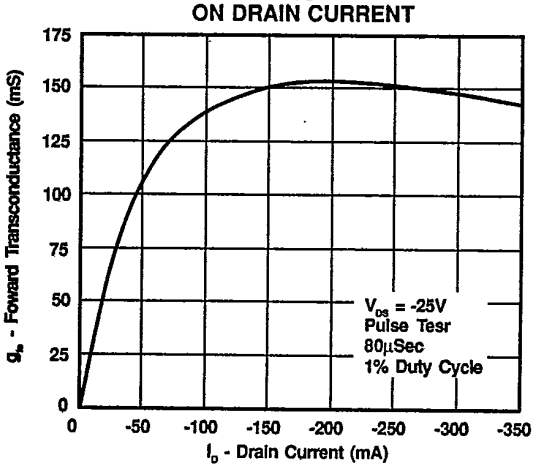
DRAIN-SOURCE OFF LEAKAGE CURRENT
-VS-
CASE TEMPERATURE



GATE-SOURCE THRESHOLD VOLTAGE
-VS-
TEMPERATURE



FORWARD TRANSCONDUCTANCE
-VS-
ON DRAIN CURRENT



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