



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-160V	2.5Ω	-4.0A	VP1216N1	VP1216N2	VP1216N5	VP1216ND
-200V	2.5Ω	-4.0A	VP1220N1	VP1220N2	VP1220N5	VP1220ND

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

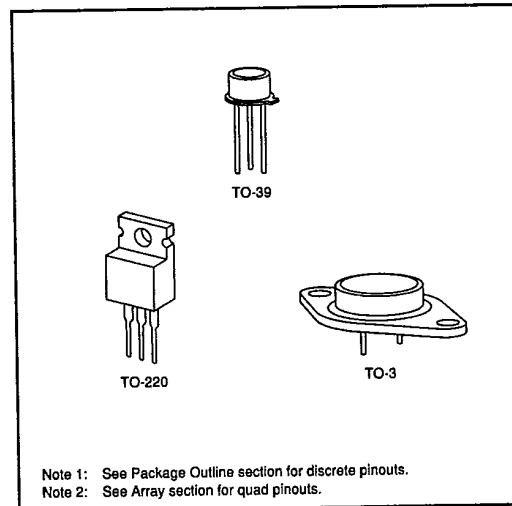
Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
 Note 2: See Array section for quad pinouts.

Thermal Characteristics

VP12C

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Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jC} °C/W	θ_{jA} °C/W	I_{DR}	I_{DRM}
TO-3	-4.5A	-8.0A	100W	30	1.25	-4.5A	-8.0A
TO-39	-2.0A	-4.5A	6.5W	125	20	-2.0A	-4.5A
TO-220	-3.5A	-6.0A	45W	70	2.75	-3.5A	-6.0A

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

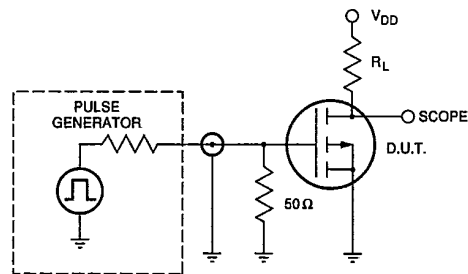
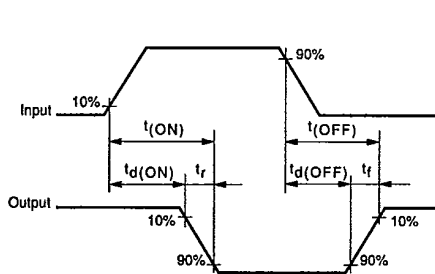
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1220 -200			V	$I_D = -10\text{mA}, V_{GS} = 0$
		VP1216 -160				
$V_{GS(th)}$	Gate Threshold Voltage	-1.5		-3.5	V	$V_{GS} = V_{DS}, I_D = -10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.5	-4.5	mV/°C	$V_{GS} = V_{DS}, I_D = -10\text{mA}$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		-1.0	-100	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				-10	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.5	-1.0		A	$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
		-4.0	-7.0			$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	4.0	Ω	$V_{GS} = -5\text{V}, I_D = -0.5\text{A}$
			1.6	2.5		$V_{GS} = -10\text{V}, I_D = -1.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.5	1.0	%/°C	$I_D = -1\text{A}, V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance	0.8	1.2		S	$V_{DS} = -25\text{V}, I_D = -3.0\text{A}$
C_{ISS}	Input Capacitance		600	650	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		200	250		
C_{RSS}	Reverse Transfer Capacitance		20	30		
$t_{d(ON)}$	Turn-ON Delay Time		30	40	ns	$V_{DD} = -15\text{V}$ $I_D = -2.0\text{A}$ $R_S = 50\Omega$
t_r	Rise Time		26	35		
$t_{d(OFF)}$	Turn-OFF Delay Time		45	90		
t_f	Fall Time		20	40		
V_{SD}	Diode Forward Voltage Drop		-1.4	-2.0	V	$I_{SD} = -0.5\text{A}, V_{GS} = 0$
t_{rr}	Reverse Recovery Time		500		ns	$I_{SD} = -0.5\text{A}, V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

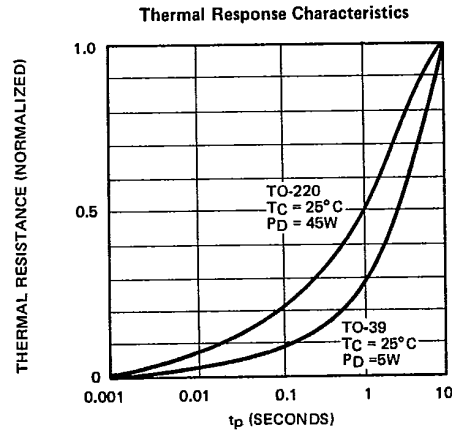
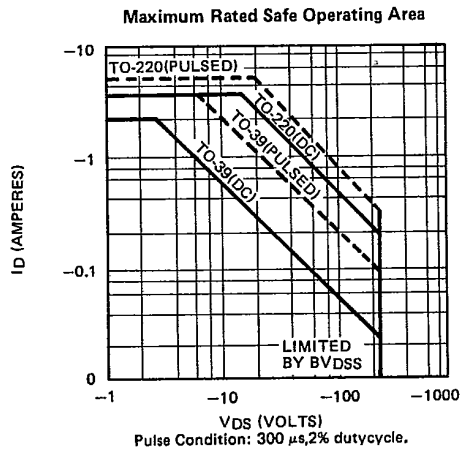
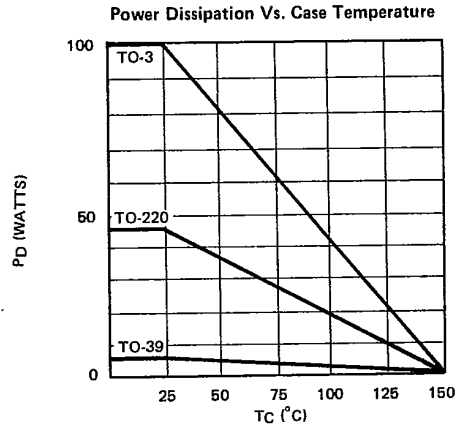
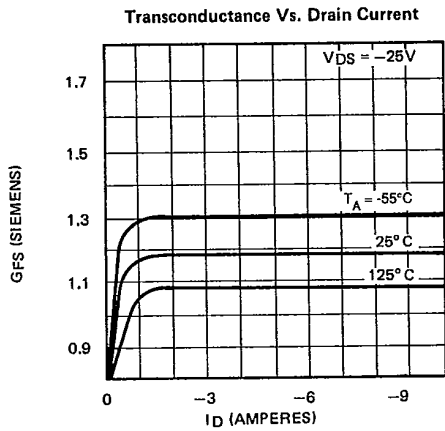
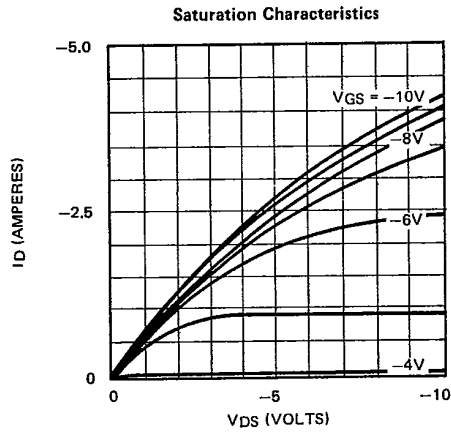
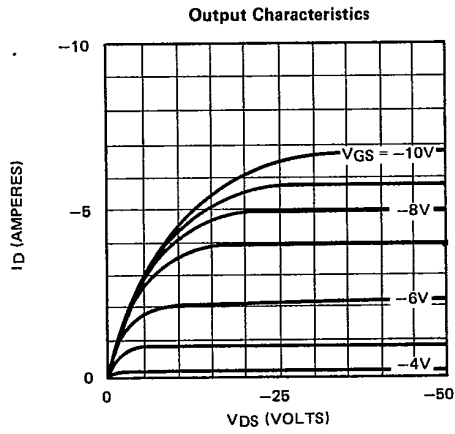
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



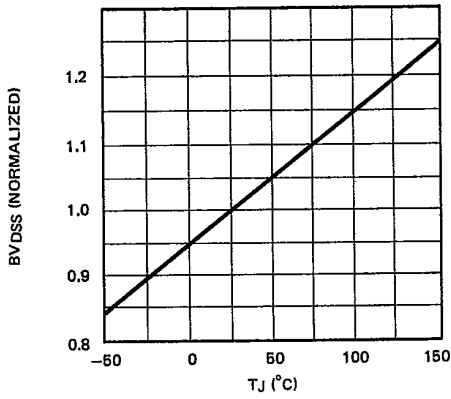
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Typical Performance Curves

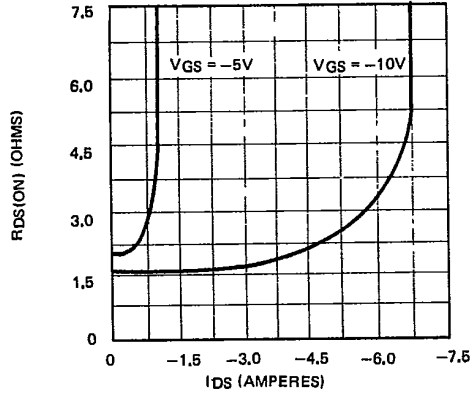


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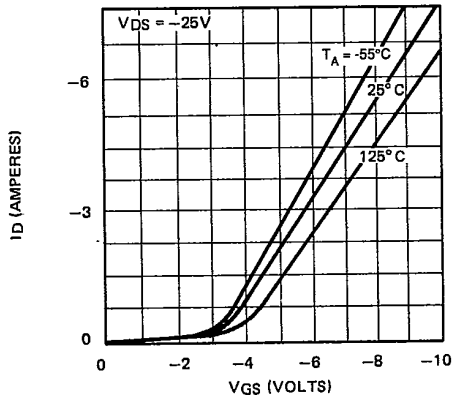
BVDSS Variation with Temperature



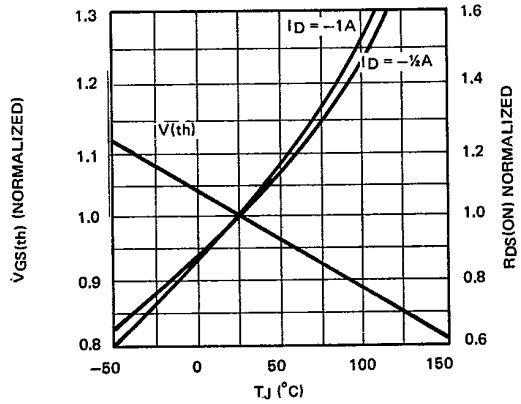
ON-Resistance Vs. Drain Current



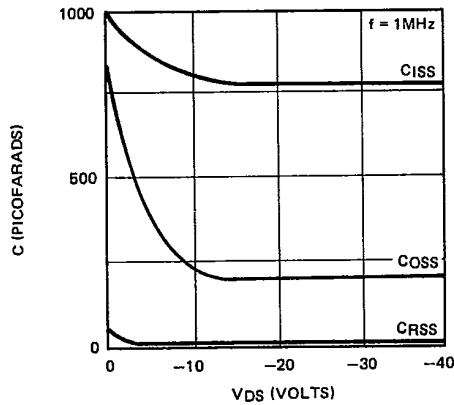
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

