VP216

Dual 90MHz 6-Bit Analog to Digital Converter with VCO

Preliminary Information

DS4070 - 1.6 May 1996

The VP216 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP216 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC, VCO or Ext. clock interface. The VP216 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- VCO or Ext. Clock Interface
- High Bandwidth ADC Driver Amplifier
- Internal ADC Reference
- TTL Data Outputs
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP216A CG HP1S (Commercial - 44 pin PLCC)

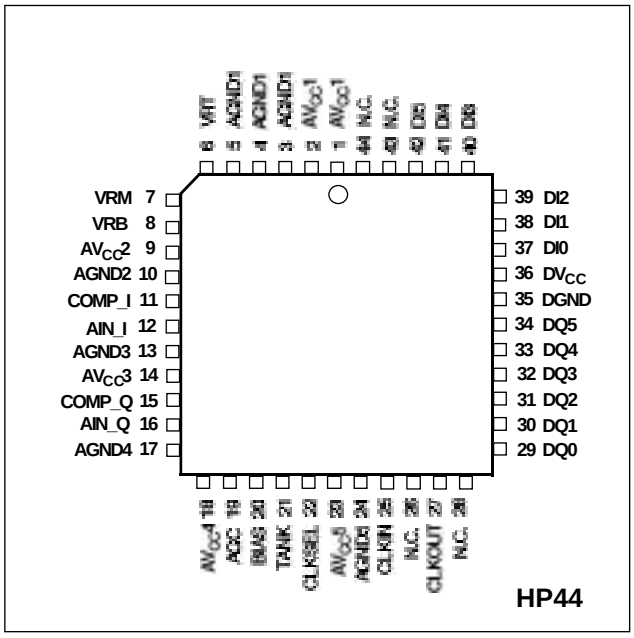


Fig.1 Pin connections - top view

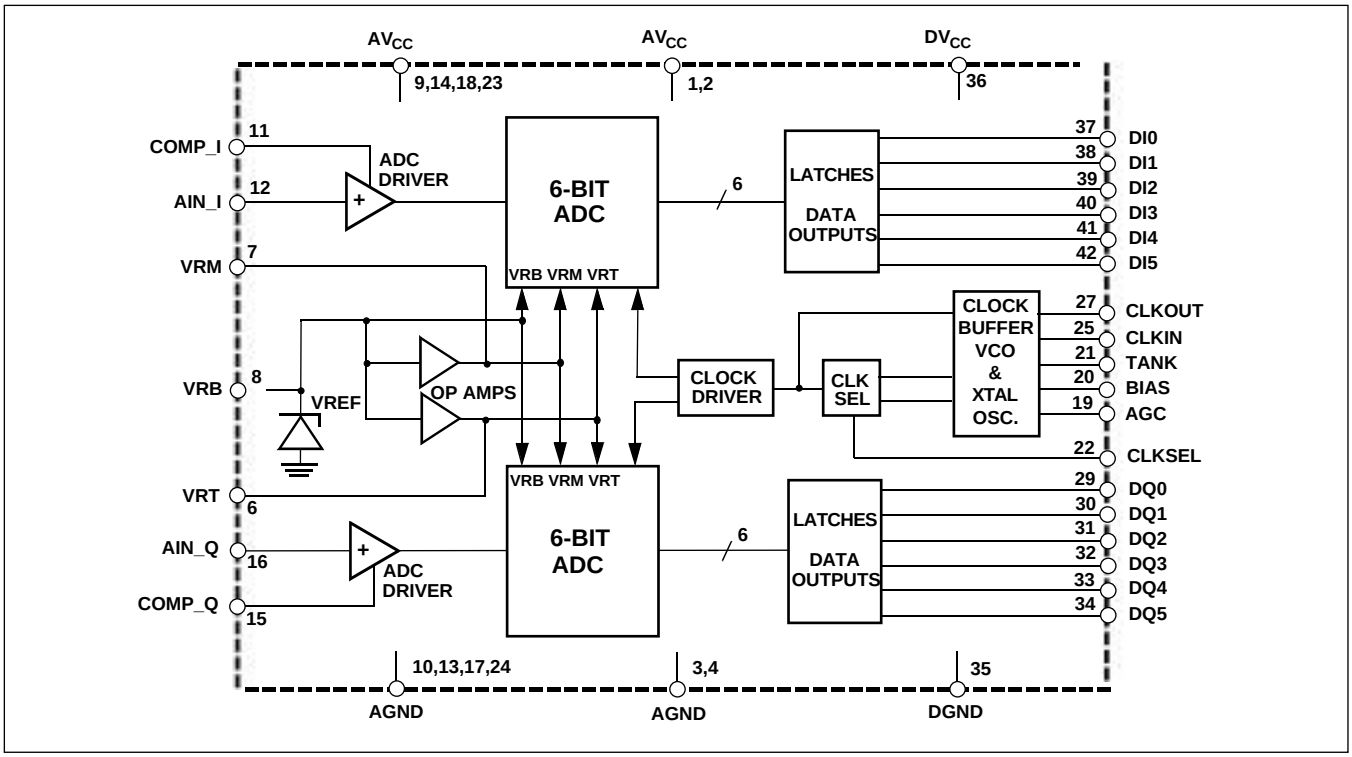


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CC})	-0.3 to +7V
Analog input voltage (AIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKSEL, MSBSEL)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES	
Junction to case(Θjc)	19°C/W
Junction to ambient(ΘjA)	55°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, AV_{CC} = DV_{CC} = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Missing codes		Full	4	Guaranteed				
Power supply								
Analog supply voltage	AV_{CC}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	DV_{CC}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	60	72	85	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	15	23	30	mA	
		Full	4	-	-	-	mA	
Power dissipation	P	+25°C	1	375	475	575	mW	
		Full	4	-	-	-	mW	
Analog input								
Input range	V_{in}	Full	5	-	1.0	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	4.5k	5.75k	7.5k	Ω	
Input capacitance	C_{in}	+25°C	5	-	3.0	-	pF	
Gain matching	A_{VH}	+25°C	1	-	-	0.25	dB	
Input -3dB bandwidth	F3dB	+25°C	4	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.6	3.85	4.1	V	
Comp output	Vcomp	+25°C	1	1.6	1.8	2.0	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	DV_{CC}= 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	–0.2	-	–0.5	mA	DV_{CC}= 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	DV_{CC} = 4.75V
		Full	4	-	-	-	V	I_{oh} = -400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	DV_{CC} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	–400	µA	DV_{CC} = 4.75V
		Full	4	-	-	-	-	
Output current low	I_{ol}	+25°C	1	-	-	1	mA	DV_{CC} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
CLKSEL								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1.0	µA	DV_{CC} = 5.25V
		Full	4	-	-	-		V_{ih} = 2.7V
Input current low	I_{il}	+25°C	1	–50	–100	–150	µA	DV_{CC} = 5.25V
		Full	4	-	-	-		V_{il} = 0.4V
VCO								
Input capacitance	C_{tank}	+25°C	5	-	2.0	-	pF	
Bias voltage	V_{bias}	+25°C	1	1.4	1.6	1.8	V	
AGC voltage	V_{agc}	+25°C	1	1.3	1.65	1.7	V	
Reference voltage								
REF 2.5	VRB	+25°C	1	2.374	2.525	2.677	V	} no load
REF 3.0	VRM	+25°C	1	2.848	3.03	3.212	V	
REF 3.5	VRT	+25°C	1	3.323	3.55	3.747	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	30	50	70	%	Cload=10pF
Clock low pulse width	$T_{pw}0$	+25°C	4	30	50	70	%	Cload=10pF
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data setup time	T_{su}	Full	4	8	10	-	ns	
Data hold time	T_h	Full	4	2	4	-	ns	
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.2	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	1	–0.95	-	+1.2	LSB	A_{IN}=15MHz
Integral non-linearity	INL	+25°C	1	-	-	±1	LSB	A_{IN}=15MHz
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	
Effective No. of bits	ENOB	+25°C	1	5.0	5.5	-	bits	A_{IN}=15MHz
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	A_{IN}=15MHz
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the ‘011111’ to ‘100000’B transition edge.

TEST LEVELS

Level 1 - 100% production tested.

Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.

Level 3 - Sample tested only.

Level 4 - Parameter is guaranteed by design and characterisation testing.

Level 5 - Parameter is typical value only.

PIN DESCRIPTIONS - 44 Pin J-lead PLCC package

Pin	Name	Description
1	AV_{CC} 1	Analog voltage supply for the 6-bit ADCs
2	AV_{CC} 1	Analog voltage supply for the 6-bit ADCs
3	AGND1	Analog ground
4	AGND1	Analog ground
5	AGND1	Analog ground
6	VRT	3.5V reference voltage - ladder top
7	VRM	Reference voltage - ladder middle
8	VRB	2.5V reference voltage - ladder bottom
9	AV_{CC}2	Analog voltage supply for the reference bias circuits
10	AGND2	Analog ground
11	COMP-I	Capacitor compensation - I channel
12	AIN-I	Analog signal input - I channel
13	AGND3	Analog ground for the I channel buffer amplifier
14	AV_{CC}3	Analog voltage supply for the I channel buffer amplifier
15	COMP-Q	Capacitor compensation - Q channel
16	AIN-Q	Analog signal input - Q channel
17	AGND4	Analog ground
18	AV_{CC}4	Analog voltage supply for the Q channel buffer amplifier
19	AGC	AGC control voltage
20	BIAS	Input bias voltage
21	TANK	Tank circuit connection
22	CLKSEL	Clock select - VCO or external clock
23	AV_{CC}5	Analog voltage supply for the VCO
24	AGND5	Analog ground
25	CLKIN	Clock input positive
26	N.C.	Not connected
27	CLKOUT	Clock output positive
28	N.C.	Not connected
29	DQ0	Digital TTL output - LSB -Q channel
30	DQ1	
31	DQ2	
32	DQ3	
33	DQ4	
34	DQ5	Digital TTL output - MSB - Q channel
35	DGND	Digital ground
36	DV_{CC}	Digital voltage supply
37	DI0	Digital TTL output - LSB - I channel
38	DI1	
39	DI2	
40	DI3	
41	DI4	
42	DI5	Digital TTL output - MSB - I channel
43	N.C.	Not connected
44	N.C.	Not connected

Table 1: Pin descriptions

An on-chip bandgap voltage reference circuit combined with two op amps provide all the necessary bias voltages

Device Description

The VP216 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL data outputs. The VP216 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC and has an optional VCO or external oscillator interface.

Analog Input

The analog inputs, (AIN_I,Q) are A.C. coupled into the non-inverting ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, (VRM = 3V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

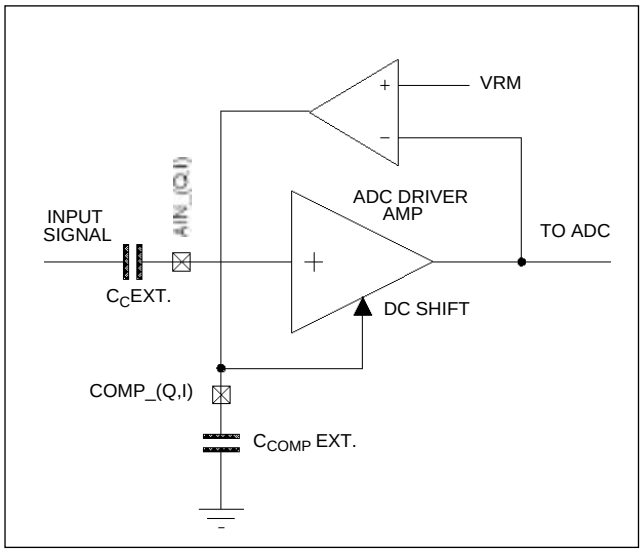


Fig.3 DC offset internal feedback loop.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, (VRB), (VRM) and (VRT). VRB, VRM and VRT have been brought out to pins 8, 7 and 6 respectively and should be decoupled with 100nF capacitors close to the package pins.

Digital Interface

The TTL data output pins, (DI0-DI5) and (DQ0-DQ5) have been optimized to interface with devices in close proximity to the VP216 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold timing. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The VP216 clock interface allows the ADC to be clocked in a number of ways. With the CLKSEL pin tied low the on chip VCO is selected. With the CLKSEL pin tied high the external TTL clock input is selected.

CLKSEL	Clock Source
1	External Clock
0	VCO

Table 2

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched after a rising edge of the input clock. Latched data is then presented to the TTL data outputs and latched on the falling edge of the input clock. The clock interface also provides a TTL clock output on pin 27. This output is limited to driving capacitive loads of 10pF. Output buffers are recommended for loads in excess of 10pF.

Code	Input Voltage 1 Volt Full Scale 16mV = 1LSB	Binary
00	Least +Ve Valid Input	000000
01	●	000001
●	●	●
31	●	011111
32	●	100000
33	●	100001
●	●	●
62	●	111110
63	Most +Ve Valid Input	111111

Table 3: Output coding

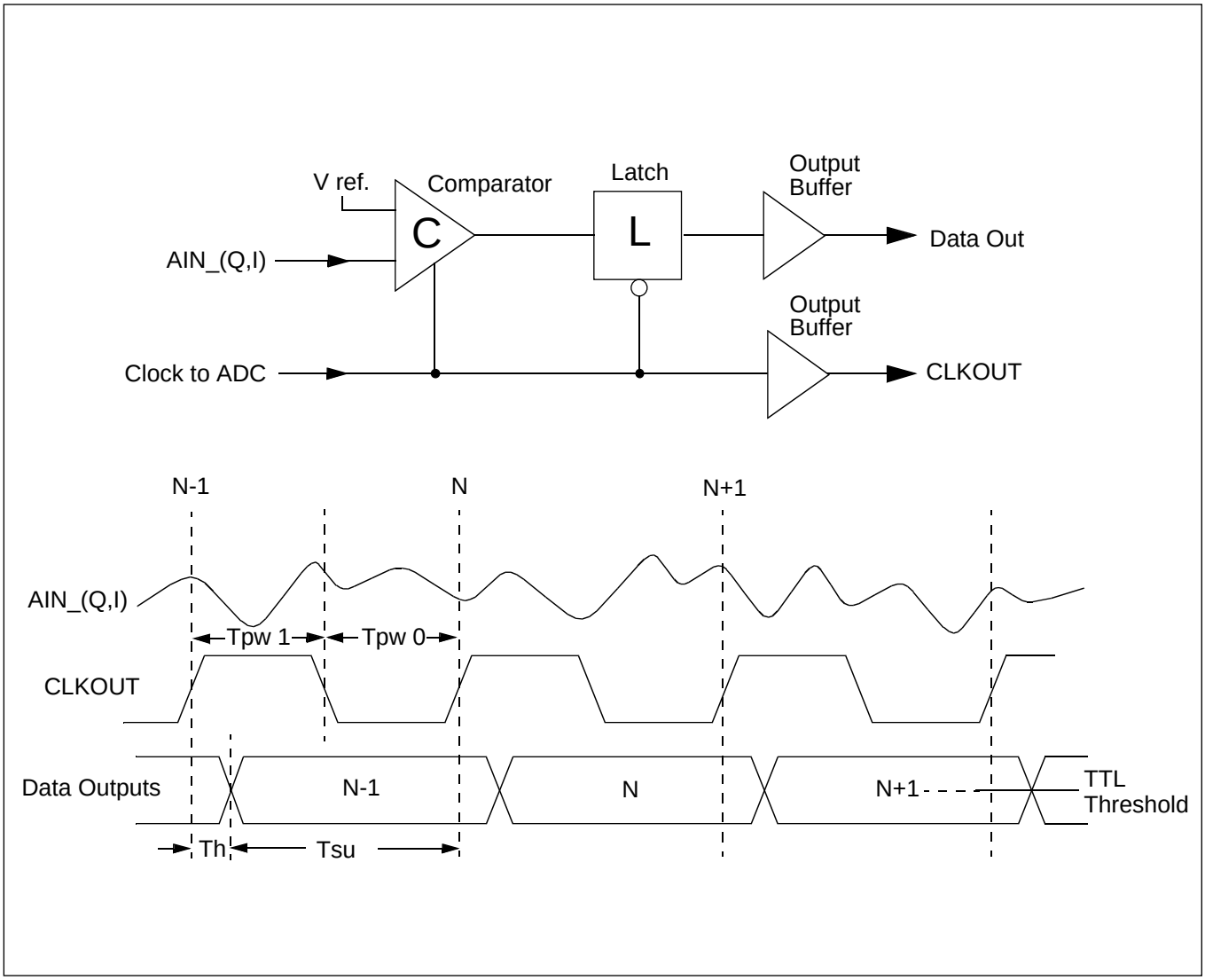


Fig.4 System timing diagram

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from 2.4V and 0.4V to the 1.4V threshold on the rising edge of the output clock.

Differential Non-linearity

The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 or

ENOB = N-log2[rms error (actual)/rms error (ideal)]

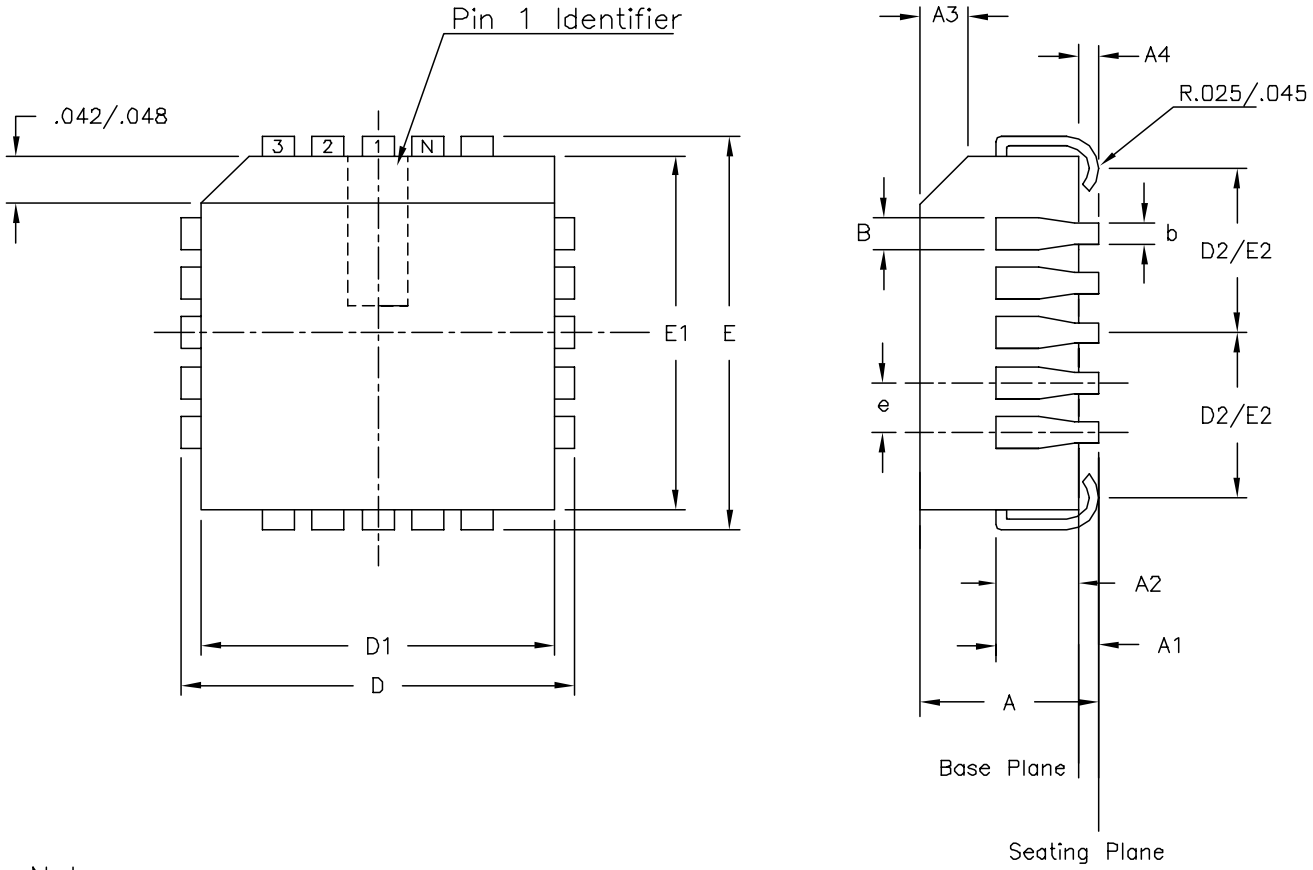
where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2				MITEL SEMICONDUCTOR
ACN	5958	207470				
DATE	15AUG94	10SEP99				
APPD.						

Title: Package Outline for 44 Lead PLCC

Drawing Number GPD00003

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