



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package		
			TO-92	TO-243AA*	Die†
-30V	0.6Ω	-4.0A	VP3203N3	VP3203N8	VP3203ND

\*Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

† MIL visual screening available.

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

#### Product marking for TO-243AA:

**VP2L\***

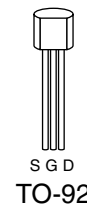
Where \* = 2-week alpha date code

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



Note: See Package Outline section for dimensions.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-92	-0.65A	-4.0A	0.74W	125	170	-0.65A	-4.0A
TO-243AA	-1.1A	-4.0A	1.6W <sup>†</sup>	15	78 <sup>†</sup>	-1.1A	-4.0A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

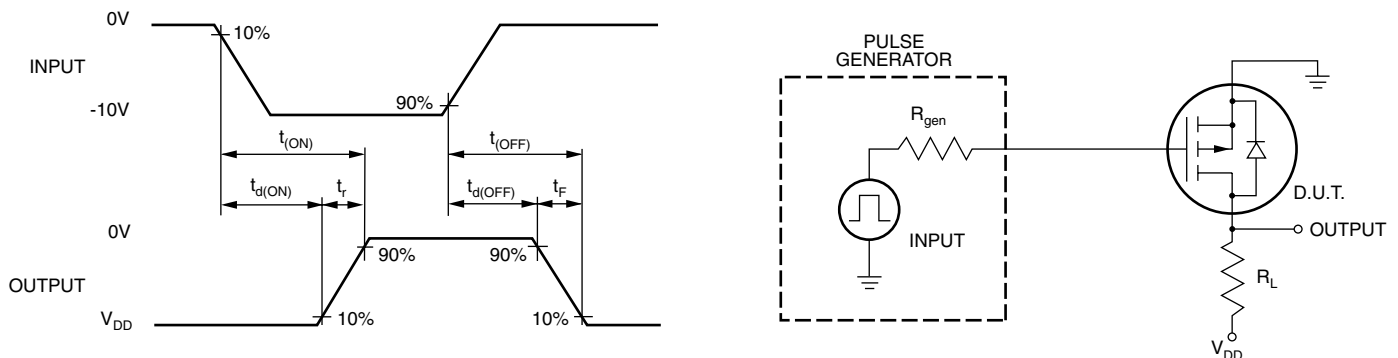
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-30			V	$V_{GS} = 0V, I_D = -10mA$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-3.5	V	$V_{GS} = V_{DS}, I_D = -10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -10mA$
$I_{GSS}$	Gate Body Leakage		-1.0	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			-10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-1	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-14		A	$V_{GS} = -10V, V_{DS} = -5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	TO-92		1.0	$\Omega$	$V_{GS} = -4.5V, I_D = -1.5A$
		SOT-89		1.0	$\Omega$	$V_{GS} = -4.5V, I_D = -0.75A$
		TO-92		0.6	$\Omega$	$V_{GS} = -10V, I_D = -3A$
		SOT-89		0.6	$\Omega$	$V_{GS} = -10V, I_D = -1.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -1.5A$
$G_{FS}$	Forward Transconductance	1.0	2.0		$\bar{\sigma}$	$V_{DS} = -25V, I_D = -2A$
$C_{ISS}$	Input Capacitance		200	300	pF	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		100	120		
$C_{RSS}$	Reverse Transfer Capacitance		45	60		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -25V$ $I_D = -2A$ $R_{GEN} = 10\Omega$
$t_r$	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			25		
$V_{SD}$	Diode Forward Voltage Drop			-1.6	V	$V_{GS} = 0V, I_{SD} = -1.5A$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -1A$

### Notes:

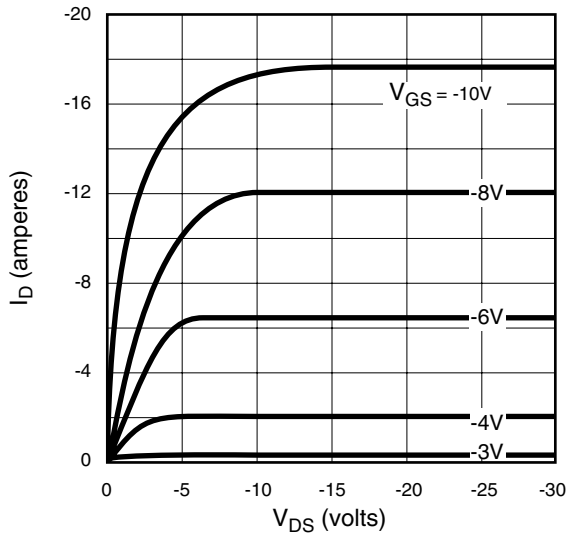
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

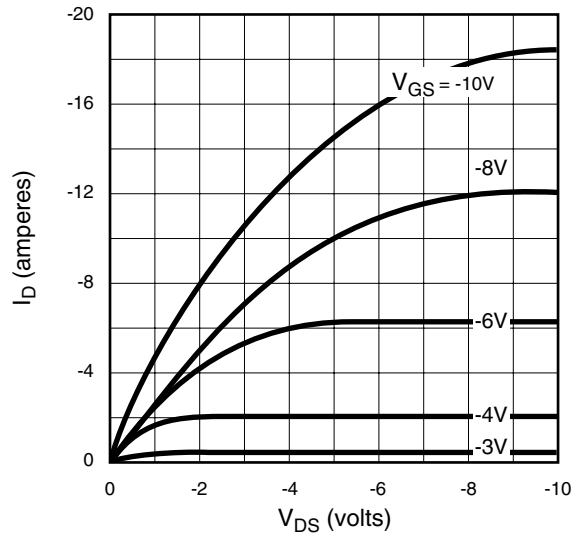


# Typical Performance Curves

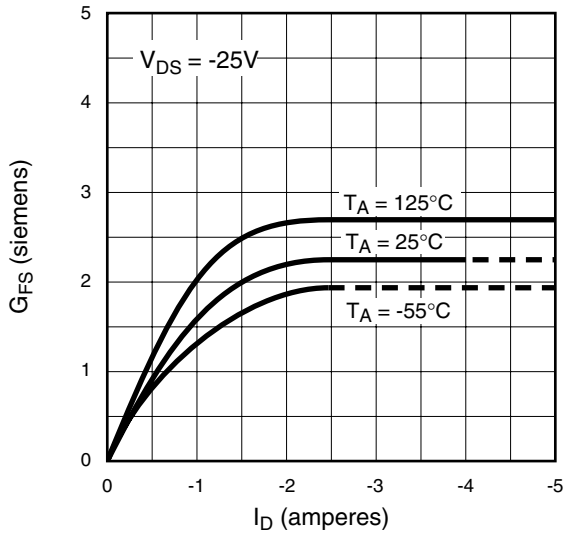
Output Characteristics



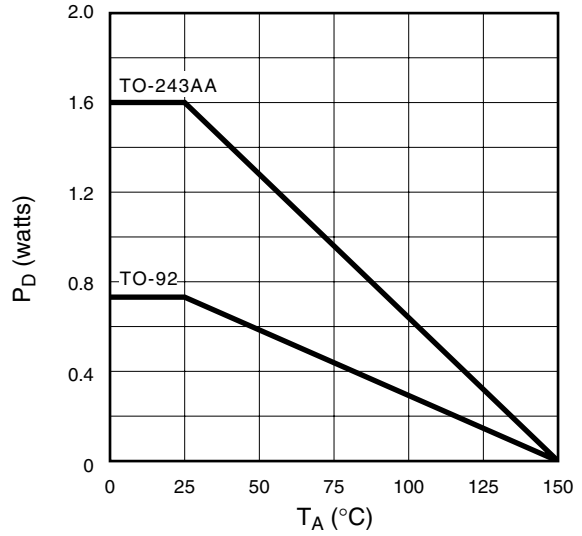
Saturation Characteristics



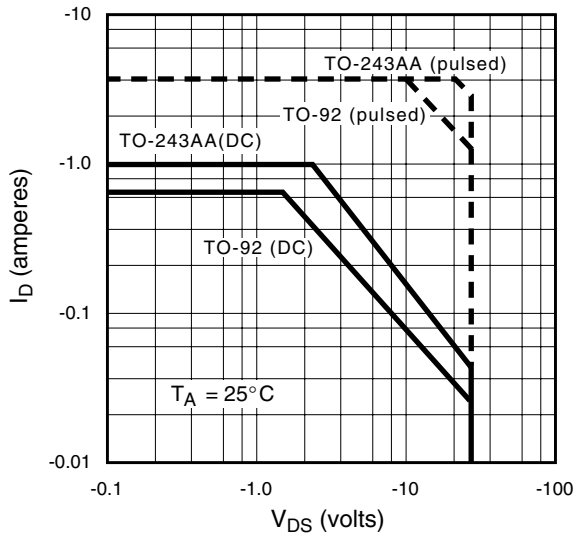
Transconductance vs. Drain Current



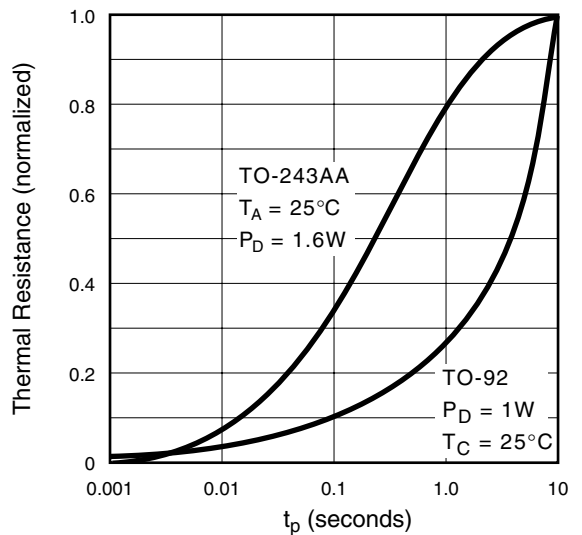
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

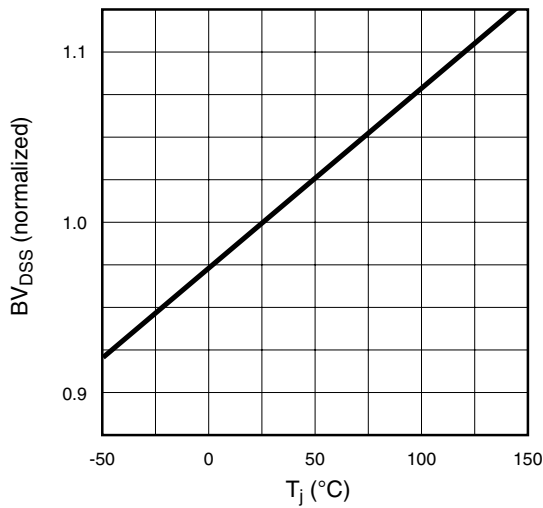


Thermal Response Characteristics

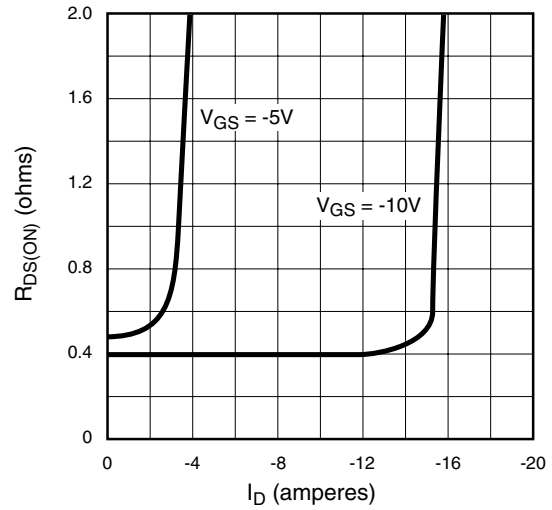


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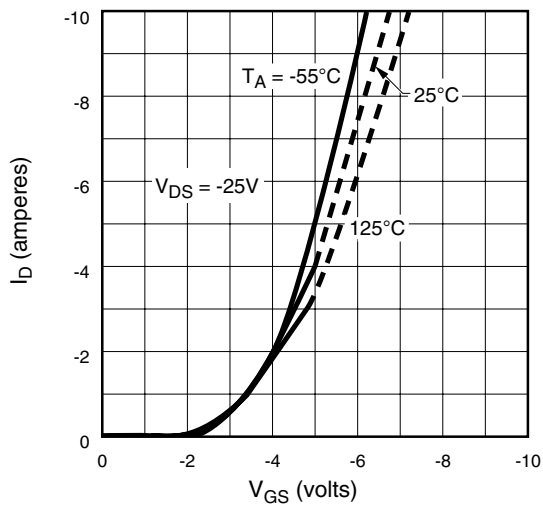
BV<sub>DSS</sub> Variation with Temperature



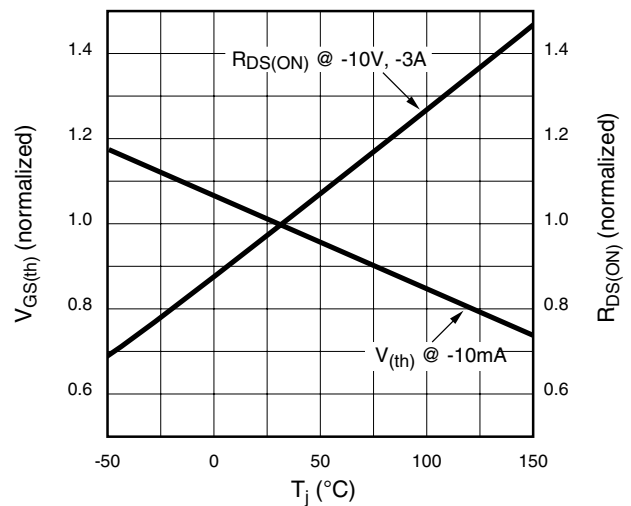
On-Resistance vs. Drain Current



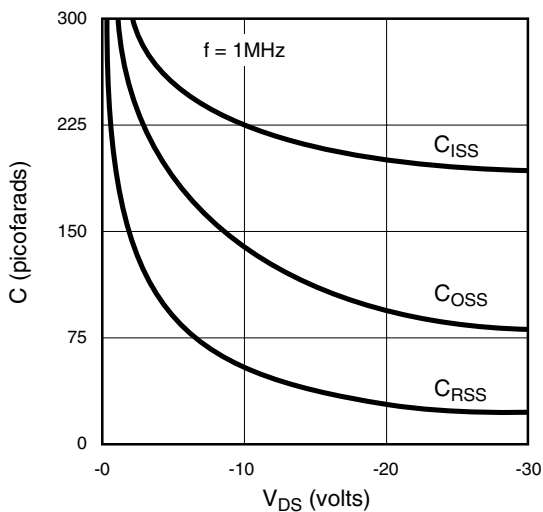
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

