# 512MB – 64Mx64 DDR SDRAM, UNBUFFERED, SO-DIMM

## FEATURES

- Fast data transfer rate: PC3200 & PC2700
- Clock speeds of 200MHz & 166MHz
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency : DDR400 (3 clock), DDR333 (2.5 clock)
- Programmable Burst Length (2, 4 or 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh, 7.8µs refresh interval (8K (64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Serial presence detect with EEPROM
- $V_{CC}$ = $V_{CCQ}$ = +2.5V ±0.2V (166MHz)
- $V_{CC}$ = $V_{CCQ}$ = +2.6V ±0.1V (200MHz)
- Gold edge contacts
- JEDEC standard 200 pin, small-outline, SO-DIMM package
  - PCB height option:
    D4: 31.75 mm (1.25") TYP

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

## DESCRIPTION

The WV3EG64M64ETSU is a 64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eight 64Mx8 DDR SDRAMs TSOP-II packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

### OPERATING FREQUENCIES

| | DDR400@CL=3 | DDR333@CL2.5 |
|---|---|---|
| Clock Speed | 200MHz | 166MHz |
| CL-$t_{RCD}$-$t_{RP}$ | 3-3-3 | 2.5-3-3 |

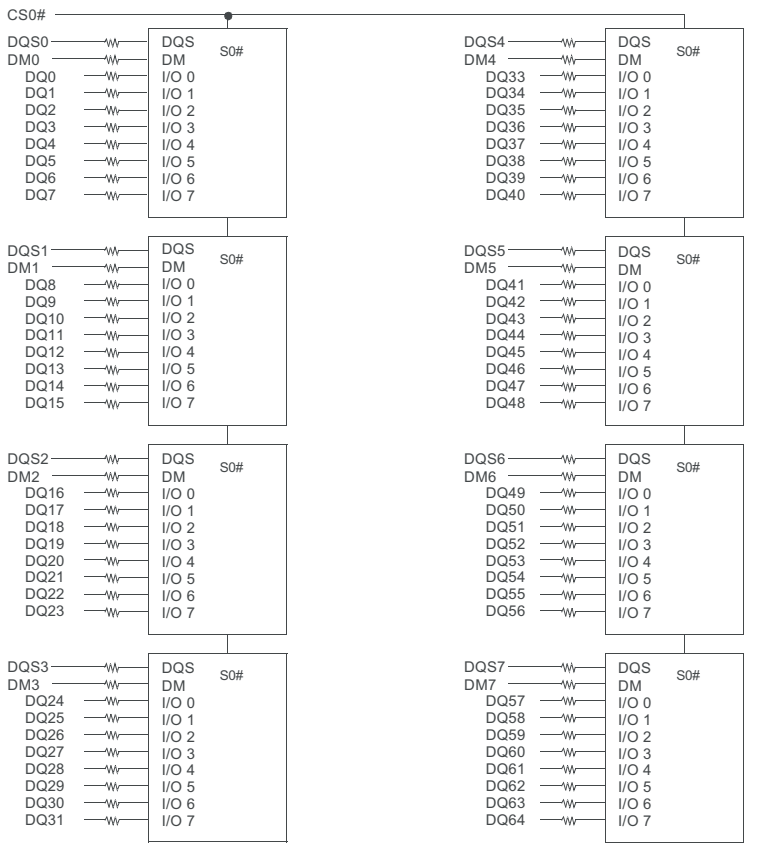
## PIN CONFIGURATION

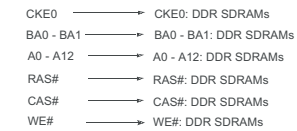
| PIN# | SYMBOL | PIN# | SYMBOL | PIN# | SYMBOL | PIN# | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 51 | $V_{SS}$ | 101 | A9 | 151 | DQ42 |
| 2 | $V_{REF}$ | 52 | $V_{SS}$ | 102 | A8 | 152 | DQ46 |
| 3 | $V_{SS}$ | 53 | DQ19 | 103 | $V_{SS}$ | 153 | DQ43 |
| 4 | $V_{SS}$ | 54 | DQ23 | 104 | $V_{SS}$ | 154 | DQ47 |
| 5 | DQ0 | 55 | DQ24 | 105 | A7 | 155 | $V_{CC}$ |
| 6 | DQ4 | 56 | DQ28 | 106 | A6 | 156 | $V_{CC}$ |
| 7 | DQ1 | 57 | $V_{CC}$ | 107 | A5 | 157 | $V_{CC}$ |
| 8 | DQ5 | 58 | $V_{CC}$ | 108 | A4 | 158 | CK1# |
| 9 | $V_{CC}$ | 59 | DQ25 | 109 | A3 | 159 | $V_{SS}$ |
| 10 | $V_{CC}$ | 60 | DQ29 | 110 | A2 | 160 | CK1 |
| 11 | DQS0 | 61 | DQS3 | 111 | A1 | 161 | $V_{SS}$ |
| 12 | DM0 | 62 | DM3 | 112 | A0 | 162 | $V_{SS}$ |
| 13 | DQ2 | 63 | $V_{SS}$ | 113 | $V_{CC}$ | 163 | DQ48 |
| 14 | DQ6 | 64 | $V_{SS}$ | 114 | $V_{CC}$ | 164 | DQ52 |
| 15 | $V_{SS}$ | 65 | DQ26 | 115 | A10 | 165 | DQ49 |
| 16 | $V_{SS}$ | 66 | DQ30 | 116 | BA1 | 166 | DQ53 |
| 17 | DQ3 | 67 | DQ27 | 117 | BA0 | 167 | $V_{CC}$ |
| 18 | DQ7 | 68 | DQ31 | 118 | RAS# | 168 | $V_{CC}$ |
| 19 | DQ8 | 69 | $V_{CC}$ | 119 | WE# | 169 | DQS6 |
| 20 | DQ12 | 70 | $V_{CC}$ | 120 | CAS# | 170 | DM6 |
| 21 | $V_{CC}$ | 71 | NC | 121 | CS0# | 171 | DQ50 |
| 22 | $V_{CC}$ | 72 | NC | 122 | NC | 172 | DQ54 |
| 23 | DQ9 | 73 | NC | 123 | NC | 173 | $V_{SS}$ |
| 24 | DQ13 | 74 | NC | 124 | NC | 174 | $V_{SS}$ |
| 25 | DQS1 | 75 | $V_{SS}$ | 125 | $V_{SS}$ | 175 | DQ51 |
| 26 | DM1 | 76 | $V_{SS}$ | 126 | $V_{SS}$ | 176 | DQ55 |
| 27 | $V_{SS}$ | 77 | NC | 127 | DQ32 | 177 | DQ56 |
| 28 | $V_{SS}$ | 78 | NC | 128 | DQ36 | 178 | DQ60 |
| 29 | DQ10 | 79 | NC | 129 | DQ33 | 179 | $V_{CC}$ |
| 30 | DQ14 | 80 | NC | 130 | DQ37 | 180 | $V_{CC}$ |
| 31 | DQ11 | 81 | $V_{CC}$ | 131 | $V_{CC}$ | 181 | DQ57 |
| 32 | DQ15 | 82 | $V_{CC}$ | 132 | $V_{CC}$ | 182 | DQ61 |
| 33 | $V_{CC}$ | 83 | NC | 133 | DQS4 | 183 | DQS7 |
| 34 | $V_{CC}$ | 84 | NC | 134 | DM4 | 184 | DM7 |
| 35 | CK0 | 85 | NC | 135 | DQ34 | 185 | $V_{SS}$ |
| 36 | $V_{CC}$ | 86 | NC | 136 | DQ38 | 186 | $V_{SS}$ |
| 37 | CK0# | 87 | $V_{SS}$ | 137 | $V_{SS}$ | 187 | DQ58 |
| 38 | $V_{SS}$ | 88 | $V_{SS}$ | 138 | $V_{SS}$ | 188 | DQ62 |
| 39 | $V_{SS}$ | 89 | NC | 139 | DQ35 | 189 | DQ59 |
| 40 | $V_{SS}$ | 90 | $V_{SS}$ | 140 | DQ39 | 190 | DQ63 |
| 41 | DQ16 | 91 | NC | 141 | DQ40 | 191 | $V_{CC}$ |
| 42 | DQ20 | 92 | $V_{CC}$ | 142 | DQ44 | 192 | $V_{CC}$ |
| 43 | DQ17 | 93 | $V_{CC}$ | 143 | $V_{CC}$ | 193 | SDA |
| 44 | DQ21 | 94 | $V_{CC}$ | 144 | $V_{CC}$ | 194 | SA0 |
| 45 | $V_{CC}$ | 95 | NC | 145 | DQ41 | 195 | SCL |
| 46 | $V_{CC}$ | 96 | CKE0 | 146 | DQ45 | 196 | SA1 |
| 47 | DQS2 | 97 | NC | 147 | DQS5 | 197 | $V_{CCSPD}$ |
| 48 | DM2 | 98 | NC | 148 | DM5 | 198 | SA2 |
| 49 | DQ18 | 99 | A12 | 149 | $V_{SS}$ | 199 | NC |
| 50 | DQ22 | 100 | A11 | 150 | $V_{SS}$ | 200 | NC |

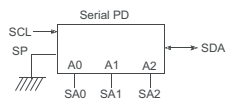
## PIN NAMES

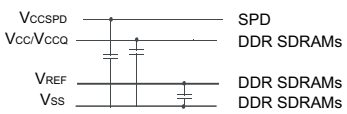
| Symbol | Description |
|---|---|
| A0-A12 | Address input |
| BA0, BA1 | Bank Address |
| DQ0-DQ63 | Input/Output: Data I/Os, Data bus |
| CK0, CK0#<br>CK1, CK1# | Clock Input |
| CKE0 | Clock Enable Input |
| CS0# | Chip Select Input |
| WE#, CAS#, RAS# | Command Input |
| DQS0-DQS7 | Data Strobe |
| DM0-DM7 | Data Write Mask |
| $V_{CC}$ | Supply: Power Supply |
| $V_{CCQ}$ | Power Supply for DQS |
| $V_{CCSPD}$ | Supply: Serial EEPROM Positive Power Supply |
| $V_{REF}$ | Supply: SSTL_2 reference voltage |
| $V_{SS}$ | Supply: Ground |
| SCL | Serial Clock |
| SA0-SA2 | Presence Detect Address Input |
| SDA | Input/Output: Serial Presence-Detect Data |
| NC | No Connect |

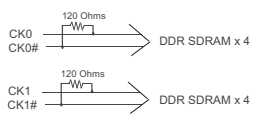
## FUNCTIONAL BLOCK DIAGRAM




Note: 1. All resistor values are 22Ω unless otherwise specified.

## DC OPERATING CONDITIONS

$T_A$ = 0°C to 70°C

| Parameter/Condition | | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage DDR400 (nominal VCC 2.6) | | $V_{CC}$ | 2.5 | 2.7 | V | |
| I/O Supply Voltage DDR400 (nominal VCC 2.6) | | $V_{CCQ}$ | 2.5 | 2.7 | V | |
| Supply Voltage DDR333 | | $V_{CC}$ | 2.3 | 2.7 | V | |
| I/O Supply Voltage DDR333 | | $V_{CCQ}$ | 2.3 | 2.7 | V | |
| I/O Reference Voltage | | $V_{REF}$ | 0.49 × $V_{CCQ}$ | 0.51 × $V_{CCQ}$ | V | 1 |
| I/O Termination Voltage (system) | | $V_{TT}$ | $V_{REF}$ - 0.04 | $V_{REF}$ + 0.04 | V | 2 |
| Input High (Logic 1) Voltage | | $V_{IH(DC)}$ | $V_{REF}$ + 0.15 | $V_{CC}$ + 0.30 | V | |
| Input Low (Logic 0) Voltage | | $V_{IL(DC)}$ | -0.3 | $V_{REF}$ - 0.15 | V | |
| Input voltage level, CK and CK# | | $V_{IN(DC)}$ | -0.3 | $V_{CCQ}$ + 0.30 | V | |
| Input differential voltage, CK and CK# | | $V_{ID(DC)}$ | -0.3 | $V_{CCQ}$ + 0.60 | V | 3 |
| Input crossing point voltage, CK and CK# | | $V_{IX(DC)}$ | -0.3 | $V_{CCQ}$ + 0.60 | V | |
| Input leakage current | Addr, CAS#, RAS#, WE# | $I_I$ | -16 | 16 | µA | |
| | CS#, CKE | | -16 | 16 | µA | |
| | CK, CK# | | -8 | 8 | µA | |
| | DM | | -2 | 2 | µA | |
| Output leakage current | | $I_{OZ}$ | -5 | 5 | µA | |
| Output high current (normal strength) $V_{OUT}$ = v + 0.84V | | $I_{OH}$ | -16.8 | — | mA | |
| Output high current (normal strength) $V_{OUT}$ = v - 0.84V | | $I_{OL}$ | -16.8 | — | mA | |
| Output high current (half strength) $V_{OUT}$ = $V_{TT}$ + 0.45V | | $V_{OH}$ | -9 | — | mA | |
| Output high current (half strength) $V_{OUT}$ = $V_{TT}$ - 0.45V | | $V_{OL}$ | 9 | — | mA | |

Notes:

1. $V_{REF}$ is expected to be equal to 0.5*$V_{CCQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on $V_{REF}$ may not exceed +/-2% of the DC values.
2. $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$, and must track variations in the DC level of $V_{REF}$.
3. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level of CK#.
4. Industrial grade modules are specified to a DRAM $t_{CASE}$ of 85°C and -40°C

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Voltage on any in relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 ~ 3.6 | V |
| Voltage on $V_{CC}$ & $V_{CCQ}$ supply relative to $V_{SS}$ | $V_{CC}$, $V_{CCQ}$ | -1.0 ~ 3.6 | V |
| Voltage on $V_{REF}$ supply relative to $V_{SS}$ | $V_{REF}$ | -1.0 ~ 3.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Operating temperature | $T_A$ | 0 ~ 70 | °C |
| Power dissipation | $P_D$ | 8 | W |
| Short circuit output current | $I_{OS}$ | 50 | mA |

Notes:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceed.
Functional operation should be restricted to recommended operating condition.
Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

## INPUT/OUTPUT CAPACITANCE

$T_A$ = 25°C, f = 100MHz

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input capacitance (A0 ~ A12, BA0 ~ BA1, RAS#, CAS# WE#) | $C_{IN1}$ | 20 | 28 | pF |
| Input capacitance (CKE0) | $C_{IN2}$ | 20 | 28 | pF |
| Input capacitance (CS0#) | $C_{IN3}$ | 20 | 28 | pF |
| Input capacitance (CK0, CK0#, CK1, CK1#) | $C_{IN4}$ | 12 | 16 | pF |
| Input capacitance (DM0 ~ DM7) | $C_{IN5}$ | 8 | 9 | pF |
| Input capacitance (DQ0 ~ DQ63), (DQS0 ~ DQS7) | $C_{OUT1}$ | 8 | 9 | pF |

Notes:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceed.
Functional operation should be restricted to recommended operating condition.
Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

## AC OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH(AC)}$ | $V_{REF}$ + 0.31 | | V |
| Input Low (Logic 0) Voltage | $V_{IL(AC)}$ | | $V_{REF}$ - 0.31 | V |
| Input Differential Voltage, CK and CK# inputs | $V_{ID(AC)}$ | 0.7 | $V_{CCQ}$ + 0.6 | V |
| Input crossing point voltage, CK and CK# input | $V_{IX(AC)}$ | 0.5*$V_{CCQ}$ - 0.2 | 0.5*$V_{CCQ}$ + 0.2 | V |

## $I_{CC}$ SPECIFICATIONS AND CONDITIONS

0°C ≤ $T_A$ ≤ +70°C DDR400: $V_{CC}$ = $V_{CCQ}$ = +2.6V ±0.1V

| Symbol | Parameter/Condition | Max DDR400 @CL=3 | Max DDR333 @CL=2.5 | Units |
|---|---|---|---|---|
| $I_{CC0}$ | OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC}$ = $t_{RC}$ (MIN); $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | 960 | 840 | mA |
| $I_{CC1}$ | OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; $t_{RC}$ = $t_{RC}$ (MIN); $t_{CK}$ = $t_{CK}$ (MIN); $I_{OUT}$ = 0mA; Address and control inputs changing once per clock cycle | 1,200 | 1,080 | mA |
| $I_{CC2P}$ | PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK}$ = $t_{CK}$ (MIN); CKE = (LOW) | 40 | 40 | mA |
| $I_{CC2F}$ | IDLE STANDBY CURRENT: CS# = HIGH; All device banks are idle; $t_{CK}$ = $t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}$ = $V_{REF}$ for DQ, DQS, and DM | 240 | 240 | mA |
| $I_{CC3P}$ | ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK}$ = $t_{CK}$ (MIN); CKE = LOW | 360 | 200 | mA |
| $I_{CC3N}$ | ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC}$ = $t_{RAS}$ (MAX); $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | 480 | 360 | mA |
| $I_{CC4R}$ | OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK}$ (MIN); $I_{OUT}$ = 0mA | 1,240 | 1,120 | mA |
| $I_{CC4W}$ | OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | 1,400 | 1,200 | mA |
| $I_{CC5}$ | AUTO REFRESH BURST CURRENT: $t_{REFC}$ = $t_{RFC}$ (MIN) | 1,760 | 1,640 | mA |
| $I_{CC6}$ | SELF REFRESH CURRENT: CKE ≤ 0.2V | 40 | 40 | mA |
| $I_{CC7}$ | OPERATING CURRENT: Four device bank interleaving READs (Burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK}$ = $t_{CK}$ (MIN); Address and control inputs change only during Active READ, or WRITE commands | 3,080 | 2,880 | mA |

Notes:

$I_{CC}$ parameters are based on **SAMSUNG** components. Other DRAM manufactures parameter may be different

## $I_{CC}$ SPECIFICATIONS AND CONDITIONS

0°C ≤ $T_A$ ≤ +70°C, DDR400: $V_{CC}$ = $V_{CCQ}$ = +2.6V ±0.1V

| Symbol | Parameter/Condition | Max DDR400 @CL=3 | Max DDR333 @CL=2.5 | Units |
|---|---|---|---|---|
| $I_{CC0}$ | OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC}$ = $t_{RC}$ (MIN); $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | TBD | 1,040 | mA |
| $I_{CC1}$ | OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; $t_{RC}$ = $t_{RC}$ (MIN); $t_{CK}$ = $t_{CK}$ (MIN); $I_{OUT}$ = 0mA; Address and control inputs changing once per clock cycle | TBD | 1,280 | mA |
| $I_{CC2P}$ | PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK}$ = $t_{CK}$ (MIN); CKE = (LOW) | TBD | 40 | mA |
| $I_{CC2F}$ | IDLE STANDBY CURRENT: CS# = HIGH; All device banks are idle; $t_{CK}$ = $t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}$ = $V_{REF}$ for DQ, DQS, and DM | TBD | 360 | mA |
| $I_{CC3P}$ | ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK}$ = $t_{CK}$ (MIN); CKE = LOW | TBD | 280 | mA |
| $I_{CC3N}$ | ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC}$ = $t_{RAS}$ (MAX); $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | TBD | 400 | mA |
| $I_{CC4R}$ | OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK}$ (MIN); $I_{OUT}$ = 0mA | TBD | 1,320 | mA |
| $I_{CC4W}$ | OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | TBD | 1,400 | mA |
| $I_{CC5}$ | AUTO REFRESH BURST CURRENT: $t_{REFC}$ = $t_{RFC}$ (MIN) | TBD | 2,320 | mA |
| $I_{CC6}$ | SELF REFRESH CURRENT: CKE ≤ 0.2V | TBD | 40 | mA |
| $I_{CC7}$ | OPERATING CURRENT: Four device bank interleaving READs (Burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK}$ = $t_{CK}$ (MIN); Address and control inputs change only during Active READ, or WRITE commands | TBD | 3,240 | mA |

Notes:

$I_{CC}$ parameters are based on **MICRON** components. Other DRAM manufactures parameter may be different

## DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

$0°C \leq T_A \leq +70°C$;

| AC Characteristics | | | 403 | | 335 | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Units** |
| Row Cycle Time | | $t_{RC}$ | 55 | | 60 | | $t_{CK}$ |
| Refresh row cycle time | | $t_{RFC}$ | 70 | | 72 | | ps |
| Row active | | $t_{RAS}$ | 40 | 70K | 42 | 70K | ps |
| RAS# to CAS# delay | | $t_{RCD}$ | 15 | | 18 | | $t_{CK}$ |
| Row percharge time | | $t_{RP}$ | 15 | | 18 | | ns |
| Row active to row active delay | | $t_{RRD}$ | 10 | | 12 | | ns |
| Write recovery time | | $t_{WR}$ | 15 | | 15 | | ns |
| Last data in to READ command | | $t_{WTR}$ | 2 | | 1 | | ns |
| Clock cycle time | CL = 2.5 | $t_{CK}$ | 6 | 12 | 6 | 12 | ns |
| | CL = 3 | | 5 | 10 | | | ns |
| CK high-level width | | $t_{CH}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ |
| CK low-level width | | $t_{CL}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ |
| Access window of DQS from CK/CK# | | $t_{DQSCK}$ | -0.55 | +0.55 | -0.6 | +0.6 | ns |
| Access window of DQs from CK/CK# | | $t_{AC}$ | -0.65 | +0.65 | -0.7 | +0.7 | ns |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | | $t_{DQSQ}$ | - | 0.4 | - | 0.4 | ns |
| Read preamble | | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ |
| Read postamble | | $t_{RPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ |
| CK to valid DQS-in | | $t_{DQSS}$ | 0.72 | 1.28 | 0.75 | 1.25 | $t_{CK}$ |
| DQS-in setup time | | $t_{WPRES}$ | 0 | | 0 | | ns |
| DQS-in hold time | | $t_{WPRE}$ | 0.25 | | 0.25 | | $t_{CK}$ |
| DQS falling edge to CK rising-setup time | | $t_{DSS}$ | 0.2 | | 0.2 | | $t_{CK}$ |
| DQS falling edge to CK rising-hold time | | $t_{DSH}$ | 0.2 | | 0.2 | | $t_{CK}$ |

Notes:

Industrial grade modules are specified to a DRAM $t_{CASE}$ of 85°C and -40°C

Continued on next page

## DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

$0°C \leq T_A \leq +70°C$

| AC Characteristics | | 403 | | 335 | | Units |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | |
| DQS-in high level width | $t_{DQSH}$ | 0.35 | | 0.35 | | $t_{CK}$ |
| DQS-in low level width | $t_{DQSL}$ | 0.35 | | 0.35 | | $t_{CK}$ |
| Address and control input setup time (fast) | $t_{ISF}$ | 0.6 | | 0.75 | | ns |
| Address and control input hold time (fast) | $t_{IHF}$ | 0.6 | | 0.75 | | ns |
| Address and control input setup time (slow) | $t_{ISs}$ | 0.7 | | 0.8 | | ns |
| Address and control input hold time (slow) | $t_{IHS}$ | 0.7 | | 0.8 | | ns |
| Data-out high-impedance time from CK/CK# | $t_{HZ}$ | | +0.65 | | +0.70 | ns |
| Data-out low-impedance time from CK/CK# | $t_{LZ}$ | -0.65 | | -0.70 | | ns |
| Mode register set cycle | $t_{MRD}$ | 10 | | 12 | | ns |
| DQ and DM input setup time to DQS | $t_{DS}$ | 0.4 | | 0.45 | | ns |
| DQ and DM input hold time to DQS | $t_{DH}$ | 0.4 | | 0.45 | | ns |
| Control & address input pulse width | $t_{IPW}$ | 2.2 | | 2.2 | | ns |
| DQ & DM input pulse width | $t_{DIPW}$ | 1.75 | | 1.75 | | ns |
| Exit self refresh to non-Read command | $t_{XSNR}$ | 75 | | 75 | | ns |
| Exit self refresh to Read command | $t_{XSRD}$ | 200 | | 200 | | $t_{CK}$ |
| Refresh interval time | $t_{REFI}$ | | 7.8 | | 7.8 | µs |
| Output DQS valid window | $t_{QH}$ | $t_{HP} - t_{QHS}$ | | $t_{HP} - t_{QHS}$ | | ns |
| Clock Half period | $t_{HP}$ | $t_{CL(MIN)}$ or $t_{CH(MAX)}$ | | $t_{CL(MIN)}$ or $t_{CH(MAX)}$ | | ns |
| Data hold skew factor | $t_{QHS}$ | | 0.5 | | 0.5 | ns |
| DQS write postable | $t_{WPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | ns |
| Active read with auto precharge command | $t_{RAP}$ | 15 | | 18 | | ns |
| Auto precharge write recovery + precharge time | $t_{DAL}$ | $t_{WR}/t_{CK}$ + $t_{RP}/t_{CK}$ | | $t_{WR}/t_{CK}$ + $t_{RP}/t_{CK}$ | | $t_{CK}$ |

Notes:

Industrial grade modules are specified to a DRAM $t_{CASE}$ of 85°C and -40°C

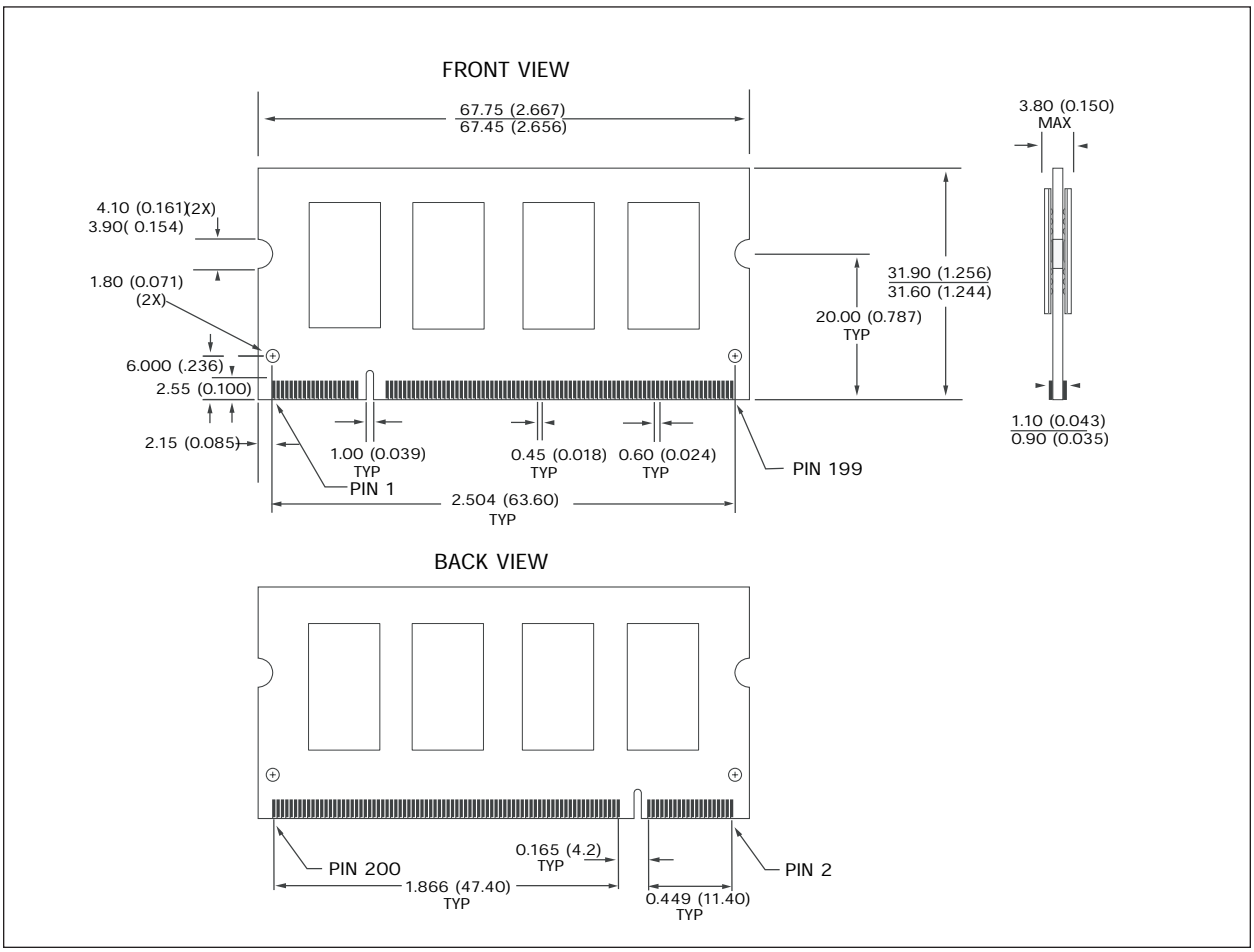
## ORDERING INFORMATION FOR D4

| Part Number | Speed | CAS Latency | $t_{RCD}$ | $t_{RP}$ | Height* |
|---|---|---|---|---|---|
| WV3EG64M64ETSU403D4xxG | 200MHz/400Mbps | 3 | 3 | 3 | 31.75 (1.25") TYP |
| WV3EG64M64ETSU335D4xxG | 166MHz/333Mbps | 2.5 | 3 | 3 | 31.75 (1.25") TYP |

NOTES:

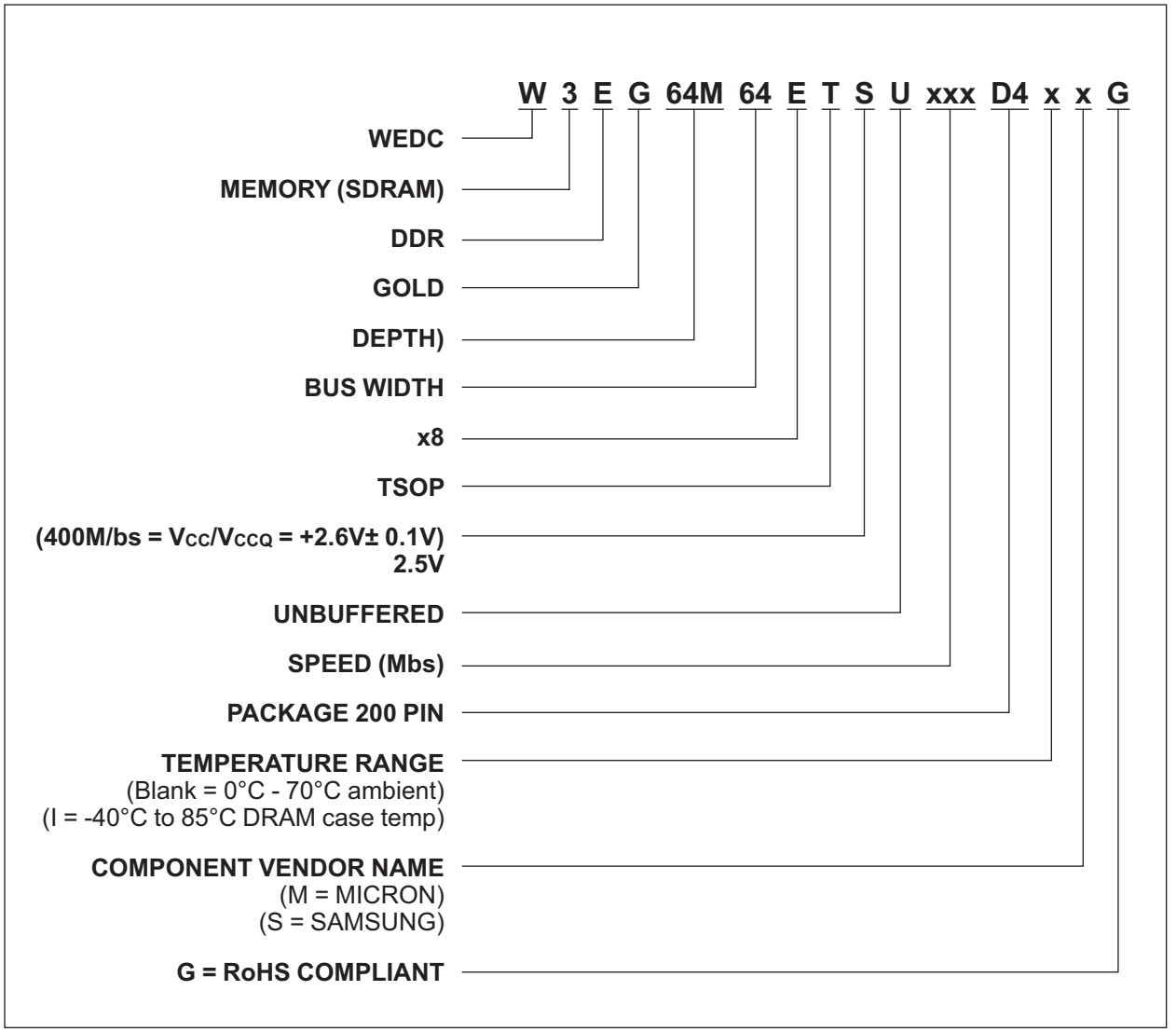
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "-x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

## 200-PIN DDR2 SO-DIMM DIMENSIONS




* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

## PART NUMBERING GUIDE



## Document Title

512MB - 64Mx64 DDR SDRAM, UNBUFFERED SO-DIMM

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Created | 3-06 | Preliminary |