PRELIMINARY

W48C111-16

Frequency Generator for Integrated Core Logic

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Power-on default to spread mode**
- **Two copies of CPU output**
- **Six copies of PCI output (synchronous w/CPU outputs)**
- **One copy of 48-MHz USB output**
- **One Buffered copy of 14.318-MHz input reference signal**
- **Supports 100-MHz or 66-MHz CPU operation**
- **Power management control input pins**
- **Low Frequency Test Mode**
- **Available in 28-pin SSOP (209 mil)**

Key Specifications

Supply Voltages: ..... V_{DDQ3} = 3.3V±5%
V_{DDQ2} = 2.5V±5%

CPU0:1 Skew: ..... 175 ps

CPU0:1 Cycle to Cycle Jitter: ..... 200 ps

PCI_F, PCI1:5 Skew: ..... 500 ps

PCI_F, PCI1:5 Cycle to Cycle Jitter: ..... 250 ps

CPU to PCI Skew: ..... 1.5 to 4.0 ns (CPU Leads)

Output Duty Cycle: 45/55%

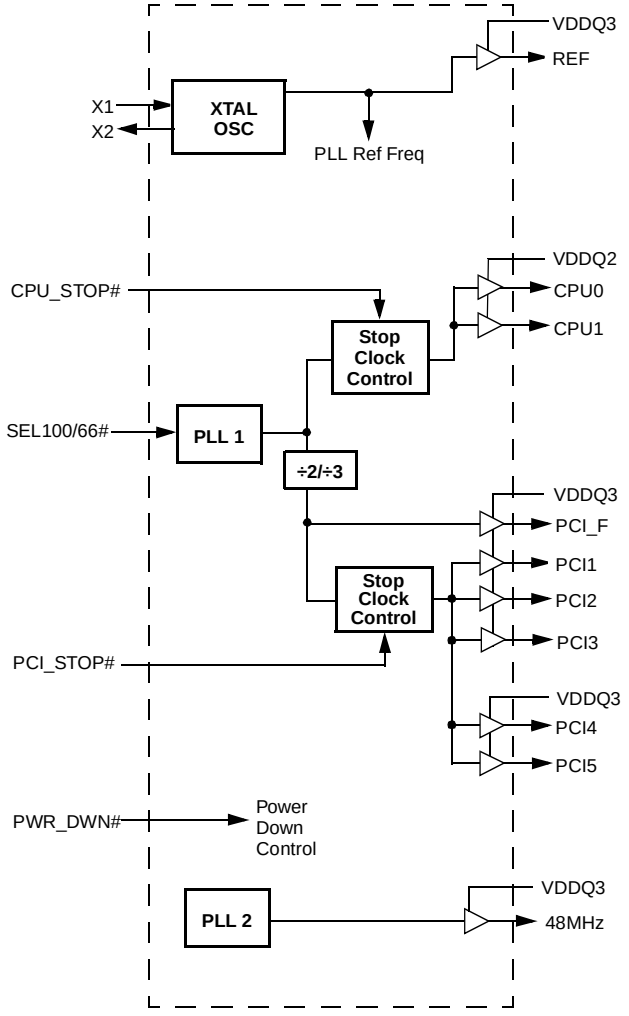
PCI_F, PCI Edge Rate: ..... ≥1 V/ns

CPU_STOP#, PWR_DWN#, PCI_STOP#: 250-kΩ pull-up resistor

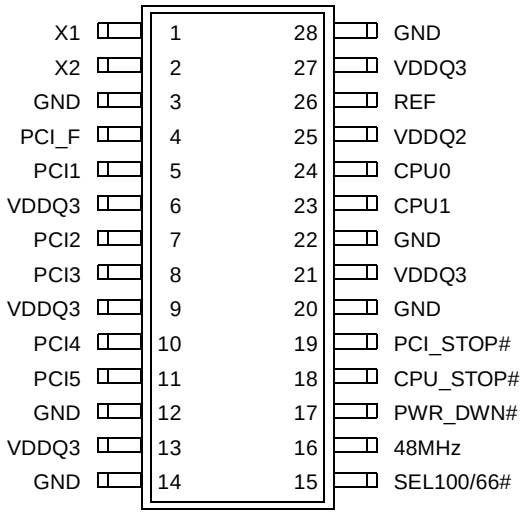
Table 1. Pin Selectable Frequency

SEL100/66#	CPU(0:1)	PCI	Spread%
0	66.6 MHz	33.3	±0.5%
1	100 MHz	33.3	±0.5%

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	24, 23	O	***CPU Clock Outputs 0 and 1:*** These two CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI1:5	5, 7, 8, 10, 11	O	***PCI Bus Clock Outputs 1 through 5:*** These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	4	O	***Fixed PCI Clock Output:*** Unlike PCI1:5 outputs, this output is not controlled by the PCI_STOP# control pin; it cannot be forced LOW by PCI_STOP#. Output voltage swing is controlled by voltage applied to VDDQ3.
48MHz	16	O	***48-MHz Output:*** Fixed clock output at 48 MHz. Output voltage swing is controlled by voltage applied to VDDQ3. This output does not have the SS feature
CPU_STOP#	18	I	***CPU_STOP# input:*** When brought LOW, clock outputs CPU0:1 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:1 start with a full clock cycle (2–3 CPU clock latency).
PCI_STOP#	19	I	***PCI_STOP# input:*** The PCI_STOP# input enables the PCI1:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effect takes place on the next PCI_F clock cycle.
REF	26	O	***Fixed 14.318-MHz Output:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
SEL100/66#	15	I	***Frequency Selection Inputs:*** Select power-up default CPU clock frequency as shown in *Table 1* on page 1.
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** This pin can either be used as a connection to a crystal or to a reference signal.
X2	2	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	17	I	***Power-Down Control:*** When this input is LOW, device goes into a low-power stand-by condition. All outputs are held LOW. CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought HIGH, CPU and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
VDDQ3	6, 9, 13, 21, 27	P	***Power Connection:*** Connected to 3.3V supply.
VDDQ2	25	P	***Power Connection:*** Power supply for CPU0:1 output buffer. Connected to 2.5V or 3.3V.
GND	3, 12, 14, 20, 22, 28	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Spread Spectrum Feature

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.5% of the center frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is always active on this device.

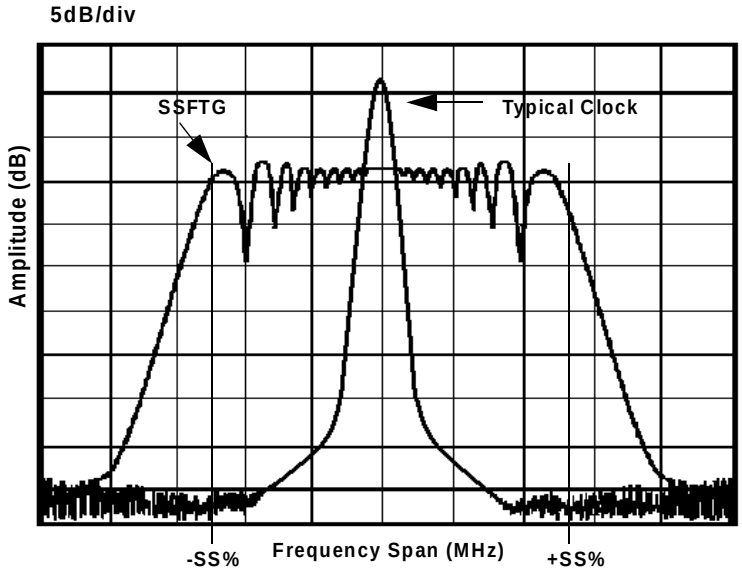


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

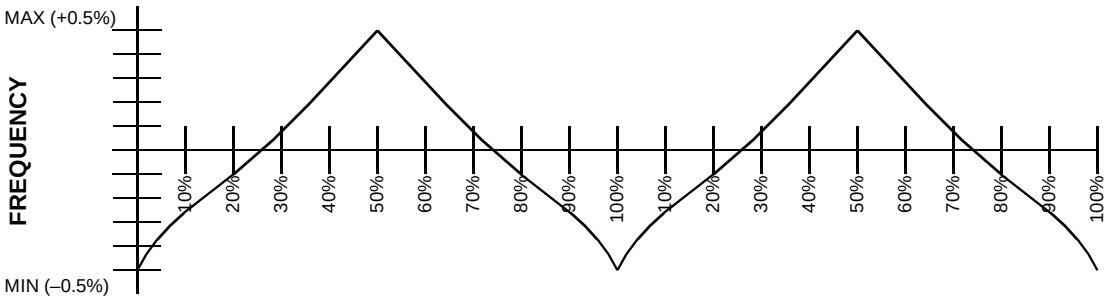


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%, CPU0:1 = 66.6/100 MHz

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD3}	Combined 3.3V Supply Current		Outputs Loaded[1]			80	mA
I_{DD2}	2.5V Supply Current					40	mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[2]					–25	µA
I_{IH}	Input High Current[2]					10	µA
I_{IL}	Input Low Current (SEL100/66#)					–5	µA
I_{IH}	Input High Current (SEL100/66#)					5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:1	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU0:1	V_{OL} = 1.25V	55	115	190	mA
		PCI_F, PCI1:5	V_{OL} = 1.5V	20.5	53	139	mA
		REF	V_{OL} = 1.5V	25	37	76	mA
I_{OH}	Output High Current	CPU0:1	V_{OL} = 1.25V	50	110	195	mA
		PCI_F, PCI1:5	V_{OL} = 1.5V	31	55	189	mA
		REFX	V_{OL} = 1.5V	27	44	94	mA
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[3]		V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, as seen by External Crystal[4]				14		pF
$C_{IN,X1}$	X1 Input Capacitance[5]		Pin X2 unconnected		28		pF
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance		Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance					6	pF
L_{IN}	Input Pin Inductance					7	nH

Notes:

1. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
2. CPU_STOP#, PCI_STOP#, and PWRDWN# logic inputs have internal pull-up resistors (pull-ups not CMOS level).
3. X1 input threshold voltage (typical) is V_{DDQ3}/2.
4. The W48C111-16 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%,V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
t_R	Output Rise Time	Measured from 0.4V to 2.0V	0.4		1.6	0.4		1.6	V/ns
t_F	Output Fall Time	Measured from 2.0V to 0.4V	0.4		1.6	0.4		1.6	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		13.5			13.5		Ω

PCI Clock Outputs, PCI1:5 and PCI_F (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

REF Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle to Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle to Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

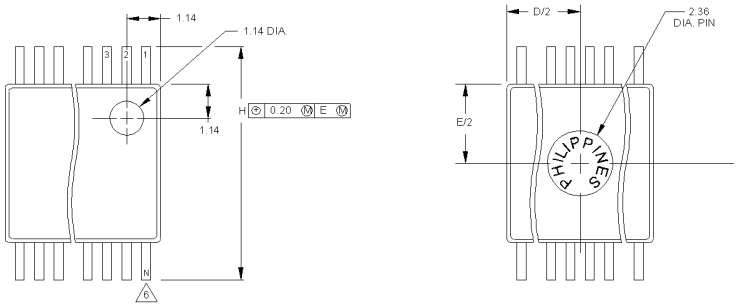
Ordering Information

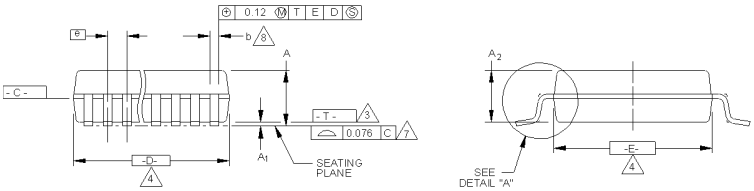
Ordering Code	Freq. Mask Code	Package Name	Package Type
W48C111	-16	H	28-pin SSOP (209 mils)

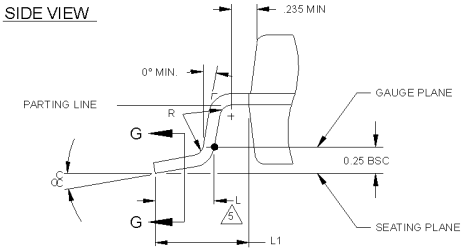
Document #: 38-00844

Package Diagram

28-Pin Small Shrink Outline Package (SSOP, 209 mils)







NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A1	.002	.005	.008		AB	.239	.244	.249	16
A2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	.004	.006							