Winbond Electronics Corp.

200MHZ CLOCK FOR CAMINO CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-97 is a Clock Synthesizer for Intel Camino 820 chipset. W83194BR-97 provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 sets of different frequencies of CPU, PCI, 3V66, IOAPIC clocks or stepless frequecies programming by M/N value via I^2C registers. All clocks are externally selectable with smooth transitions.

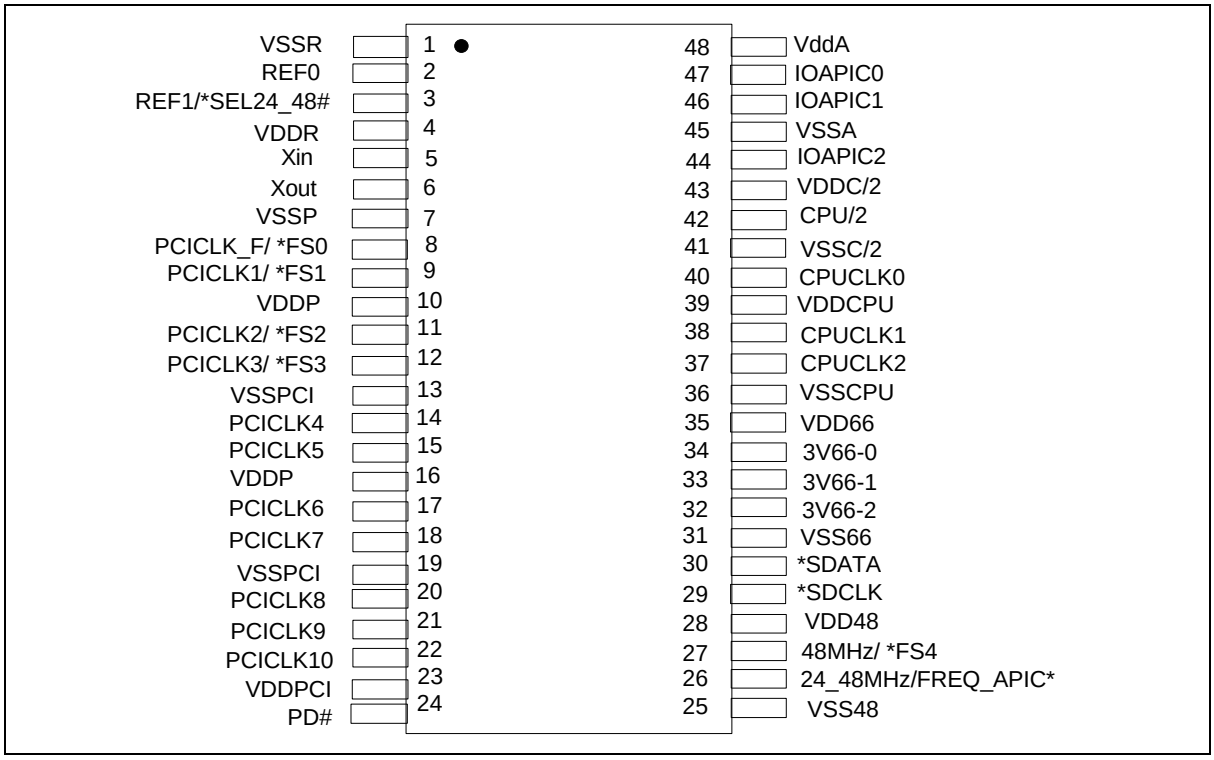
The W83194BR-97 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.5% and 0.25% center type spread spectrum to reduce EMI.

The W83194BR-97 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clock outputs
- One CPU/2 output as reference input to DRCG
- 3 3V66 clock outputs
- 3 IOAPIC clock outputs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VddQ2 = VddQ3 = 3.3V or VddQ3=3.3V, VddQ2=2.5V)
- CPU to 3V66 offset 0 to 1.5 ns
- 3V66 to PCI offset 1.5 to 4.0 ns
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- Stepless programmable frequencies by I^2C register9 ~ register12
- I^2C 2-Wire serial interface and I^2C read back
- 0.5% and 0.75% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz pins for USB
- 24 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION



4.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	CPU/2	3V66/ CPU	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz) FREQ_APIC=1	IOAPIC (MHz) FREQ_APIC=0
0	0	0	0	0	103.00	51.50	0.67	68.67	34.33	17.17	34.33
0	0	0	0	1	105.00	52.50	0.67	70.00	35.00	17.50	35.00
0	0	0	1	0	100.30	50.15	0.67	66.87	33.43	16.72	33.43
0	0	0	1	1	100.90	50.45	0.67	67.27	33.63	16.82	33.63
0	0	1	0	0	107.00	53.50	0.67	71.33	35.67	17.83	35.67
0	0	1	0	1	109.00	54.50	0.67	72.67	36.33	18.17	36.33
0	0	1	1	0	112.00	56.00	0.67	74.67	37.33	18.67	37.33
0	0	1	1	1	114.00	57.00	0.67	76.00	38.00	19.00	38.00
0	1	0	0	0	116.10	58.05	0.67	77.40	38.70	19.35	38.70
0	1	0	0	1	118.00	59.00	0.67	78.67	39.33	19.67	39.33
0	1	0	1	0	133.30	66.65	0.50	66.65	33.33	16.66	33.33
0	1	0	1	1	120.00	60.00	0.67	80.00	40.00	20.00	40.00
0	1	1	0	0	122.00	61.00	0.67	81.33	40.67	20.33	40.67
0	1	1	0	1	125.10	62.55	0.67	83.40	41.70	20.85	41.70
0	1	1	1	0	128.20	64.10	0.67	85.47	42.73	21.37	42.73
0	1	1	1	1	130.00	65.00	0.67	86.67	43.33	21.67	43.33
1	**0**	**0**	**0**	**0**	**133.00**	**66.50**	**0.67**	**88.67**	**44.33**	**22.17**	44.33
1	0	0	0	1	133.90	66.95	0.50	66.95	33.48	16.74	33.48
1	0	0	1	0	138.00	69.00	0.50	69.00	34.50	17.25	34.50
1	0	0	1	1	142.00	71.00	0.50	71.00	35.50	17.75	35.50
1	0	1	0	0	146.00	73.00	0.50	73.00	36.50	18.25	36.50
1	0	1	0	1	150.00	75.00	0.50	75.00	37.50	18.75	37.50
1	0	1	1	0	153.00	76.50	0.50	76.50	38.25	19.13	38.25
1	0	1	1	1	156.00	78.00	0.50	78.00	39.00	19.50	39.00
1	1	0	0	0	159.10	79.55	0.50	79.55	39.78	19.89	39.78
1	1	0	0	1	162.00	81.00	0.50	81.00	40.50	20.25	40.50
1	1	0	1	0	165.00	82.50	0.50	82.50	41.25	20.63	41.25
1	1	0	1	1	168.00	84.00	0.50	84.00	42.00	21.00	42.00
1	1	1	0	0	171.00	85.50	0.50	85.50	42.75	21.38	42.75
1	1	1	0	1	174.00	87.00	0.50	87.00	43.50	21.75	43.50
1	1	1	1	0	177.00	88.50	0.50	88.50	44.25	22.13	44.25
1	1	1	1	1	180.00	90.00	0.50	90.00	45.00	22.50	45.00

5.0 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency Selection BY I2C

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	CPU/2	3V66/ CPU	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz) FREQ_APIC=1	IOAPIC (MHz) FREQ_APIC=0
0	0	0	0	0	0	103.00	51.50	0.67	68.67	34.33	17.17	34.33
0	0	0	0	0	1	105.00	52.50	0.67	70.00	35.00	17.50	35.00
0	0	0	0	1	0	100.30	50.15	0.67	66.87	33.43	16.72	33.43
0	0	0	0	1	1	100.90	50.45	0.67	67.27	33.63	16.82	33.63
0	0	0	1	0	0	107.00	53.50	0.67	71.33	35.67	17.83	35.67
0	0	0	1	0	1	109.00	54.50	0.67	72.67	36.33	18.17	36.33
0	0	0	1	1	0	112.00	56.00	0.67	74.67	37.33	18.67	37.33
0	0	0	1	1	1	114.00	57.00	0.67	76.00	38.00	19.00	38.00
0	0	1	0	0	0	116.10	58.05	0.67	77.40	38.70	19.35	38.70
0	0	1	0	0	1	118.00	59.00	0.67	78.67	39.33	19.67	39.33
0	0	1	0	1	0	133.30	66.65	0.50	66.65	33.33	16.66	33.33
0	0	1	0	1	1	120.00	60.00	0.67	80.00	40.00	20.00	40.00
0	0	1	1	0	0	122.00	61.00	0.67	81.33	40.67	20.33	40.67
0	0	1	1	0	1	125.10	62.55	0.67	83.40	41.70	20.85	41.70
0	0	1	1	1	0	128.20	64.10	0.67	85.47	42.73	21.37	42.73
0	0	1	1	1	1	130.00	65.00	0.67	86.67	43.33	21.67	43.33
0	**1**	**0**	**0**	**0**	**0**	**133.00**	**66.50**	**0.67**	**88.67**	**44.33**	**22.17**	44.33
0	1	0	0	0	1	133.90	66.95	0.50	66.95	33.48	16.74	33.48
0	1	0	0	1	0	138.00	69.00	0.50	69.00	34.50	17.25	34.50
0	1	0	0	1	1	142.00	71.00	0.50	71.00	35.50	17.75	35.50
0	1	0	1	0	0	146.00	73.00	0.50	73.00	36.50	18.25	36.50
0	1	0	1	0	1	150.00	75.00	0.50	75.00	37.50	18.75	37.50
0	1	0	1	1	0	153.00	76.50	0.50	76.50	38.25	19.13	38.25
0	1	0	1	1	1	156.00	78.00	0.50	78.00	39.00	19.50	39.00
0	1	1	0	0	0	159.10	79.55	0.50	79.55	39.78	19.89	39.78
0	1	1	0	0	1	162.00	81.00	0.50	81.00	40.50	20.25	40.50
0	1	1	0	1	0	165.00	82.50	0.50	82.50	41.25	20.63	41.25
0	1	1	0	1	1	168.00	84.00	0.50	84.00	42.00	21.00	42.00
0	1	1	1	0	0	171.00	85.50	0.50	85.50	42.75	21.38	42.75
0	1	1	1	0	1	174.00	87.00	0.50	87.00	43.50	21.75	43.50
0	1	1	1	1	0	177.00	88.50	0.50	88.50	44.25	22.13	44.25
0	1	1	1	1	1	180.00	90.00	0.50	90.00	45.00	22.50	45.00
SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	CPU/2	3V66/ CPU	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz) FREQ_APIC=1	IOAPIC (MHz) FREQ_APIC=0

1	0	0	0	0	0	134.00	67.00	0.50	67.00	33.50	16.75	33.50
1	0	0	0	0	1	135.00	67.50	0.50	67.50	33.75	16.88	33.75
1	0	0	0	1	0	136.00	68.00	0.50	68.00	34.00	17.00	34.00
1	0	0	0	1	1	137.00	68.50	0.50	68.50	34.25	17.13	34.25
1	0	0	1	0	0	139.00	69.50	0.50	69.50	34.75	17.38	34.75
1	0	0	1	0	1	140.00	70.00	0.50	70.00	35.00	17.50	35.00
1	0	0	1	1	0	143.00	71.50	0.50	71.50	35.75	17.88	35.75
1	0	0	1	1	1	144.00	72.00	0.50	72.00	36.00	18.00	36.00
1	0	1	0	0	0	145.00	72.50	0.50	72.50	36.25	18.13	36.25
1	0	1	0	0	1	147.00	73.50	0.50	73.50	36.75	18.38	36.75
1	0	1	0	1	0	148.00	74.00	0.50	74.00	37.00	18.50	37.00
1	0	1	0	1	1	149.00	74.50	0.50	74.50	37.25	18.63	37.25
1	0	1	1	0	0	152.00	76.00	0.50	76.00	38.00	19.00	38.00
1	0	1	1	0	1	154.00	77.00	0.50	77.00	38.50	19.25	38.50
1	0	1	1	1	0	155.00	77.50	0.50	77.50	38.75	19.38	38.75
1	0	1	1	1	1	157.00	78.50	0.50	78.50	39.25	19.63	39.25
1	1	0	0	0	0	158.00	79.00	0.50	79.00	39.50	19.75	39.50
1	1	0	0	0	1	160.00	80.00	0.50	80.00	40.00	20.00	40.00
1	1	0	0	1	0	163.00	81.50	0.50	81.50	40.75	20.38	40.75
1	1	0	0	1	1	164.00	82.00	0.50	82.00	41.00	20.50	41.00
1	1	0	1	0	0	166.00	83.00	0.50	83.00	41.50	20.75	41.50
1	1	0	1	0	1	167.00	83.50	0.50	83.50	41.75	20.88	41.75
1	1	0	1	1	0	169.00	84.50	0.50	84.50	42.25	21.13	42.25
1	1	0	1	1	1	170.00	85.00	0.50	85.00	42.50	21.25	42.50
1	1	1	0	0	0	172.00	86.00	0.50	86.00	43.00	21.50	43.00
1	1	1	0	0	1	173.00	86.50	0.50	86.50	43.25	21.63	43.25
1	1	1	0	1	0	175.00	87.50	0.50	87.50	43.75	21.88	43.75
1	1	1	0	1	1	181.00	90.50	0.50	90.50	45.25	22.63	45.25
1	1	1	1	0	0	183.00	91.50	0.50	91.50	45.75	22.88	45.75
1	1	1	1	0	1	185.00	92.50	0.50	92.50	46.25	23.13	46.25
1	1	1	1	1	0	190.00	95.00	0.50	95.00	47.50	23.75	47.50
1	1	1	1	1	1	200.00	100.00	0.50	100.00	50.00	25.00	50.00

5.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I^2C)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (0,2, 6:4)
2	0	-	SSEL4 (Frequency table selection by software via I^2C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	SSEL5 (Frequency table selection by software via I^2C)

5.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	40	CPUCLK0(Active / Inactive)
6	1	38	CPUCLK1(Active / Inactive)
5	1	37	CPUCLK2(Active / Inactive)
4	1	42	CPU/2(Active / Inactive)
3	1	47	IOAPIC0 (Active / Inactive)
2	1	46	IOAPIC1 (Active / Inactive)
1	1	2	REF1 (Active / Inactive)
0	1	3	REF0 (Active / Inactive)

5.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	18	PCICLK7 (Active / Inactive)
6	1	17	PCICLK6 (Active / Inactive)
5	1	15	PCICLK5 (Active / Inactive)
4	1	14	PCICLK4 (Active / Inactive)
3	1	12	PCICLK3 (Active / Inactive)
2	1	11	PCICLK2 (Active / Inactive)
1	1	9	PCICLK1 (Active / Inactive)
0	1	8	PCICLK_F (Active / Inactive)

5.4 Register 3: 3V66 Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	34	3V66_0(Active / Inactive)
6	1	33	3V66_1(Active / Inactive)
5	1	32	3V66_2(Active / Inactive)
4	**X**	**-**	**FS1#**
3	0	-	0 = ±0.25% Center type Spread Spectrum Modulation 1 =±0.5% Center type Spread Spectrum Modulation
2	0	-	0 = Running 1 = Tristate all outputs
1	**X**	**-**	**FS3#**
0	**X**	**-**	**FS2#**

5.5 Register 4: PCI Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	26	24_48MHz(Active / Inactive)
6	1	27	48MHz(Active / Inactive)
5	**X**	**-**	**FS0#**
4	1	22	PCICLK10 (Active / Inactive)
3	1	21	PCICLK9 (Active / Inactive)
2	1	20	PCICLK8 (Active / Inactive)
1	1	-	Reserve
0	**X**	**-**	**FS4#**

5.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	**1**	**-**	**Skew2 (CPU to 3V66 skew program bit)**
6	**0**	**-**	**Skew1 (CPU to 3V66 skew program bit)**
5	**0**	**-**	**Skew0 (CPU to 3V66 skew program bit)**
4	1	-	Reserve
3	1	-	Reserve
2	1	-	Reserve
1	1	-	Reserve
0	1	-	Reserve

5.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

5.8 Register 7: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**0**	**-**	**Winbond Chip ID**
5	**1**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Version ID**
2	**0**	**-**	**Winbond Version ID**
1	**0**	**-**	**Winbond Version ID**
0	**1**	**-**	**Winbond Version ID**

5.9 Register 8: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	0	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

5.10 Register 9: M/N Program Register and 3V66 Divisor

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	0	-	3V66 divisor 00: CPU/2 ; 01: CPU/1.5
5	0	-	3V66 divisor 10: CPU/1 ; 11: CPU/3
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

5.11 Register 10: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

5.12 Register 11: Divisor Register

Bit	@PowerUp	Pin	Description
7	1	-	Spread spectrum up count[0:3]
6	1	-	Spread spectrum up count[0:3]
5	1	-	Spread spectrum up count[0:3]
4	1	-	Spread spectrum up count[0:3]
3	1	-	Spread spectrum down count[0:3]
2	1	-	Spread spectrum down count[0:3]
1	1	-	Spread spectrum down count[0:3]
0	1	-	Spread spectrum down count[0:3]

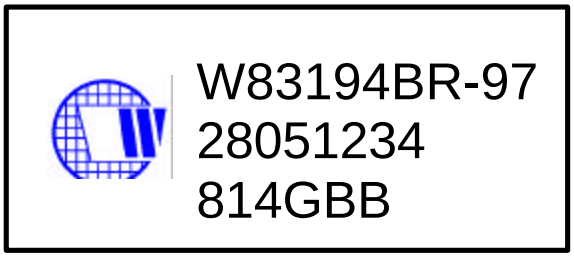
5.12 Register 12 Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register 9~12 to program frequency The equation is **CPU freq. = 14.318MHz * (N+4)/ 2*M**
6	1	-	Reserve
5	1	-	Reserve
4	1	-	Reserve
3	1	-	Reserve
2	1	-	Reserve
1	1	-	Reserve
0	1	-	Reserve

6.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-97	48 PIN SSOP	Commercial, 0°C to +70°C

7.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-97

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

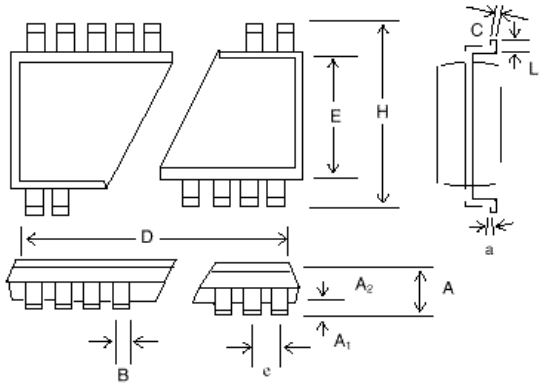
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

B: Winbond internal use code

B: IC revision

8.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668