8Mx32 SDRAM

FEATURES

- 53% Space Savings vs. Monolithic Solution
- Reduced System Inductance and Capacitance
- Pinout and Footprint Compatible to SSRAM 119 BGA
- 3.3V Operating Supply Voltage
- Fully Synchronous to Positive Clock Edge
- Clock Frequencies of 133MHz, 125MHz and 100MHz
- Burst Operation
  - Sequential or Interleave
  - Burst Length = Programmable 1, 2, 4, 8 or Full Page
  - Burst Read and Write
  - Multiple Burst Read and Single Write
- Data Mask Control Per Byte
- Auto and Self Refresh
- Automatic and Controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 119 Pin BGA, JEDEC MO-163

DESCRIPTION

The WED3DL328V is an 8Mx32 Synchronous DRAM configured as 4x2Mx32. The SDRAM BGA is constructed with two 8Mx16 SDRAM die mounted on a multi-layer laminate substrate and packaged in a 119 lead, 14mm by 22mm, BGA.

The WED3DL328V is an ideal SDRAM wide I/O memory solution for all high performance, computer applications which include Network Processors, DSPs and Functional ASICs.

The WED3DL328V is available in clock speeds of 133MHz, 125MHz and 100MHz. The range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The package and design provides performance enhancements via a 50% reduction in capacitance vs. two monolithic devices. The design includes internal ground and power planes which reduces inductance on the ground and power pins allowing for improved decoupling and a reduction in system noise.

PIN CONFIGURATION (TOP VIEW)

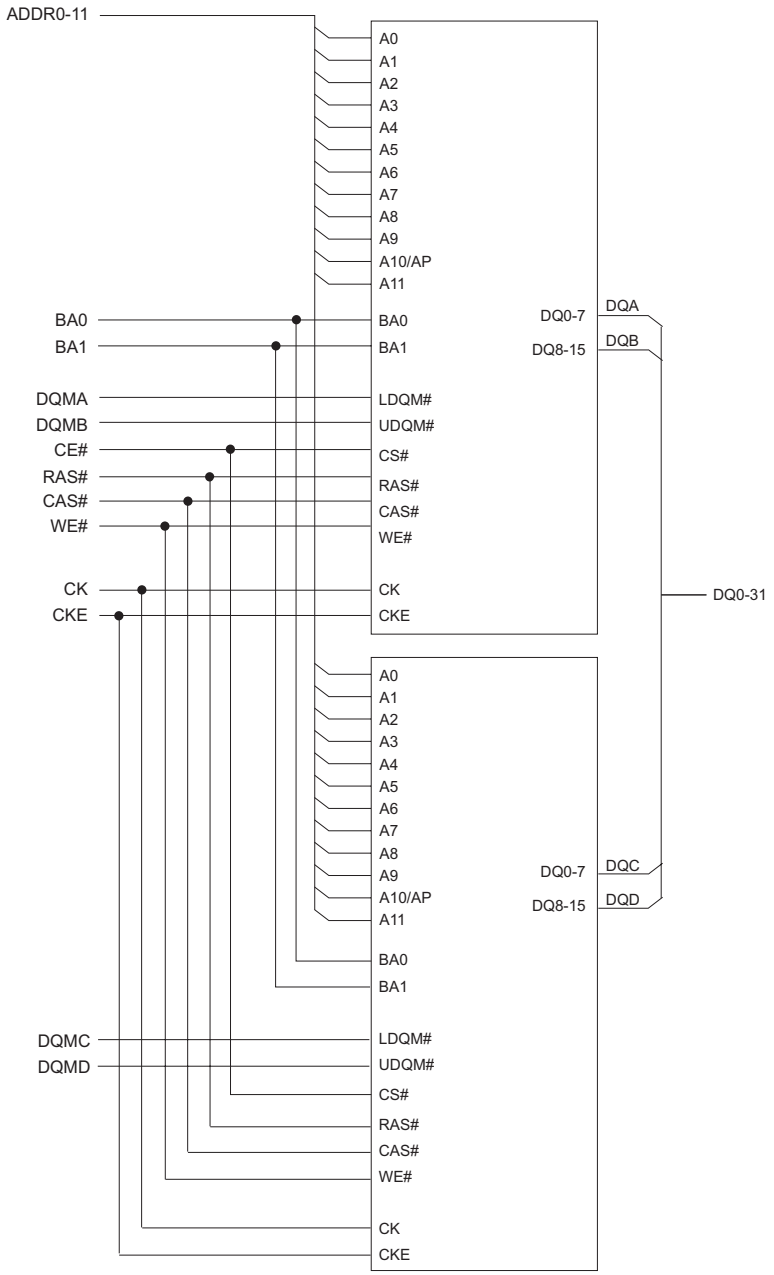
	1	2	3	4	5	6	7	
A	V_{CCQ}	NC	BA0	NC	A10	A7	V_{CCQ}	A
B	NC	NC	NC/A12*	CAS#	A11	NC	NC	B
C	NC	NC	BA1	V_{CC}	A9	A8	NC	C
D	DQc	NC	V_{SS}	NC	V_{SS}	NC	DQb	D
E	DQc	DQc	V_{SS}	CE#	V_{SS}	DQb	DQb	E
F	V_{CCQ}	DQc	V_{SS}	RAS#	V_{SS}	DQb	V_{CCQ}	F
G	DQc	DQc	DQMC	NC	DQMB	DQb	DQb	G
H	DQc	DQc	V_{SS}	CKE	V_{SS}	DQb	DQb	H
J	V_{CCQ}	VCC	NC	V_{CC}	NC	V_{CC}	V_{CCQ}	J
K	DQd	DQd	V_{SS}	CK	V_{SS}	DQa	DQa	K
L	DQd	DQd	DQMD	NC	DQMA	DQa	DQa	L
M	V_{CCQ}	DQd	V_{SS}	WE#	V_{SS}	DQa	V_{CCQ}	M
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa	N
P	DQd	NC	V_{SS}	A0	V_{SS}	NC	DQa	P
R	NC	A6	NC	V_{CC}	NC	A2	NC	R
T	NC	NC	A5	A4	A3	NC	NC	T
U	V_{CCQ}	NC	NC	NC	NC	NC	V_{CCQ}	U
	1	2	3	4	5	6	7	

*NOTE: Pin B3 is designated as NC/A12. This pin is used for future density upgrades as address pin A12.

PIN DESCRIPTION

A0 – A11	Address Bus
BA0-1	Bank Select Addresses
DQ	Data Bus
CK	Clock
CKE	Clock Enable
DQM	Data Input/Output Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
CE#	Chip Enable
V_{CC}	Power Supply pins, 3.3V
V_{CCQ}	Data Bus Power Supply pins,3.3V
V_{SS}	Ground pins

FIG. 1 8MX32 SDRAM BLOCK DIAGRAM



INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Signal	Polarity	Function
CK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
CE#	Input	Pulse	Active Low	CE# disable or enable device operation by masking or enabling all inputs except CK, CKE and DQM.
RAS#, CAS# WE#	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be executed by the SDRAM.
BA0,BA1	Input	Level	—	Selects which SDRAM bank is to be active.
A0-11, A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-11 defines the row address (RA0-11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-8 defines the column address (CA0-8) when sampled at the rising clock edge. In addition to the row address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If A10/AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged . If A10/AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If A10/AP is high, all banks will be precharged regardless of the state of BA0, BA1. If A10/AP is low, then BA0, BA1 is used to define which bank to precharge.
DQ	Input/Output	Level	—	Data Input/Output are multiplexed on the same pins
DQM	Input	Pulse	Mask	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write Active High mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
V_{CC}, V_{SS}	Supply			Power and ground for the input buffers and the core logic.
V_{CCQ}	Supply			Isolated power and ground for the output buffers to improve noise immunity.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{CC}/V_{CCQ}	-1.0	+4.6	V
Input Voltage	V_{IN}	-1.0	+4.6	V
Output Voltage	V_{OUT}	-1.0	+4.6	V
Operating Temperature	t_{OPR}	-0	+70	°C
Storage Temperature	t_{STG}	-55	+125	°C
Power Dissipation	P_D	—	1.5	W
Short Circuit Output Current	I_{OS}	—	50	mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}/V_{CCQ}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	3.0	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Output High Voltage (I_{OH} = -2mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}	—	—	0.4	V
Input Leakage Voltage	I_{IL}	-5	—	5	µA
Output Leakage Voltage	I_{OL}	-5	—	5	µA

CAPACITANCE

(T_A = 25°C, f = 1MHz, V_{DD} = 3.3V)

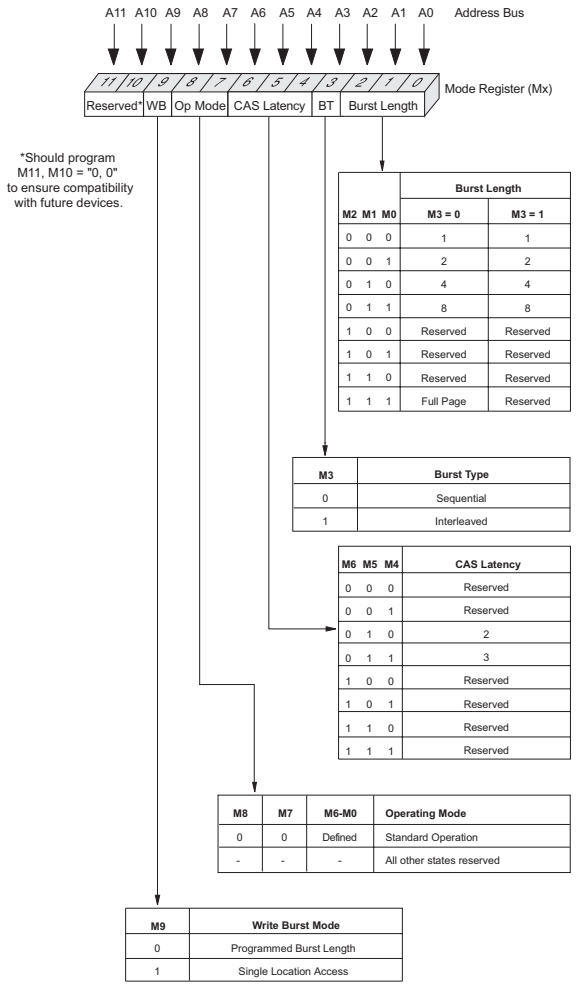
Parameter	Symbol	Max	Unit
Input Capacitance	C_{I1}	4	pF
Input/Output Capacitance (DQ)	C_{OUT}	5	pF

OPERATING CURRENT CHARACTERISTICS
(V_{CC} = 3.6V)

Parameter	Symbol	Conditions	7	8	10	Units
Operating Current (One Bank Active) (1)	I_{CC1}	Burst Length = 1, $t_{RC} \geq t_{RC}$(min), I_{OL} = 0mA	300	280	225	mA
Operating Current (Burst Mode) (1)	I_{CC4}	Page Burst, 4 banks active, t_{CCD} = 2 clocks	340	290	240	mA
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns	2	2	2	mA
	I_{CC2PS}	CKE, CK ≤ V_{IL}(max), t_{CC} = ∞, Inputs Stable	2	2	2	mA
Precharge Standby Current in Non-Power Down Mode	I_{CC1N}	CKE = V_{IH}, t_{CC} = 15ns Input Change one time every 30ns	100	100	100	mA
	I_{CC1NS}	CKE ≥ V_{IH}(min), t_{CC} = ∞ No Input Change	70	70	70	mA
Precharge Standby Current in Power Down Mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns	12	12	12	mA
	I_{CC3PS}	CKE ≤ V_{IL}(max), t_{CC} = ∞	12	12	12	mA
Active Standby Current in Non-Power Down Mode (One Bank Active)	I_{CC3N}	CKE = V_{IH}, t_{CC} = 15ns Input Change one time every 30ns	60	60	60	mA
	I_{CC3NS}	CKE ≥ V_{IH}(min), t_{CC} = ∞, No Input Change	40	40	40	mA
Refresh Current (2)	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	440	420	420	mA
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	3	3	3	mA

NOTES:
1. Measured with outputs open.
2. Refresh period is 64ms.

FIG. 2 MODE REGISTER DEFINITION



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A11/9/8 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

NOTES:
1. For full-page accesses: y = 2,048 (x4), y = 1,024 (x8), y = 512 (x16).
2. For a burst length of two, A1-A9, A11 (x4), A1-A9 (x8) or A1-A8 (x16) select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A9, A11 (x4), A2-A9 (x8) or A2-A8 (x16) select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A9, A11 (x4), A3-A9 (x8) or A3-A8 (x16) select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-A9, A11 (x4), A0-A9 (x8) or A0-A8 (x16) select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A9, A11 (x4), A0-A9 (x8) or A0-A8 (x16) select the unique column to be accessed, and mode register bit M3 is ignored.

SDRAM AC CHARACTERISTICS

Parameter		Symbol	133MHz		125MHz		100MHz		Units
			Min	Max	Min	Max	Min	Max	
Clock Cycle Time (1)	CL = 3	t_{CC}	7	1000	8	1000	10	1000	ns
	CL = 2	t_{CC}	7.5	1000	10	1000	12	1000	
Clock to valid Output delay (1,2)		t_{SAC}		5.4		6		7	ns
Output Data Hold Time (2)		t_{OH}	3		3		3		ns
Clock HIGH Pulse Width (3)		t_{CH}	2.5		3		3		ns
Clock LOW Pulse Width (3)		t_{CL}	3		3		3		ns
Input Setup Time (3)		t_{SS}	2		2		2		ns
Input Hold Time (3)		t_{SH}	1		1		1		ns
CK to Output Low-Z (2)		t_{SLZ}	1.0		1.0		1.0		ns
CK to Output High-Z		t_{SHZ}		7		7		8	ns
Row Active to Row Active Delay (4)		t_{RRD}	15		20		20		ns
RAS# to CAS# Delay (4)		t_{RCD}	15		20		20		ns
Row Precharge Time (4)		t_{RP}	20		20		24		ns
Row Active Time (4)		t_{RAS}	50	120,000	50	120,000	60	120,000	ns
Row Cycle Time - Operation (4)		t_{RC}	60		70		80		ns
Row Cycle Time - Auto Refresh (4,8)		t_{RFC}	70		70		80		ns
Last Data in to New Column Address Delay (5)		t_{CDL}	1		1		1		CK
Last Data in to Row Precharge (5)		t_{RDL}	1		1		1		CK
Last Data in to Burst Stop (5)		t_{BDL}	1		1		1		CK
Column Address to Column Address Delay (6)		t_{CCD}	1.5		1.5		1.5		CK
Number of Valid OutputData (7)			2		2		2		ea
			1		2		1		

NOTES:

1. Parameters depend on programmed CAS# latency.
2. If clock rise time is longer than 1ns (t_{RISE}/2 -0.5)ns should be added to the parameter.
3. Assumed input rise and fall time = 1ns. If trise of tfall are longer than 1ns. [(t_{RISE} = t_{FALL})/2] - 1ns should be added to the parameter.
4. The minimum number of clock cycles required is detemined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
5. Minimum delay is required to complete write.
6. All devices allow every cycle column address changes.
7. In case of row precharge interrupt, auto precharge and read burst stop.
8. A new command may be given trfc after self-refresh exit.

COMMAND TRUTH TABLE

Function		CKE		CE#	RAS#	CAS#	WE#	DQM	BA	A10/AP A9-0	A11	Notes
		Previous Cycle	Current Cycle									
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			
Refresh	Auto Refresh (CBR)	H	H	L	L	L	H	X	X	X	X	
	Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	
Precharge	Single Bank Precharge	H	X	L	L	H	L	X	BA	L	X	2
	Precharge all Banks	H	X	L	L	H	L	X	X	H	X	
Bank Activate		H	X	L	L	H	H	X	BA	Row Address		2
Write		H	X	L	H	L	L	X	BA	L	Column	2
Write with Auto Precharge		H	X	L	H	L	L	X	BA	H	Column	2
Read		H	X	L	H	L	L	X	BA	L	Column	2
Read with Auto Precharge		H	X	L	H	L	H	X	BA	H	Column	2
Burst Termination		H	X	L	H	H	L	X	X	X	X	3
No Operation		H	X	L	H	H	H	X	X	X	X	
Device Deselect		H	X	H	X	X	X	X	X	X	X	
Clock Suspend/Standby Mode		L	X	X	X	X	X	X	X	X	X	4
Data Write/Output Disable		H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable		H	X	X	X	X	X	H	X	X	X	5
Power Down Mode	Entry	X	L	H	X	X	X	X	X	X	X	6
	Exit	X	H	H	X	X	X	X	X	X	X	6

Notes:

1. All of the SDRAM operations are defined by states of CE#, WE#, RAS#, CAS#, and DQM at the positive rising edge of the clock.
2. Bank Select (BA), if BA = 0 then bank A is selected, if BA = 1 then bank B is selected.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS# latency.
4. During normal access mode, CKE is held high and CK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).

All banks must be precharged before entering the Power Down Mode. The Power Down Mode does not preform any Refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.

CLOCK ENABLE (CKE) TRUTH TABLE

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	CE#	RAS#	CAS#	WE#	BA0-1	A10-11		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down Mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	H	X	L	H	L	L	X		Maintain Power Down Mode	2
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				
	H	H	L	L	H	X				
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				
	H	L	L	L	H	X				
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	H	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to the Operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

NOTES:

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CKS}) must be satisfied before any command other than Exit is issued.
3. The address inputs (A11-0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Power Down Mode, Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.

Must be a legal command as defined in the Current State Truth Table.

CURRENT STATE TRUTH TABLE

Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0-1	A11, A10/AP-A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto orSelf Refresh	Start Auto orSelf Refresh	2,3
	L	L	H	L	X	X	Precharge	No Operation	
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	2
	L	H	H	L	X	X	Burst Termination	No Operation	2
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	6
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	7,8
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	7,8
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	8,9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	8,9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0-1	A11, A10/AP-A0	Description		
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4,10
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{RCD}	
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	9
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	4,9
	L	H	L	H	BA	Column	Read	ILLEGAL	4,9
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	

CURRENT STATE TRUTH TABLE (CONT.)

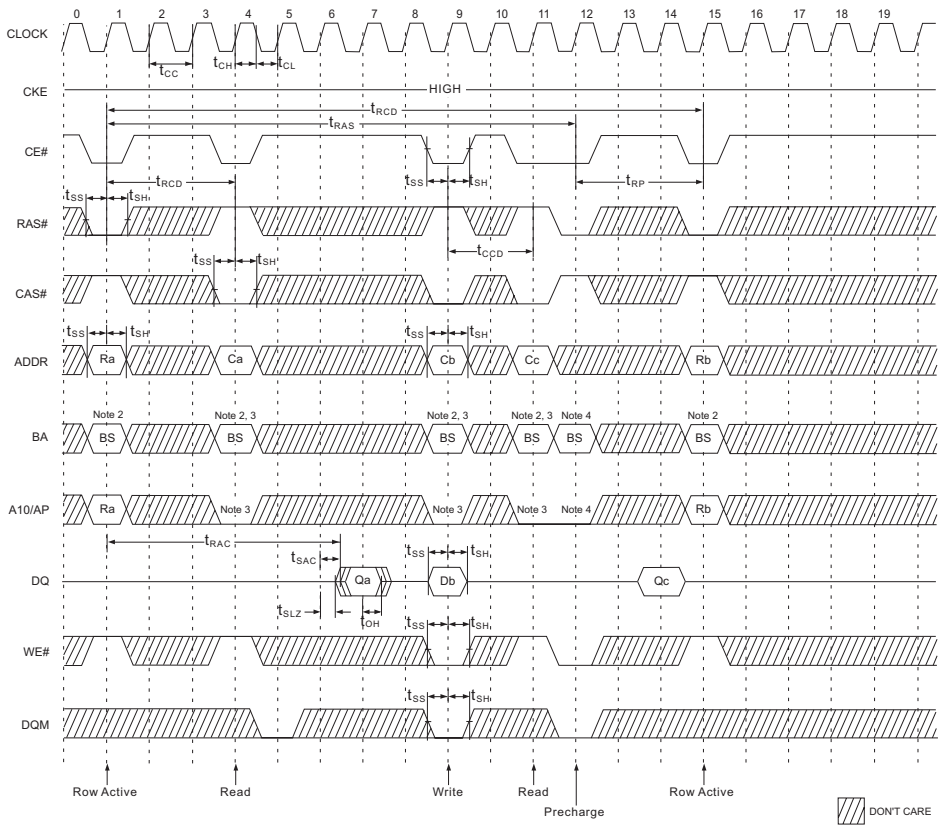
Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA0-1	A11, A10/AP-A0	Description		
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

NOTES:

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the command is being applied to.
2. Both Banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the SDRAM starts the Auto (CBR) Refresh operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The Current State only refers to one of the banks, if BA selects this bank then the action is illegal. If BA selects the bank not being referenced by the Current Sate then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The RAS# to CAS# Delay (t_{RCD}) must occur before the command is given.
8. Address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.

The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satified.

FIG. 3 SINGLE BIT READ-WRITE CYCLE (SAME PAGE) @CAS LATENCY=3, BURST LENGTH=1



NOTES:

1. All input except CKE & DQM can be don't care when CE# is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	x	x	All Banks

3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA0	BA1	Operation
0	0	0	Distribute auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

FIG. 4 POWER UP SEQUENCE

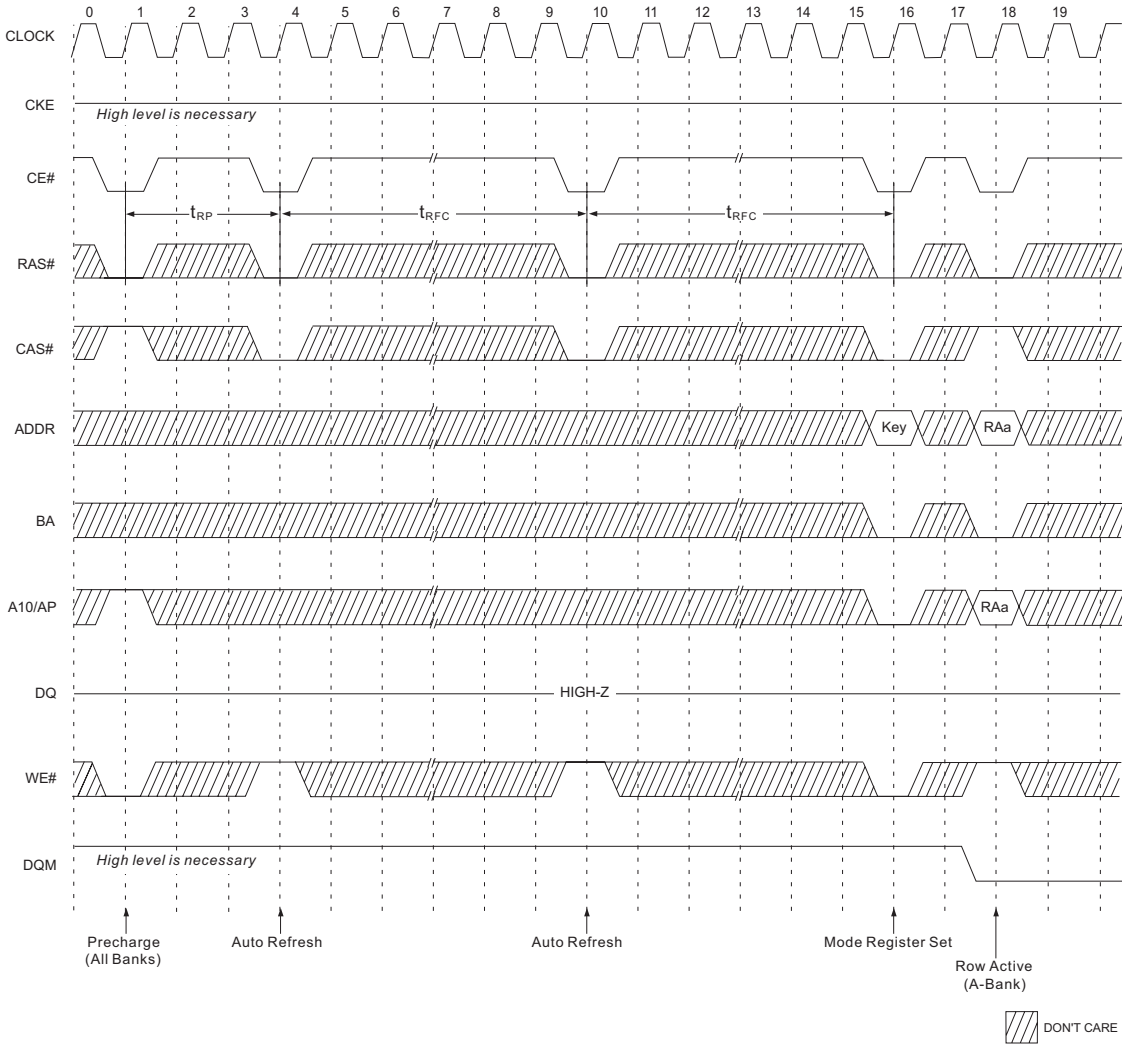
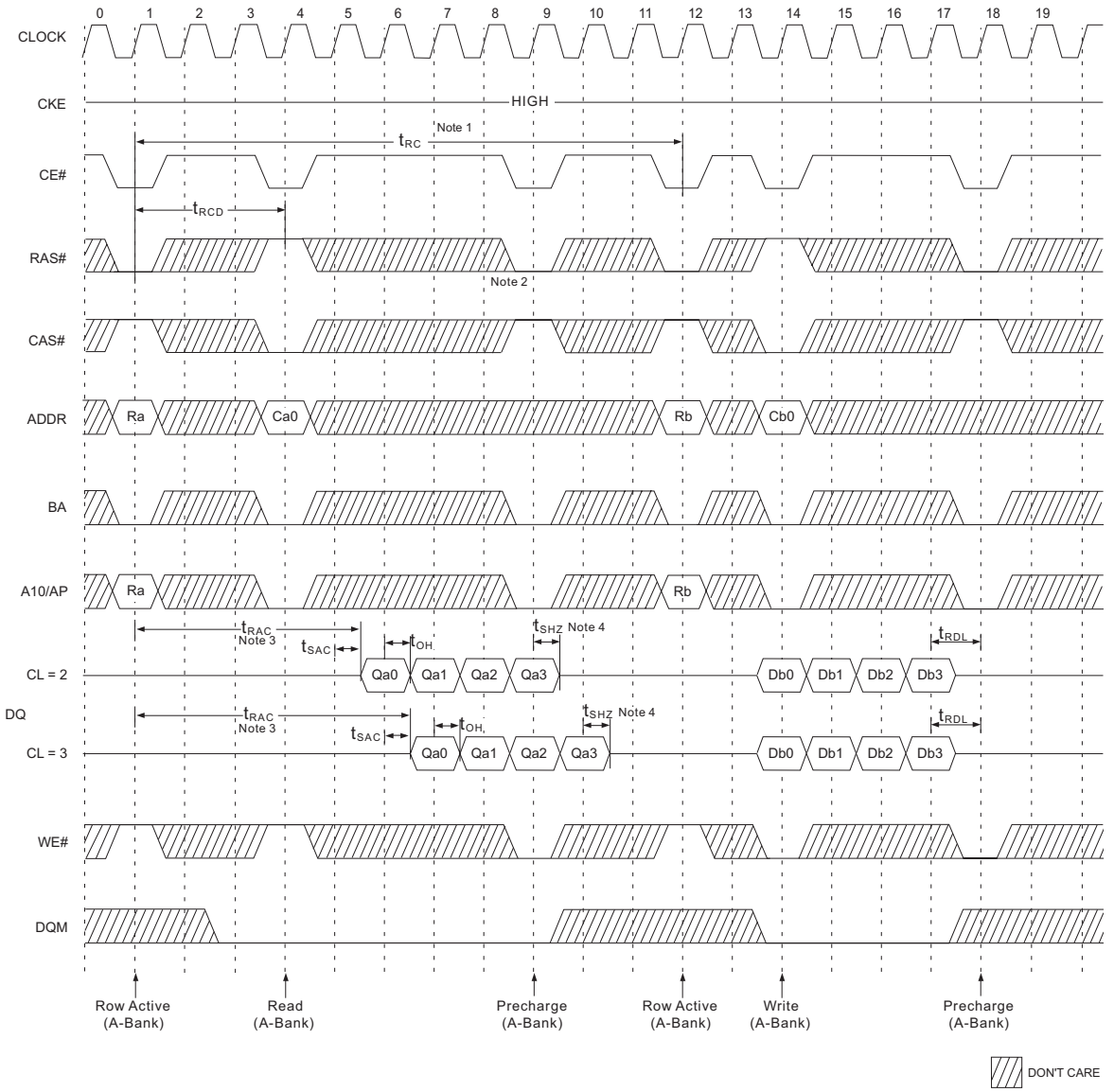


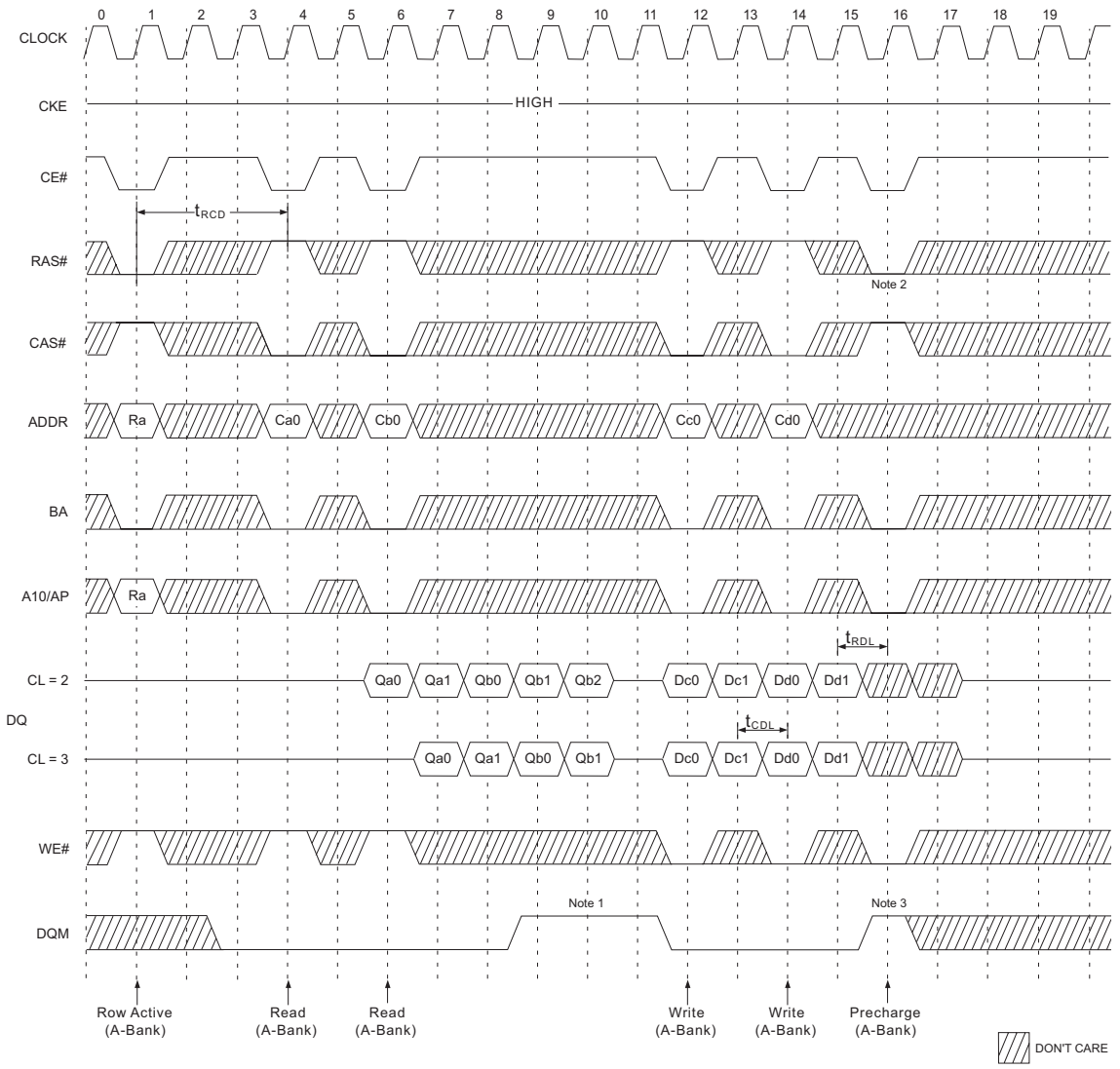
FIG. 5 READ & WRITE CYCLE AT SAME BANK @BURST LENGTH=4



NOTES:

1. Minimum row cycle times are required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. (CAS# Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS# latency - 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst (1, 2, 4, 8 & full page bit burst).

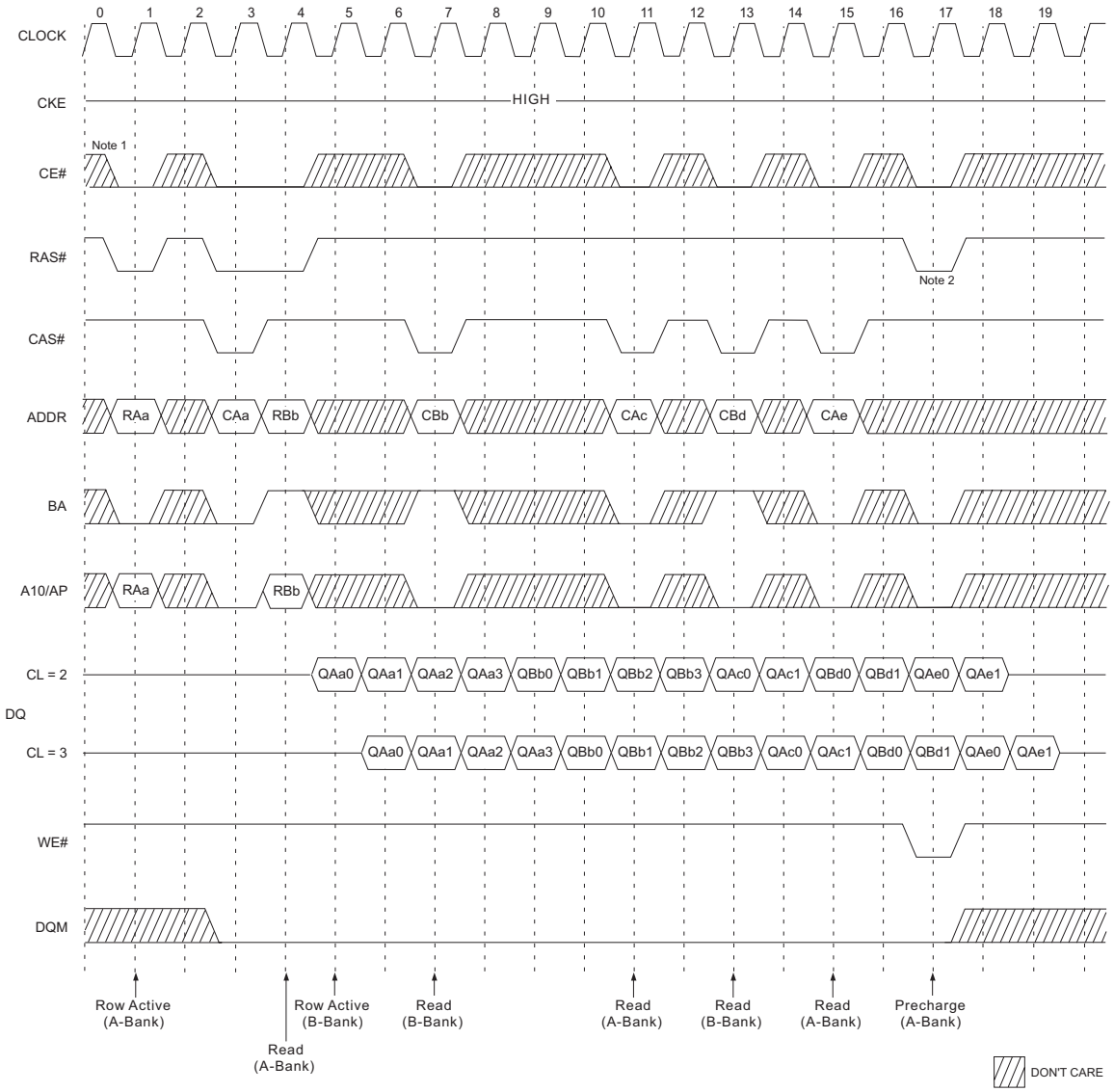
FIG. 6 PAGE READ & WRITE CYCLE AT SAME BANK @BURST LENGTH=4



NOTES:

1. To write data before burst read ends, DQM should be asserted three cycles prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

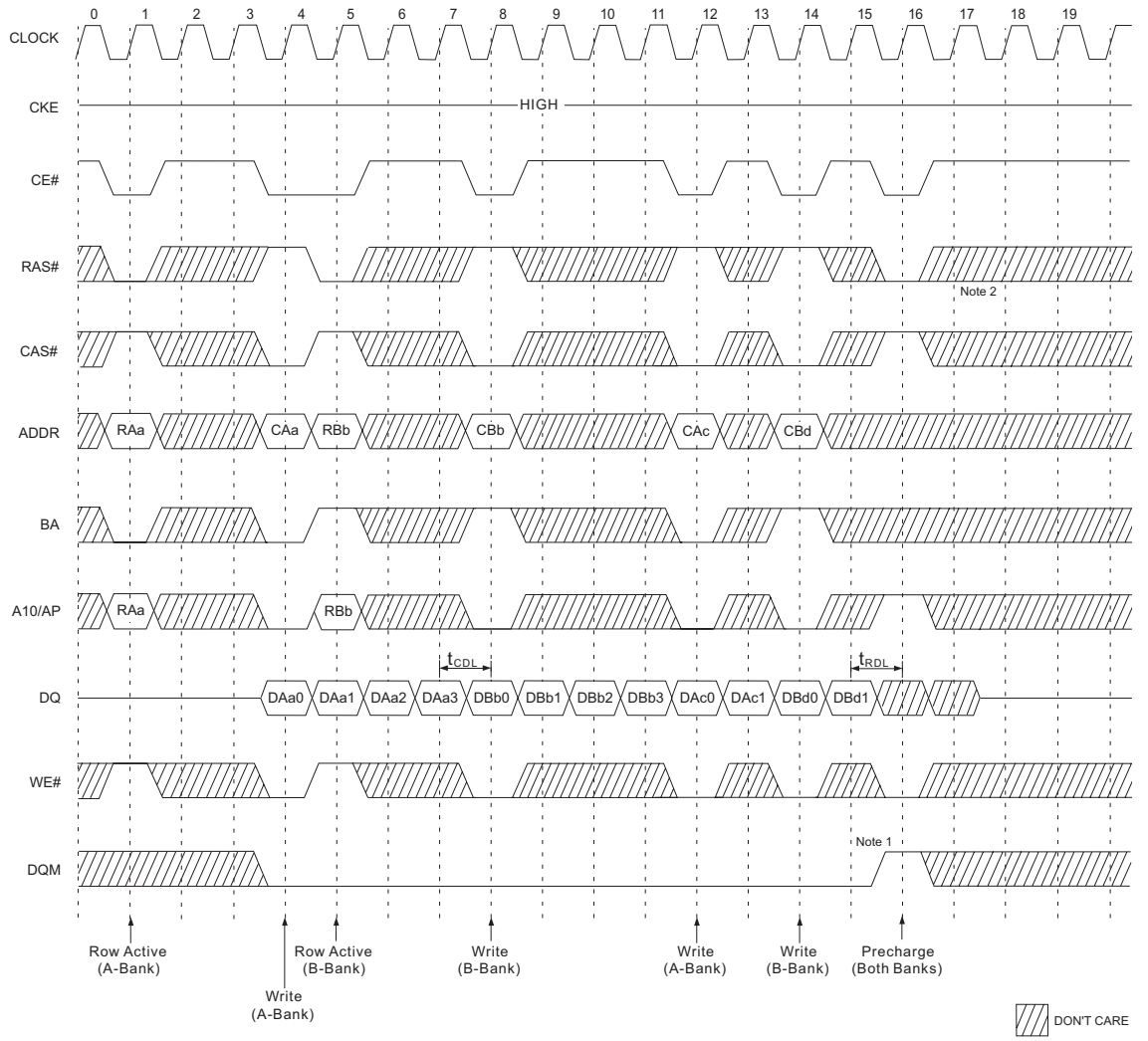
FIG. 7 PAGE READ CYCLE AT DIFFERENT BANK @BURST LENGTH=4



NOTES:

1. CE# can be don't cared when RAS#, CAS# and WE# are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

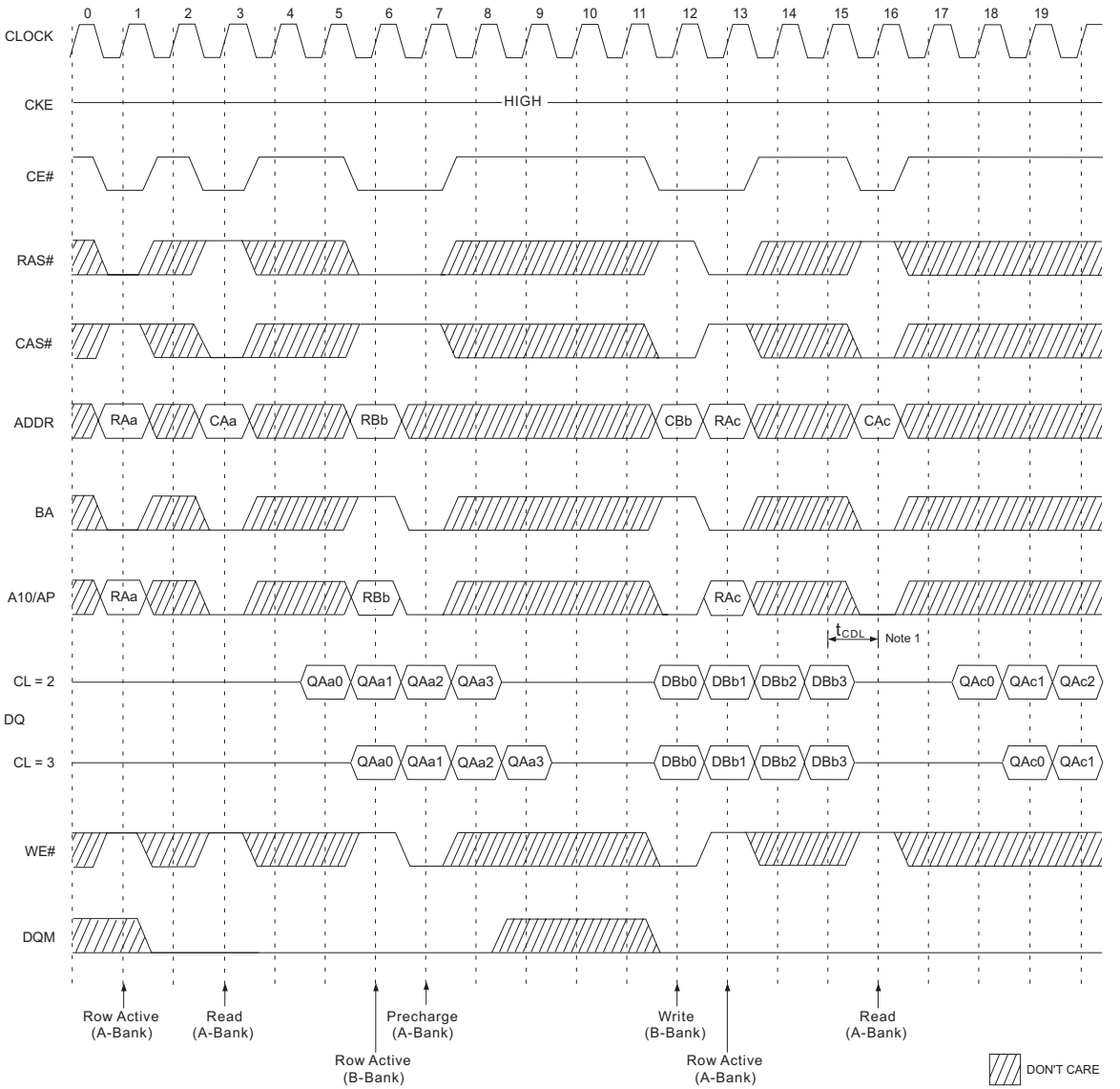
FIG. 8 PAGE WRITE CYCLE AT DIFFERENT BANK @BURST LENGTH=4



NOTES:

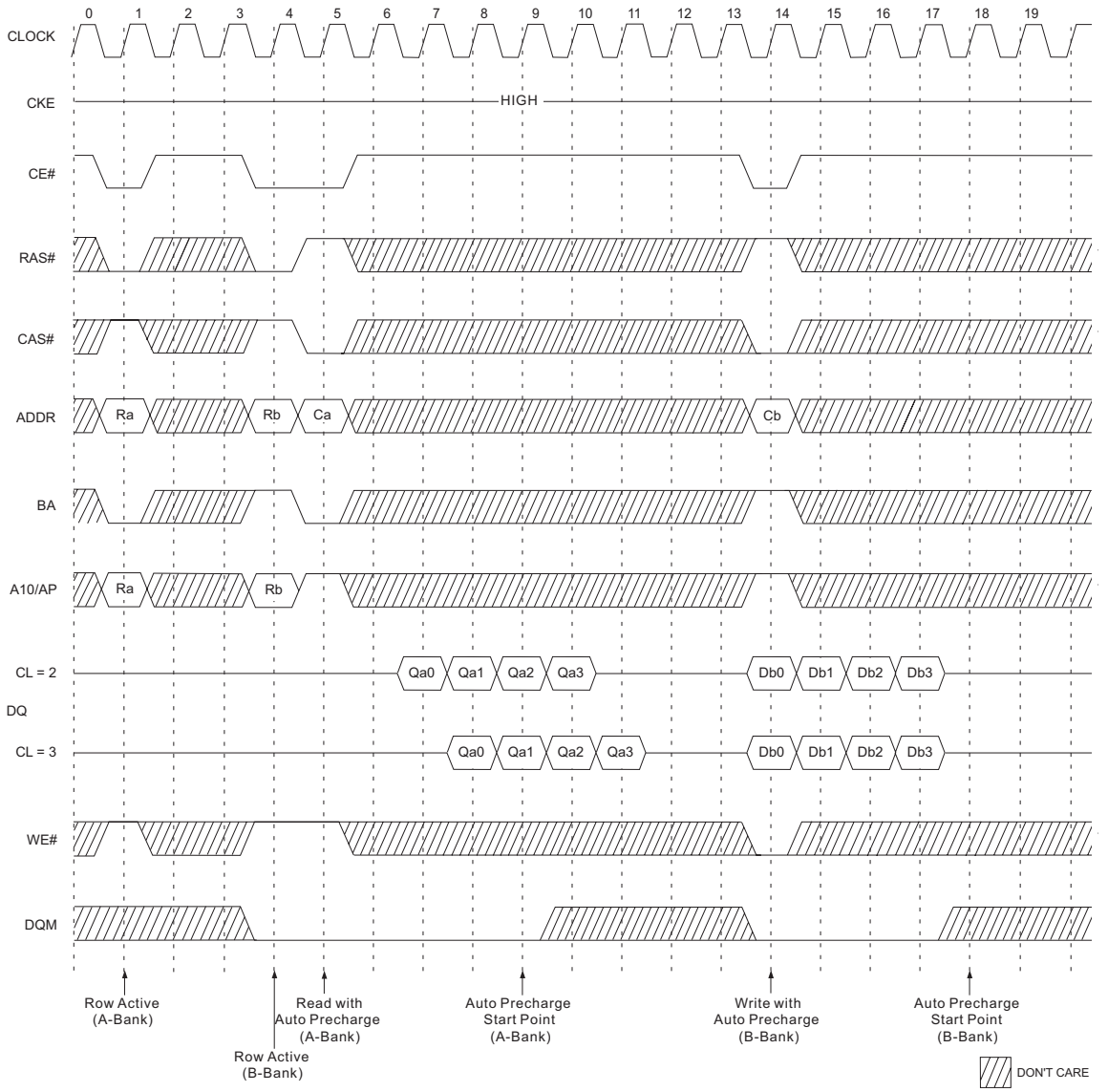
1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

FIG. 9 READ & WRITE CYCLE AT DIFFERENT BANK @BURST LENGTH=4



NOTE:
1. t_{CDL} should be met to complete write.

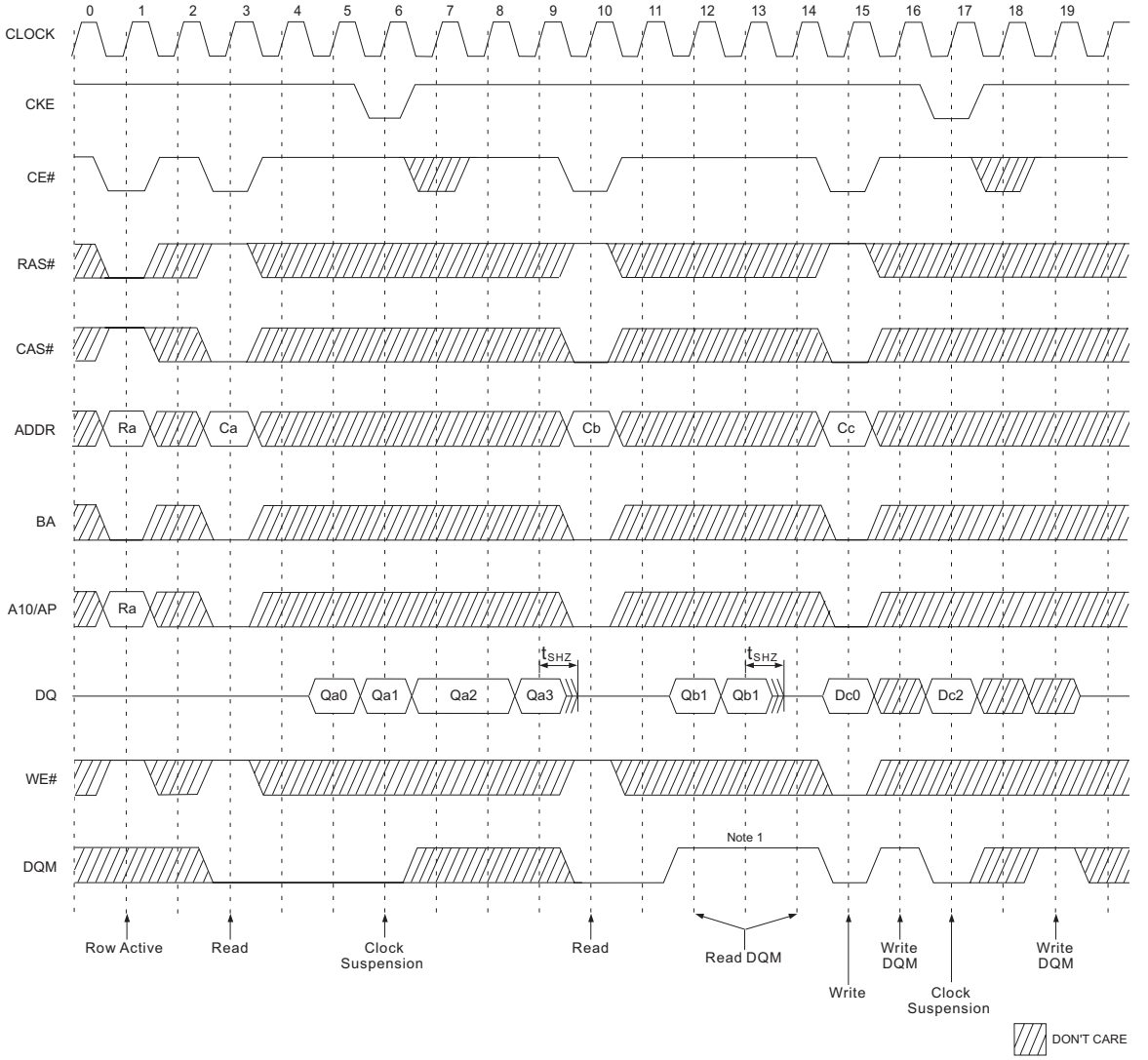
FIG. 10 READ & WRITE CYCLE WITH AUTO PRECHARGE @BURST LENGTH=4



NOTE:

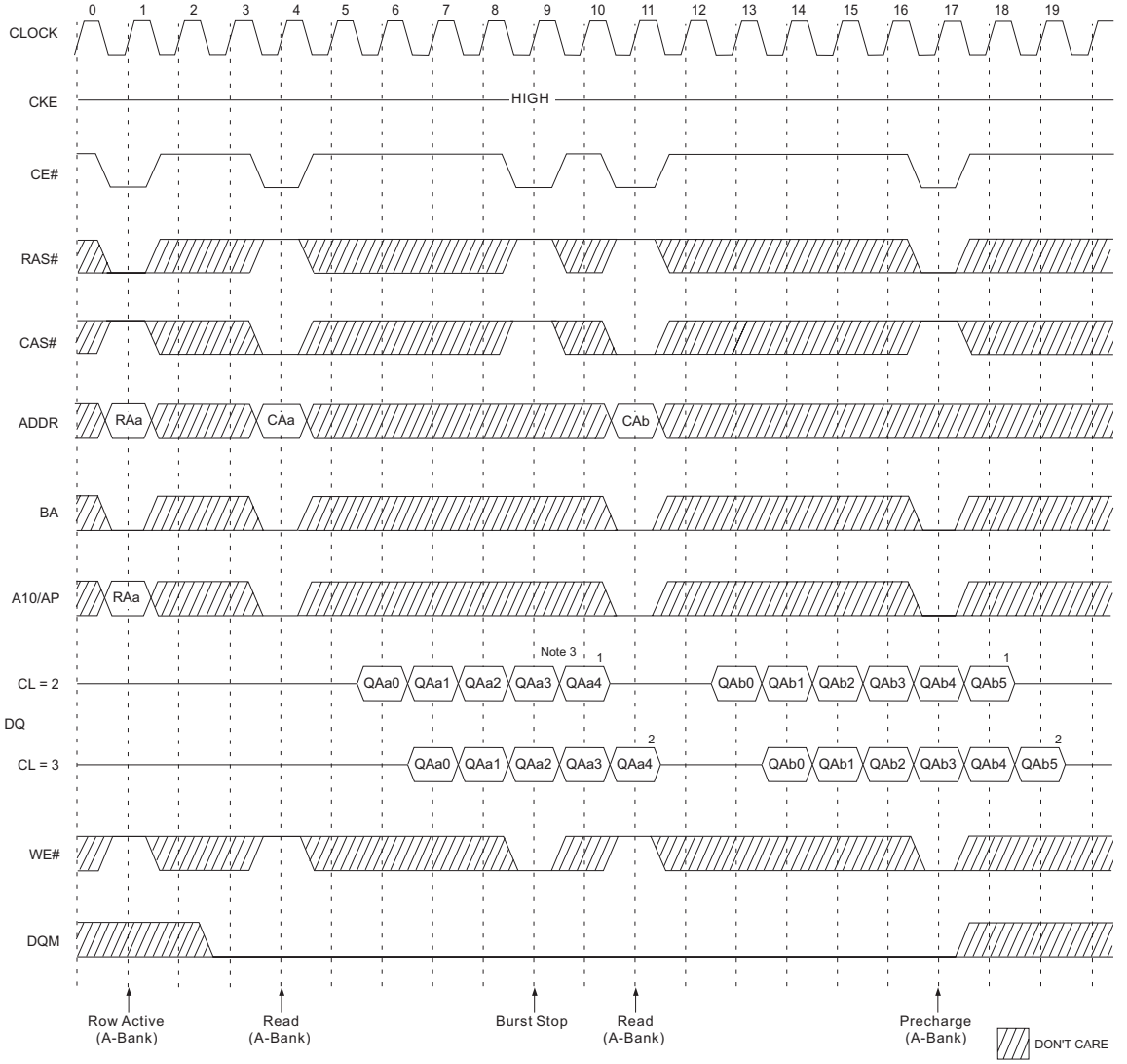
1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
   (in the case of Burst Length=1 & 2 and BRSW mode)

FIG. 11 CLOCK SUSPENSION & DQM OPERATION CYCLE @CAS LATENCY=2, BURST LENGTH=4



NOTE:
1. DQM is needed to prevent bus contention.

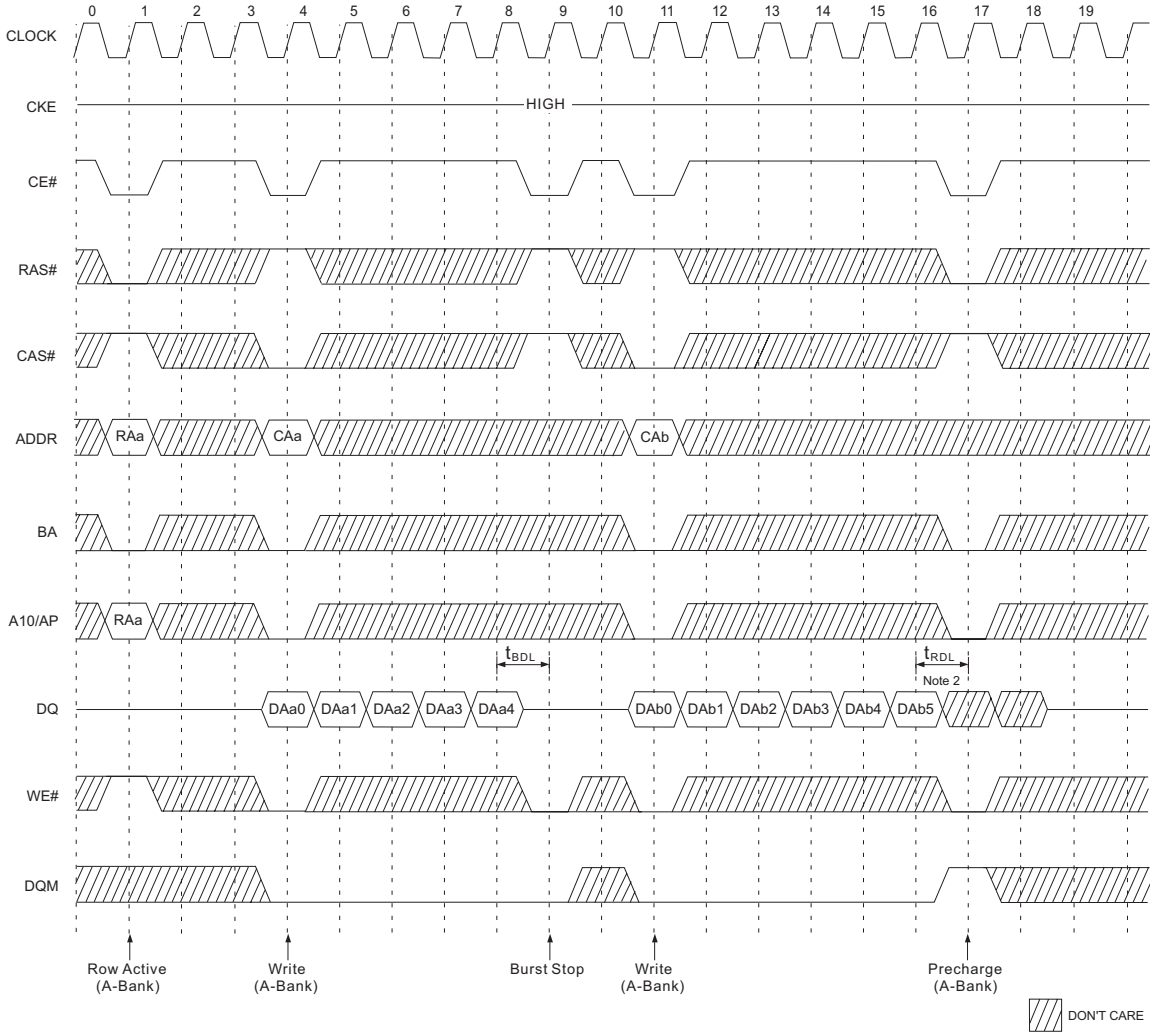
FIG. 12 READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @BURST LENGTH=FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of RAS# interrupt.
   Both cases are illustrated in above timing diagram. See the label 1, 2.
   But at burst write, Burst stop and RAS# interrupt should be compared carefully.
   Refer to the timing diagram of "Full page write burst stop cycle."
3. Burst stop is valid at every burst length.

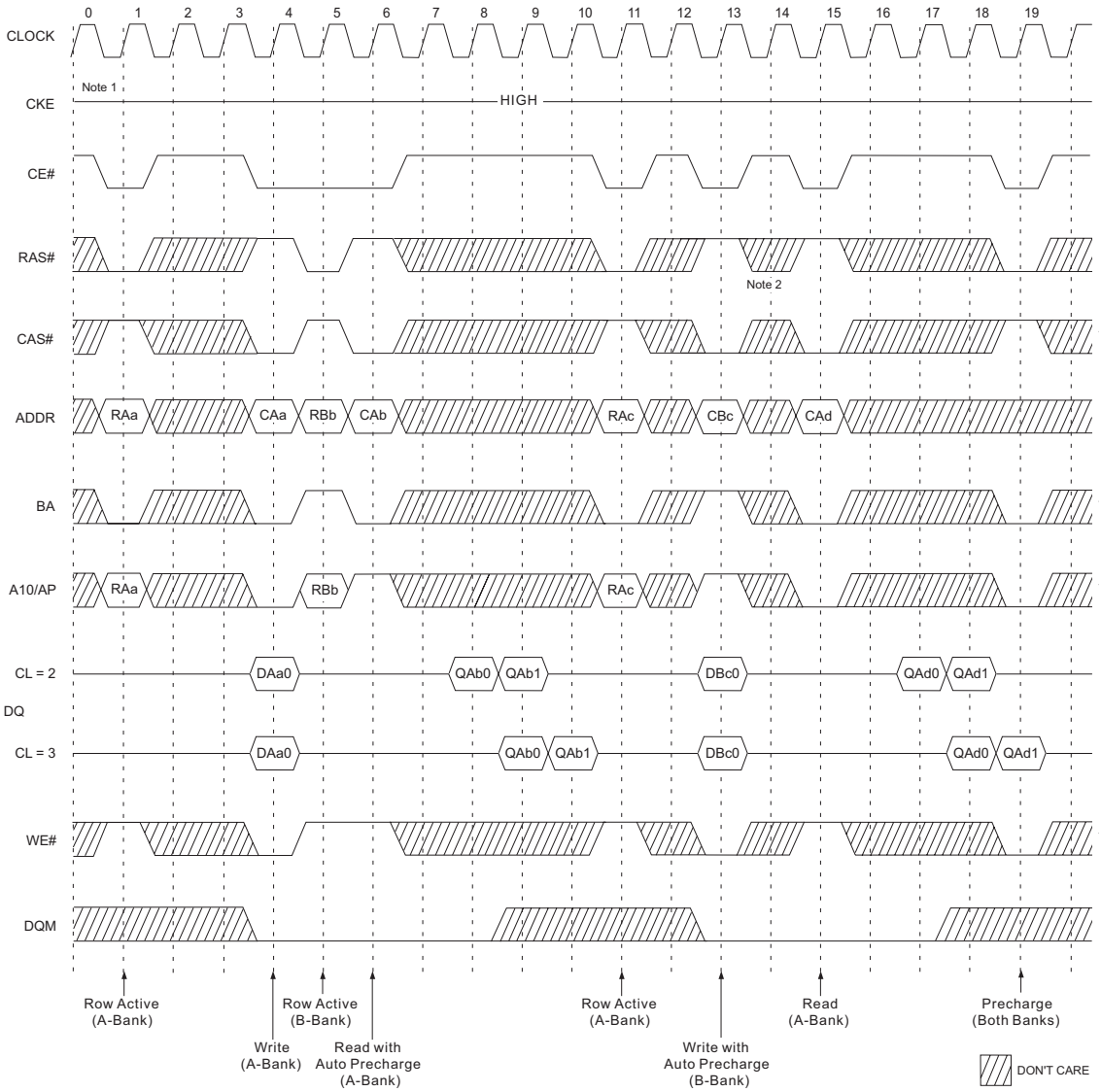
FIG. 13 WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP CYCLE @BURST LENGTH=FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge cannot be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

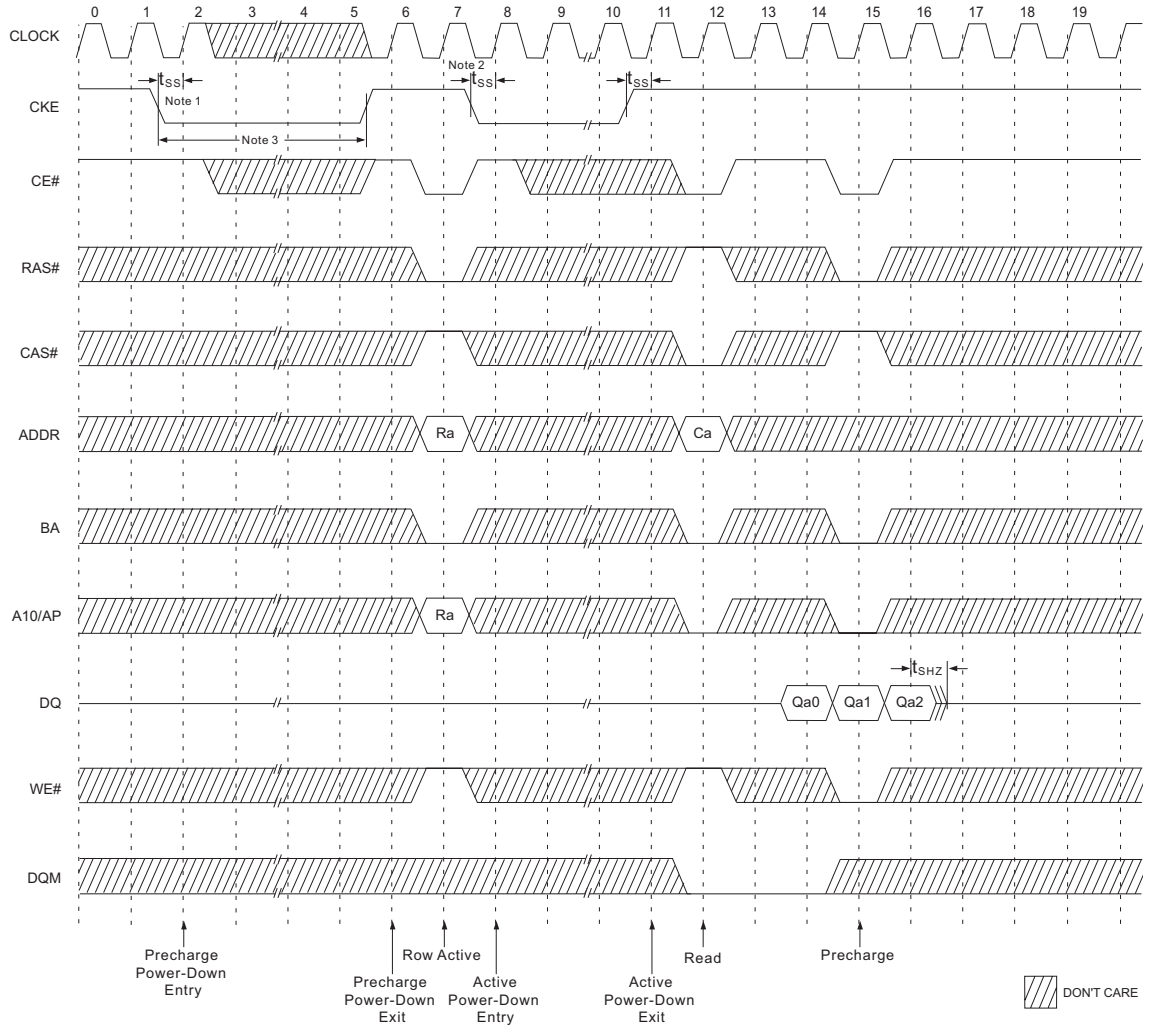
FIG. 14 BURST READ SINGLE BIT WRITE CYCLE @BURST LENGTH=2



NOTES:

1. BRSW mode is enabled by setting As "High" at MRS (Mode Register Set). At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

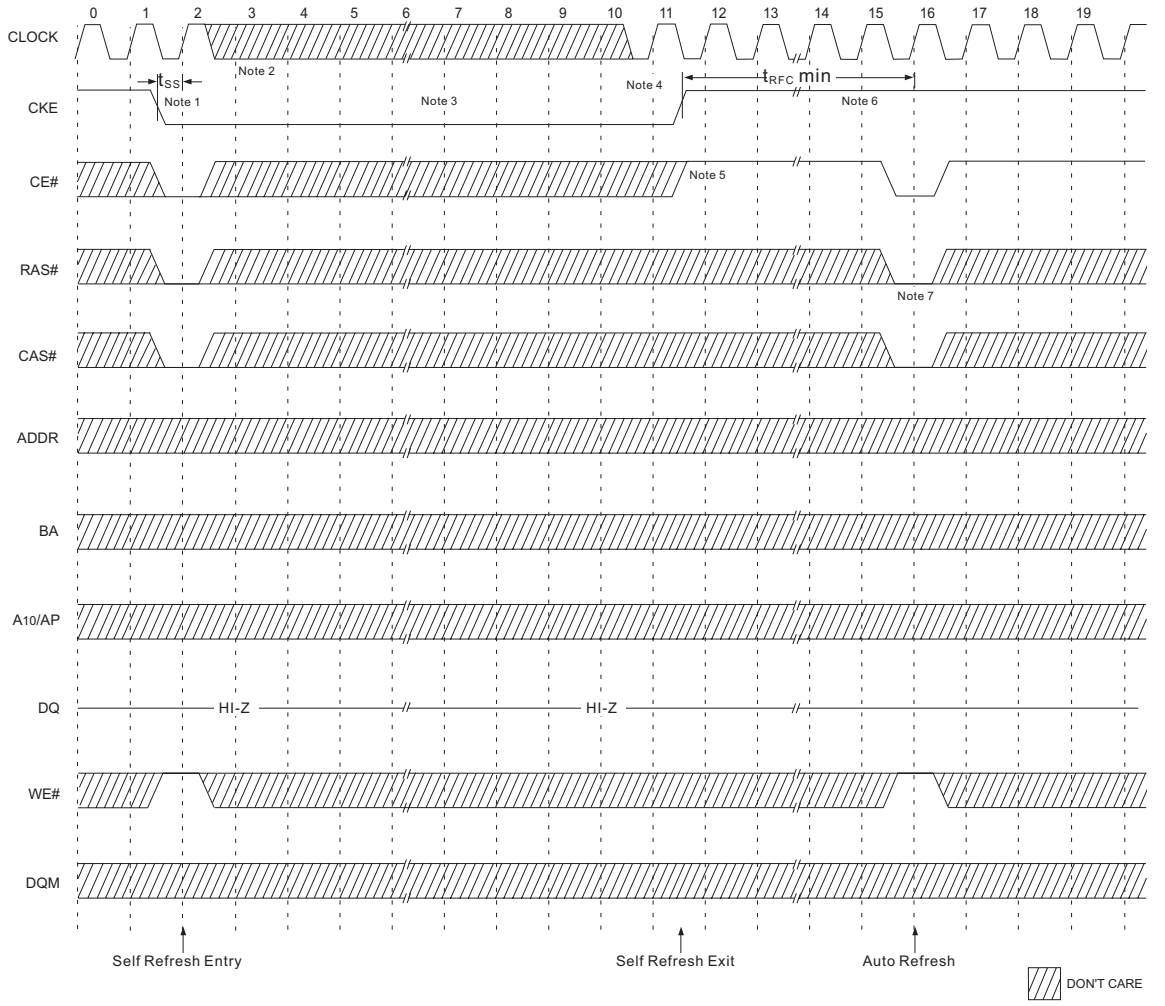
FIG. 15 ACTIVE/PRECHARGE POWER DOWN MODE @CAS# LATENCY=2, BURST LENGTH=4



NOTES:

1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1 CK + t_{SS} prior to Row active command.
3. Cannot violate minimum refresh specification (64ms).

FIG. 16 SELF REFRESH ENTRY & EXIT CYCLE



NOTES:

TO ENTER SELF REFRESH MODE

1. CE#, RAS# & CAS# with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low."
Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. CE# starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

FIG. 17 MODE REGISTER SET CYCLE

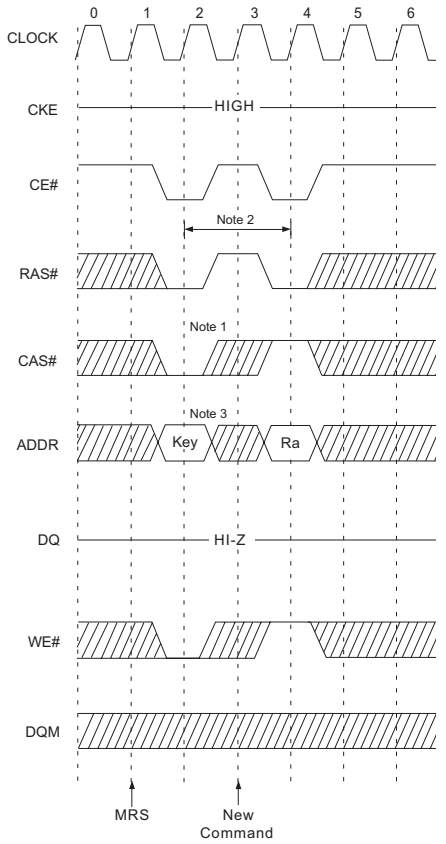
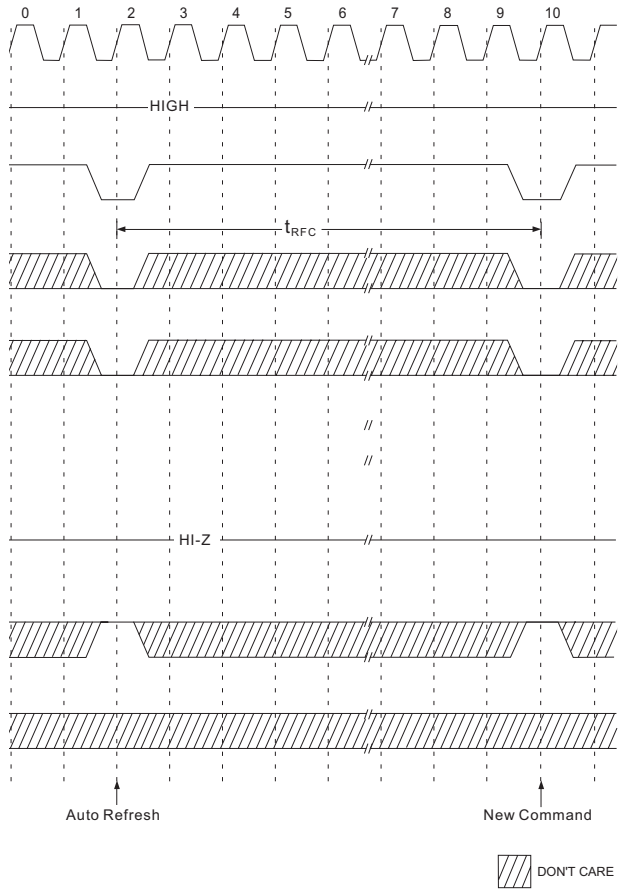


FIG. 18 AUTO REFRESH CYCLE



NOTES:
Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE
1. CE#, RAS#, CAS#, & WE# activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS# activation.
3. Please refer to Mode Register Set table.

PACKAGE DESCRIPTION 119 PIN BGA
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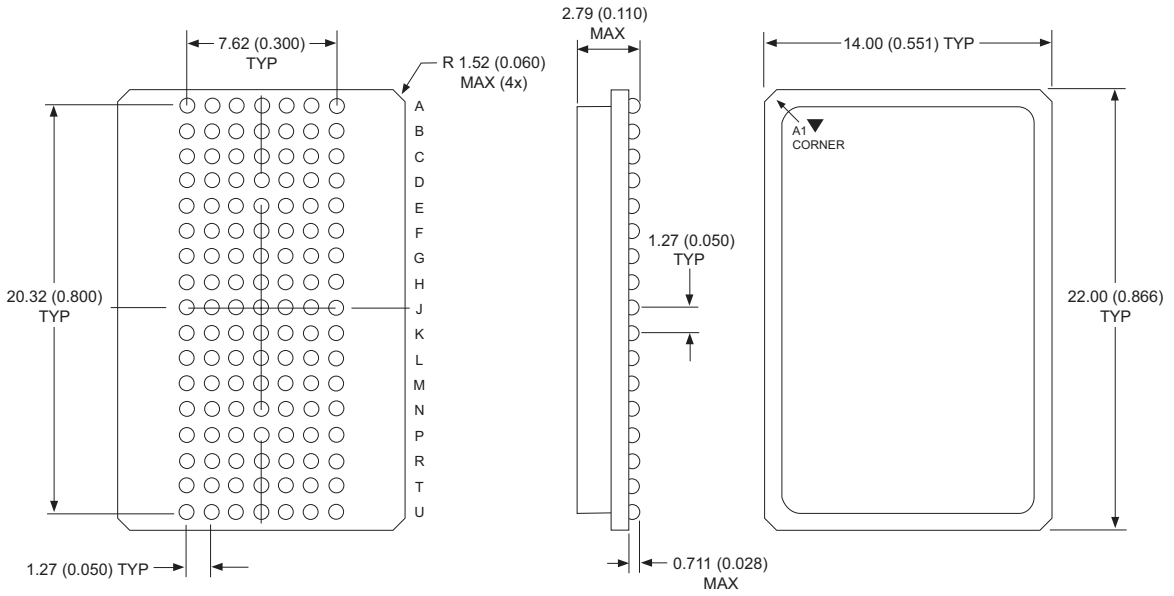

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

Part Number	Clock Frequency	Package	Operating Range
WED3DL328V7BC	133MHz	119 BGA	Commercial
WED3DL328V8BC	125MHz	119 BGA	Commercial
WED3DL328V10BC	100MHz	119 BGA	Commercial
WED3DL328V7BI	133MHz	119 BGA	Industrial
WED3DL328V8BI	125MHz	119 BGA	Industrial
WED3DL328V10BI	100MHz	119 BGA	Industrial