NIPPON PRECISION CIRCUITS INC.

# WF5025 series

## Crystal Oscillator Module ICs

## OVERVIEW

The WF5025 series are miniature crystal oscillator module ICs. They feature a damping resistor $R_D$ matched to the crystal's characteristics to reduce crystal current. The pad layout is arranged for flip chip mounting, which gives the pattern design more flexibility, even for mounting ultra-miniature crystal oscillators that provide almost no space for wiring patterns. They support fundamental oscillation and 3rd overtone oscillation modes. The WF5025 series can be used to correspond to wide range of applications.

## FEATURES

- Pad layout optimized for flip chip mounting
- Miniature-crystal matched oscillator characteristics
- Operating supply voltage range
  - 2.5V operation: 2.25 to 2.75V
  - 3.0V operation: 2.7 to 3.6V
- Recommended operating frequency range
  - For fundamental oscillator
    - WF5025AL×: 20MHz to 50MHz
    - WF5025BL1: 20MHz to 100MHz
  - For 3rd overtone oscillator
    - WF5025ML×: 70MHz to 133MHz
- –40 to 85°C operating temperature range
- Oscillator capacitor with excellent frequency characteristics built-in
- Oscillator circuit with damping resistor $R_D$ built-in for reduced crystal current
- Standby function
  - High impedance in standby mode, oscillator stops
- Low standby current
  - Power-saving pull-up resistor built-in
- Oscillation detector function
- Frequency divider built-in (WF5025AL×)
  - varies with version: $f_O$, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$
- CMOS output duty level (1/2VDD)
- 50 ± 5% output duty @ 1/2VDD
- 30pF output load
- Molybdenum-gate CMOS process

## SERIES CONFIGURATION

| Version | Operating supply voltage [V] | Oscillation mode | Recommended operating frequency range (fundamental oscillation)*1 [MHz] | Output current ($V_{DD}$ = 2.5V) [mA] | Output frequency | Output duty level | Standby mode | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Oscillator stop function | Output state |
| WF5025AL1 | 2.25 to 3.6 | Fundamental | 20 to 50 | 4 | $f_O$ | CMOS | Yes | Hi-Z |
| WF5025AL2 | | | | | $f_O/2$ | | | |
| WF5025AL3 | | | | | $f_O/4$ | | | |
| WF5025AL4 | | | | | $f_O/8$ | | | |
| WF5025AL5 | | | | | $f_O/16$ | | | |
| WF5025AL6 | | | | | $f_O/32$ | | | |
| WF5025BL1*2 | 2.25 to 3.6 | Fundamental | 20 to 100 | 8 | $f_O$ | CMOS | Yes | Hi-Z |
| WF5025MLA | 2.25 to 3.6 | 3rd overtone | 70 to 80 | 8 | $f_O$ | CMOS | Yes | Hi-Z |
| (WF5025MLB) | | | 80 to 100 | | | | | |
| WF5025MLC | | | 90 to 133 | | | | | |

*1. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. The WF5025BL1 has a higher maximum operating frequency, hence the negative resistance is also larger than in the WF5025AL× devices.

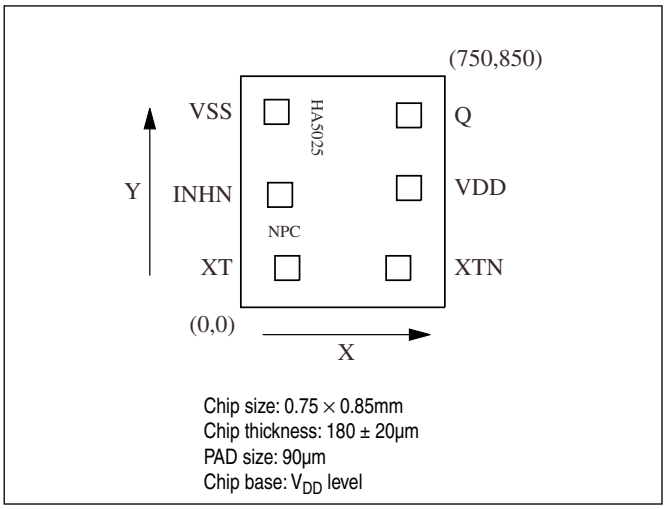
Note. These versions in parentheses ( ) are under development. Please ask our Sales & Marketing section for further detail.

## ORDERING INFORMATION

| Device | Package |
|---|---|
| WF5025×××–3 | Wafer form |

## PAD LAYOUT

(Unit: µm)

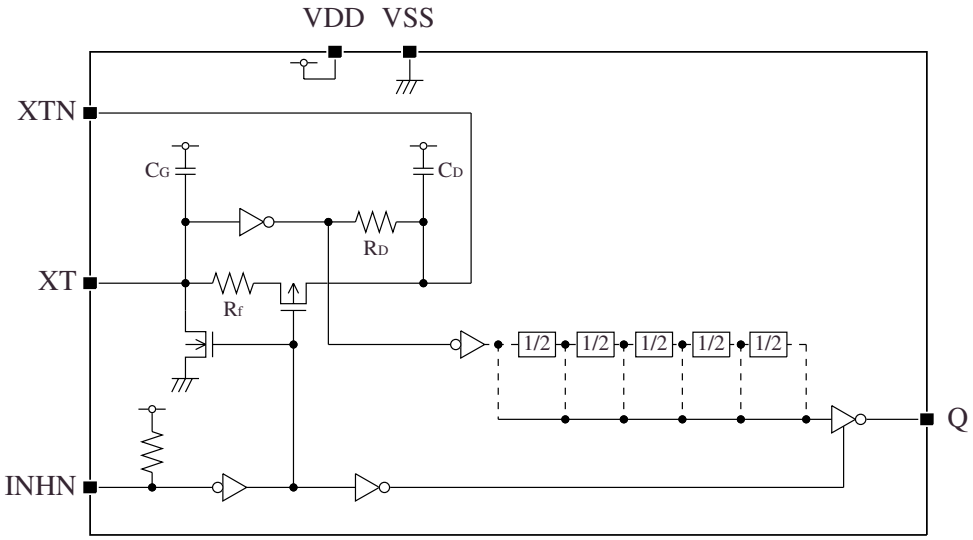



## PIN DESCRIPTION and PAD DIMENSIONS

| Name | I/O | Description | | Pad dimensions [µm] | |
|---|---|---|---|---|---|
| | | | | X | Y |
| INHN | I | Output state control input. High impedance when LOW (oscillator stops). Power-saving pull-up resistor built-in. | | 144.6 | 413.4 |
| XT | I | Amplifier input | Crystal connection pins. Crystal is connected between XT and XTN. | 171.0 | 144.6 |
| XTN | O | Amplifier output | | 579.0 | 144.6 |
| VDD | – | Supply voltage | | 618.2 | 438.6 |
| Q | O | Output. Output frequency determined by internal circuit to one of $f_O$, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$. High impedance in standby mode | | 618.2 | 705.4 |
| VSS | – | Ground | | 131.8 | 718.2 |

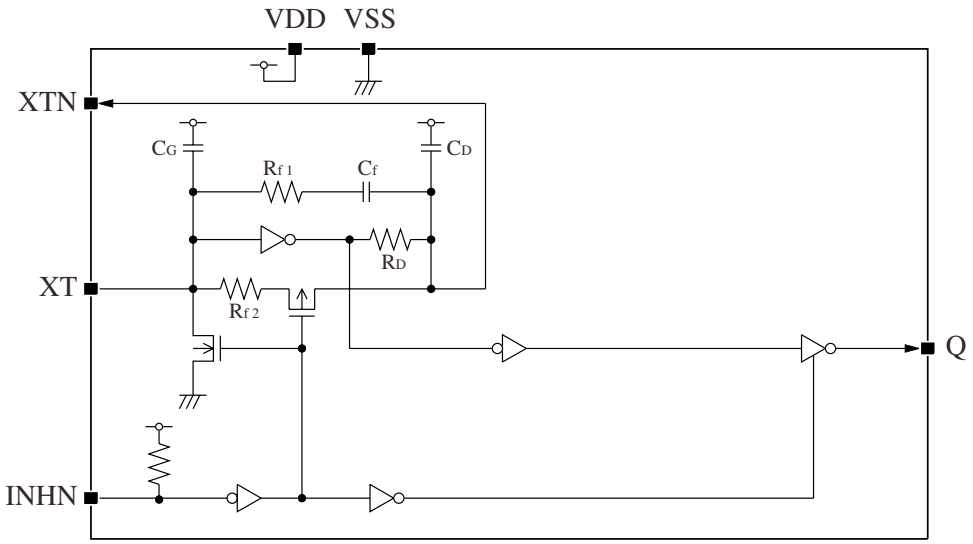
## BLOCK DIAGRAM

### For Fundamental Oscillator (WF5025AL×, WF5025BL1)




INHN = LOW active

### For 3rd Overtone Oscillator (WF5025ML×)




INHN = LOW active

# SPECIFICATIONS

## Absolute Maximum Ratings

$V_{SS}$ = 0V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | | –0.5 to +7.0 | V |
| Input voltage range | $V_{IN}$ | | –0.5 to $V_{DD}$ + 0.5 | V |
| Output voltage range | $V_{OUT}$ | | –0.5 to $V_{DD}$ + 0.5 | V |
| Operating temperature range | $T_{opr}$ | | –40 to +85 | °C |
| Storage temperature range | $T_{STG}$ | | –65 to +150 | °C |
| Output current | $I_{OUT}$ | | 20 | mA |

## Recommended Operating Conditions

$V_{SS}$ = 0V

| Parameter | Symbol | Condition | | Rating[*1] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Operating supply voltage | $V_{DD}$ | WF5025AL× | CL ≤ 30pF | 2.25 | – | 3.6 | V |
| | | WF5025BL1 | CL ≤ 30pF | 2.25 | – | 3.6 | V |
| | | WF5025MLA | f ≤ 80MHz, CL ≤ 30pF | 2.25 | – | 3.6 | V |
| | | WF5025MLB | f ≤ 100MHz, CL ≤ 30pF | (2.25) | – | (3.6) | V |
| | | WF5025MLC | f ≤ 100MHz, CL ≤ 30pF | 2.25 | – | 3.6 | V |
| | | | f ≤ 133MHz, CL ≤ 15pF | 2.25 | – | 3.6 | V |
| Input voltage | $V_{IN}$ | | | $V_{SS}$ | – | $V_{DD}$ | V |
| Operating temperature | $T_{OPR}$ | | | –40 | – | +85 | °C |
| Operating frequency[*2] | $f_O$ | WF5025AL× | | 20 | – | 50 | MHz |
| | | WF5025BL1[*3] | | 20 | – | 100 | MHz |
| | | WF5025MLA | | 70 | – | 80 | MHz |
| | | WF5025MLB[*3] | | (80) | – | (100) | MHz |
| | | WF5025MLC[*3] | | 90 | – | 133 | MHz |

*1. Values in parentheses ( ) are provisional only.

*2. The operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*3. When 2.5V operation, the ratings of switching characteristics are difference by the frequency or output load. Refer to “Switching Characteristics”.

## Electrical Characteristics

### WF5025AL× (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.25V, $I_{OH}$ = 4mA | | 1.65 | 1.95 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.25V, $I_{OL}$ = 4mA | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | 0.7$V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | – | – | 0.3$V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | $V_{OH}$ = $V_{DD}$ | – | – | 10 | µA |
| | | | $V_{OL}$ = $V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF, f = 50MHz | WF5025AL1 | – | 7 | 14 | mA |
| | | | WF5025AL2 | – | 4.5 | 9 | mA |
| | | | WF5025AL3 | – | 3.5 | 7 | mA |
| | | | WF5025AL4 | – | 2.9 | 5.8 | mA |
| | | | WF5025AL5 | – | 2.5 | 5 | mA |
| | | | WF5025AL6 | – | 2.4 | 4.8 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | – | – | 3 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | 2 | 6 | 12 | MΩ |
| | $R_{UP2}$ | | | 20 | 100 | 200 | kΩ |
| Feedback resistance | $R_f$ | Measurement cct 5 | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | 340 | 400 | 460 | Ω |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | 6.8 | 8 | 9.2 | pF |
| | $C_D$ | | | 8.5 | 10 | 11.5 | pF |

## WF5025AL× (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.7V, $I_{OH}$ = 4mA | | 2.3 | 2.4 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.7V, $I_{OL}$ = 4mA | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | 0.7$V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | – | – | 0.3$V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | $V_{OH}$ = $V_{DD}$ | – | – | 10 | µA |
| | | | $V_{OL}$ = $V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF, f = 50MHz | WF5025AL1 | – | 8.5 | 17 | mA |
| | | | WF5025AL2 | – | 5.5 | 11 | mA |
| | | | WF5025AL3 | – | 4 | 8 | mA |
| | | | WF5025AL4 | – | 3.3 | 6.6 | mA |
| | | | WF5025AL5 | – | 2.9 | 5.8 | mA |
| | | | WF5025AL6 | – | 2.7 | 5.4 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | – | – | 5 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | 2 | 4 | 8 | MΩ |
| | $R_{UP2}$ | | | 15 | 75 | 150 | kΩ |
| Feedback resistance | $R_f$ | Measurement cct 5 | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | 340 | 400 | 460 | Ω |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | 6.8 | 8 | 9.2 | pF |
| | $C_D$ | | | 8.5 | 10 | 11.5 | pF |

## WF5025BL1 (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = −40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.25V, $I_{OH}$ = 8mA | | 1.65 | 1.95 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.25V, $I_{OL}$ = 8mA | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | 0.7$V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | – | – | 0.3$V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | $V_{OH}$ = $V_{DD}$ | – | – | 10 | µA |
| | | | $V_{OL}$ = $V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF, f = 100MHz | | – | 14 | 28 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | – | – | 3 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | 2 | 6 | 12 | MΩ |
| | $R_{UP2}$ | | | 20 | 100 | 200 | kΩ |
| Feedback resistance | $R_f$ | Measurement cct 5 | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | 170 | 200 | 230 | Ω |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | 6.8 | 8 | 9.2 | pF |
| | $C_D$ | | | 8.5 | 10 | 11.5 | pF |

## WF5025BL1 (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = −40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.7V, $I_{OH}$ = 8mA | | 2.3 | 2.4 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.7V, $I_{OL}$ = 8mA | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | 0.7$V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | – | – | 0.3$V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | $V_{OH}$ = $V_{DD}$ | – | – | 10 | µA |
| | | | $V_{OL}$ = $V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF, f = 100MHz | | – | 19 | 38 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | – | – | 5 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | 2 | 4 | 8 | MΩ |
| | $R_{UP2}$ | | | 15 | 75 | 150 | kΩ |
| Feedback resistance | $R_f$ | Measurement cct 5 | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | 170 | 200 | 230 | Ω |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | 6.8 | 8 | 9.2 | pF |
| | $C_D$ | | | 8.5 | 10 | 11.5 | pF |

## WF5025ML× (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = −40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | | Rating*1 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.25V, $I_{OH}$ = 8mA | | | 1.65 | 1.95 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.25V, $I_{OL}$ = 8mA | | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | | $0.7V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | | – | – | $0.3V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | | $V_{OH} = V_{DD}$ | – | – | 10 | µA |
| | | | | $V_{OL} = V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD1}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 15pF | f = 100MHz | WF5025MLB | – | TBD | TBD | mA |
| | | | f = 133MHz | WF5025MLC | – | 15 | 30 | mA |
| | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF | f = 72MHz | WF5025MLA | – | 11 | 22 | mA |
| | | | f = 100MHz | WF5025MLB | – | TBD | TBD | mA |
| | | | f = 100MHz | WF5025MLC | – | 15 | 30 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | | – | – | 3 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | | 2 | 6 | 12 | MΩ |
| | $R_{UP2}$ | | | | 20 | 100 | 200 | kΩ |
| AC feedback resistance | $R_{f1}$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 3.99 | 4.7 | 5.41 | kΩ |
| | | | | WF5025MLB | TBD | TBD | TBD | kΩ |
| | | | | WF5025MLC | 2.97 | 3.5 | 4.03 | kΩ |
| DC feedback resistance | $R_{f2}$ | Measurement cct 5 | | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | | 85 | 100 | 115 | Ω |
| AC feedback capacitance | $C_f$ | Design value. A monitor pattern on a wafer is tested. | | | 8.5 | 10 | 11.5 | pF |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 1.70 | 2 | 2.30 | pF |
| | | | | WF5025MLB | (1.70) | (2) | (2.30) | pF |
| | | | | WF5025MLC | 0.85 | 1 | 1.15 | pF |
| | $C_D$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 3.40 | 4 | 4.60 | pF |
| | | | | WF5025MLB | (3.40) | (4) | (4.60) | pF |
| | | | | WF5025MLC | 3.40 | 4 | 4.60 | pF |

*1. Values in parentheses ( ) are provisional only.

## WF5025ML× (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | | Rating*1 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| HIGH-level output voltage | $V_{OH}$ | Q: Measurement cct 1, $V_{DD}$ = 2.7V, $I_{OH}$ = 8mA | | | 2.3 | 2.4 | – | V |
| LOW-level output voltage | $V_{OL}$ | Q: Measurement cct 2, $V_{DD}$ = 2.7V, $I_{OL}$ = 8mA | | | – | 0.3 | 0.4 | V |
| HIGH-level input voltage | $V_{IH}$ | INHN | | | $0.7V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | INHN | | | – | – | $0.3V_{DD}$ | V |
| Output leakage current | $I_Z$ | Q: Measurement cct 2, INHN = LOW | | $V_{OH} = V_{DD}$ | – | – | 10 | µA |
| | | | | $V_{OL} = V_{SS}$ | – | – | 10 | µA |
| Current consumption | $I_{DD1}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 15pF | f = 100MHz | WF5025MLB | – | TBD | TBD | mA |
| | | | f = 133MHz | WF5025MLC | – | 20 | 40 | mA |
| | $I_{DD2}$ | Measurement cct 3, load cct 1, INHN = open, $C_L$ = 30pF | f = 72MHz | WF5025MLA | – | 15 | 30 | mA |
| | | | f = 100MHz | WF5025MLB | – | TBD | TBD | mA |
| | | | f = 100MHz | WF5025MLC | – | 20 | 40 | mA |
| Standby current | $I_{ST}$ | Measurement cct 3, INHN = LOW | | | – | – | 5 | µA |
| INHN pull-up resistance | $R_{UP1}$ | Measurement cct 4 | | | 2 | 4 | 8 | MΩ |
| | $R_{UP2}$ | | | | 15 | 75 | 150 | kΩ |
| AC feedback resistance | $R_{f1}$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 3.99 | 4.7 | 5.41 | kΩ |
| | | | | WF5025MLB | TBD | TBD | TBD | kΩ |
| | | | | WF5025MLC | 2.97 | 3.5 | 4.03 | kΩ |
| DC feedback resistance | $R_{f2}$ | Measurement cct 5 | | | 50 | – | 150 | kΩ |
| Oscillator amplifier output resistance | $R_D$ | Design value. A monitor pattern on a wafer is tested. | | | 85 | 100 | 115 | Ω |
| AC feedback capacitance | $C_f$ | Design value. A monitor pattern on a wafer is tested. | | | 8.5 | 10 | 11.5 | pF |
| Built-in capacitance | $C_G$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 1.70 | 2 | 2.30 | pF |
| | | | | WF5025MLB | (1.70) | (2) | (2.30) | pF |
| | | | | WF5025MLC | 0.85 | 1 | 1.15 | pF |
| | $C_D$ | Design value. A monitor pattern on a wafer is tested. | | WF5025MLA | 3.40 | 4 | 4.60 | pF |
| | | | | WF5025MLB | (3.40) | (4) | (4.60) | pF |
| | | | | WF5025MLC | 3.40 | 4 | 4.60 | pF |

*1. Values in parentheses ( ) are provisional only.

## Switching Characteristics

### WF5025AL× (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | $C_L$ = 15pF | – | 3 | 6 | ns |
| | $t_{r2}$ | | $C_L$ = 30pF | – | 5 | 10 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | $C_L$ = 15pF | – | 3 | 6 | ns |
| | $t_{f2}$ | | $C_L$ = 30pF | – | 5 | 10 | ns |
| Output duty cycle*1 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, f = 50MHz | $C_L$ = 15pF | 45 | – | 55 | % |
| | Duty2 | | $C_L$ = 30pF | 45 | – | 55 | % |
| Output disable delay time*2 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, $C_L$ = 15pF | | – | – | 100 | ns |
| Output enable delay time*2 | $t_{PZL}$ | | | – | – | 100 | ns |

*1. The duty cycle characteristic is checked the sample chips of each production lot.
*2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

### WF5025AL× (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | $C_L$ = 15pF | – | 2.5 | 5 | ns |
| | $t_{r2}$ | | $C_L$ = 30pF | – | 4.5 | 9 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | $C_L$ = 15pF | – | 2.5 | 5 | ns |
| | $t_{f2}$ | | $C_L$ = 30pF | – | 4.5 | 9 | ns |
| Output duty cycle*1 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, f = 50MHz | $C_L$ = 15pF | 45 | – | 55 | % |
| | Duty2 | | $C_L$ = 30pF | 45 | – | 55 | % |
| Output disable delay time*2 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, $C_L$ = 15pF | | – | – | 100 | ns |
| Output enable delay time*2 | $t_{PZL}$ | | | – | – | 100 | ns |

*1. The duty cycle characteristic is checked the sample chips of each production lot.
*2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

## WF5025BL1 (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating min | Rating typ | Rating max | Unit |
|---|---|---|---|---|---|---|---|
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | $C_L$ = 15pF | – | 2 | 4 | ns |
| | $t_{r2}$ | | $C_L$ = 30pF | – | 3 | 6 | ns |
| | $t_{r3}$ | Measurement cct 3, load cct 1, 0.2$V_{DD}$ to 0.8$V_{DD}$ | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | $C_L$ = 15pF | – | 2 | 4 | ns |
| | $t_{f2}$ | | $C_L$ = 30pF | – | 3 | 6 | ns |
| | $t_{f3}$ | Measurement cct 3, load cct 1, 0.8$V_{DD}$ to 0.2$V_{DD}$ | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output duty cycle*1 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C | $C_L$ = 15pF f = 100MHz | 45 | – | 55 | % |
| | Duty2 | | $C_L$ = 30pF f = 80MHz | 45 | – | 55 | % |
| | Duty3 | | $C_L$ = 30pF f = 100MHz | 40 | – | 60 | % |
| Output disable delay time*2 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, $C_L$ = 15pF | | – | – | 100 | ns |
| Output enable delay time*2 | $t_{PZL}$ | | | – | – | 100 | ns |

*1. The duty cycle characteristic is checked the sample chips of each production lot.
*2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

## WF5025BL1 (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | Rating min | Rating typ | Rating max | Unit |
|---|---|---|---|---|---|---|---|
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | $C_L$ = 15pF | – | 1.5 | 3 | ns |
| | $t_{r2}$ | | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | $C_L$ = 15pF | – | 1.5 | 3 | ns |
| | $t_{f2}$ | | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output duty cycle*1 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, f = 100MHz | $C_L$ = 15pF | 45 | – | 55 | % |
| | Duty2 | | $C_L$ = 30pF | 45 | – | 55 | % |
| Output disable delay time*2 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, $C_L$ = 15pF | | – | – | 100 | ns |
| Output enable delay time*2 | $t_{PZL}$ | | | – | – | 100 | ns |

*1. The duty cycle characteristic is checked the sample chips of each production lot.
*2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

## WF5025ML× (2.5V operation)

$V_{DD}$ = 2.25 to 2.75V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | | Rating*1 min | Rating*1 typ | Rating*1 max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | | $C_L$ = 15pF | – | 2 | 4 | ns |
| | $t_{r2}$ | | | $C_L$ = 30pF | – | 3 | 6 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | | $C_L$ = 15pF | – | 2 | 4 | ns |
| | $t_{f2}$ | | | $C_L$ = 30pF | – | 3 | 6 | ns |
| Output duty cycle*2 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, $C_L$ = 15pF | f = 72MHz | WF5025MLA | 45 | – | 55 | % |
| | | | f = 100MHz | WF5025MLB | (45) | – | (55) | % |
| | | | f = 133MHz | WF5025MLC | 45 | – | 55 | % |
| | Duty2 | Measurement cct 3, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, $C_L$ = 30pF | f = 72MHz | WF5025MLA | 45 | – | 55 | % |
| | | | f = 100MHz | WF5025MLB | (40) | – | (60) | % |
| | | | f = 100MHz | WF5025MLC | 40 | – | 60 | % |
| Output disable delay time*3 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 2.5V, Ta = 25°C, $C_L$ = 15pF | | | – | – | 100 | ns |
| Output enable delay time*3 | $t_{PZL}$ | | | | – | – | 100 | ns |

*1. Values in parentheses ( ) are provisional only.
*2. The duty cycle characteristic is checked the sample chips of each production lot.
*3. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

## WF5025ML× (3.0V operation)

$V_{DD}$ = 2.7 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C unless otherwise noted.

| Parameter | Symbol | Condition | | | Rating*1 min | Rating*1 typ | Rating*1 max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output rise time | $t_{r1}$ | Measurement cct 3, load cct 1, 0.1$V_{DD}$ to 0.9$V_{DD}$ | | $C_L$ = 15pF | – | 1.5 | 3 | ns |
| | $t_{r2}$ | | | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output fall time | $t_{f1}$ | Measurement cct 3, load cct 1, 0.9$V_{DD}$ to 0.1$V_{DD}$ | | $C_L$ = 15pF | – | 1.5 | 3 | ns |
| | $t_{f2}$ | | | $C_L$ = 30pF | – | 2.5 | 5 | ns |
| Output duty cycle*2 | Duty1 | Measurement cct 3, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, $C_L$ = 15pF | f = 72MHz | WF5025MLA | 45 | – | 55 | % |
| | | | f = 100MHz | WF5025MLB | (45) | – | (55) | % |
| | | | f = 133MHz | WF5025MLC | 45 | – | 55 | % |
| | Duty2 | Measurement cct 3, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, $C_L$ = 30pF | f = 72MHz | WF5025MLA | 45 | – | 55 | % |
| | | | f = 100MHz | WF5025MLB | (45) | – | (55) | % |
| | | Measurement cct 3, load cct 1, $V_{DD}$ = 3.3V, Ta = 25°C, $C_L$ = 30pF, f = 100MHz | | WF5025MLC | 45 | – | 55 | % |
| Output disable delay time*3 | $t_{PLZ}$ | Measurement cct 6, load cct 1, $V_{DD}$ = 3.0V, Ta = 25°C, $C_L$ = 15pF | | | – | – | 100 | ns |
| Output enable delay time*3 | $t_{PZL}$ | | | | – | – | 100 | ns |

*1. Values in parentheses ( ) are provisional only.
*2. The duty cycle characteristic is checked the sample chips of each production lot.
*3. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

# FUNCTIONAL DESCRIPTION

## Standby Function

When INHN goes LOW, the oscillator stops and the oscillator output on Q becomes high impedance.

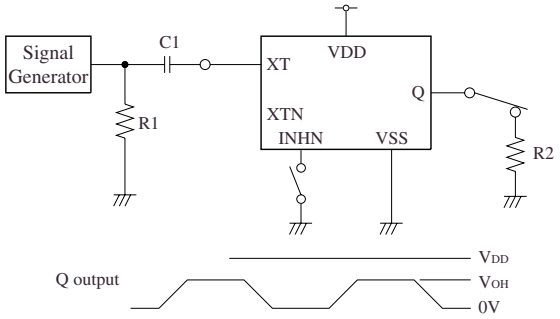
| Version | INHN | Q | Oscillator |
|---|---|---|---|
| WF5025AL× | HIGH (or open) | Any $f_O$, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$ or $f_O/32$ output frequency | Normal operation |
| WF5025BL1, ML× | | $f_O$ | |
| WF5025AL×, BL1, ML× | LOW | High impedance | Stopped |

## Power-save Pull-up Resistor

The INHN pull-up resistance changes in response to the input level (HIGH or LOW). When INHN goes LOW (standby state), the pull-up resistance becomes large to reduce the current consumption during standby.

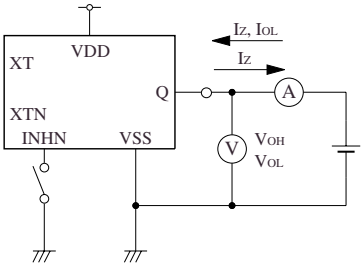
# MEASUREMENT CIRCUITS

## Measurement cct 1

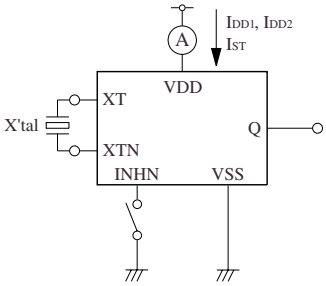



2Vp-p, 10MHz sine wave input signal
C1: 0.001µF
R1: 50Ω
R2: 5025AL× : 412Ω (2.5V operation)
575Ω (3.0V operation)
5025BL1, ML× : 206Ω (2.5V operation)
287Ω (3.0V operation)

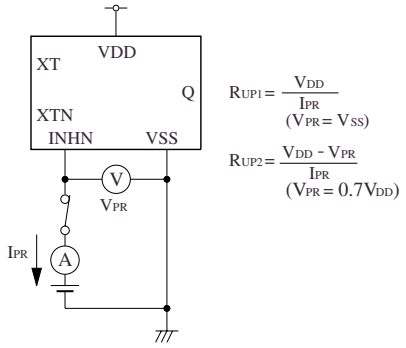
## Measurement cct 2



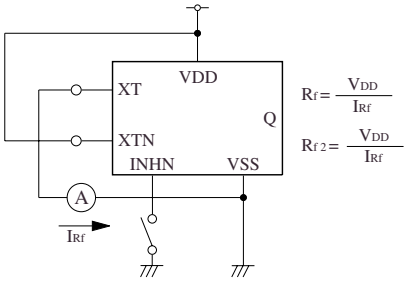

## Measurement cct 3



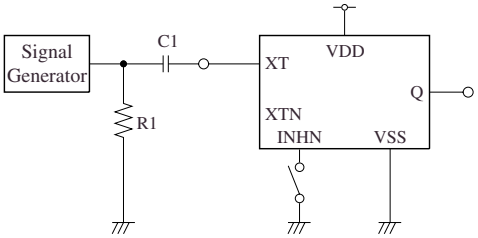

## Measurement cct 4




## Measurement cct 5

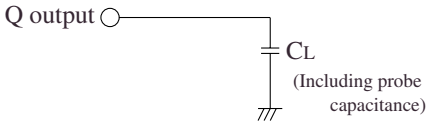



## Measurement cct 6



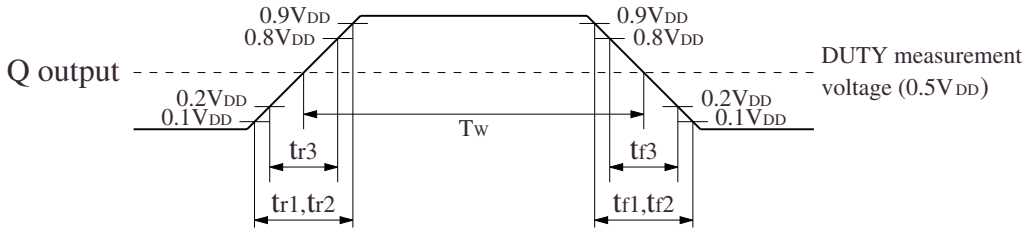

2Vp-p, 10MHz sine wave input signal
C1: 0.001µF
R1: 50Ω

## Load cct 1

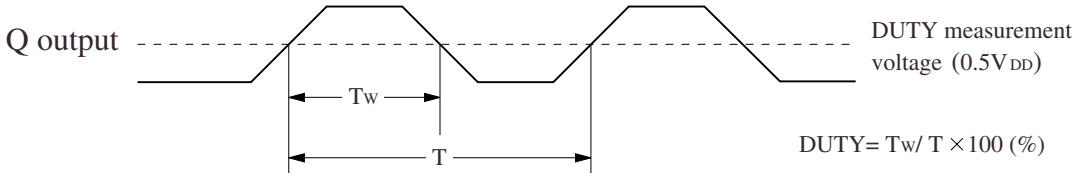


## Switching Time Measurement Waveform

### Output duty level, $t_r$, $t_f$

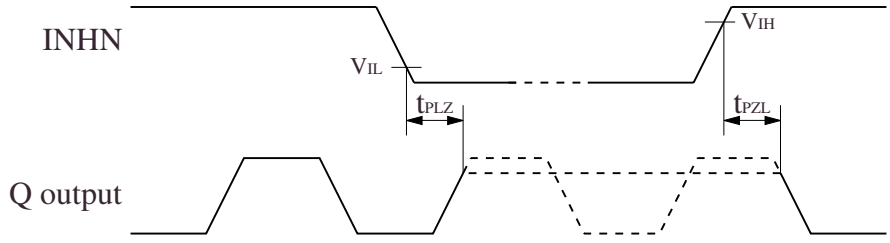



### Output duty cycle




## Output Enable/Disable Delay

when the device is in standby, the oscillator stops. When standby is released, the oscillator starts and stable oscillator output occurs after a short delay.




INHN input waveform tr = tf ≤ 10ns

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