GEC PLESSEY
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ADVANCE INFORMATION
DS4054-2.2

WL100
WLAN INTERFACE CIRCUIT

The WL100, together with the DE6003 frequency hopping radio transceiver, implements a wide variety of WLAN applications where NRZ encoding is used.

FEATURES
- Low Power CMOS Technology
- Flexible Data Transceiver
- Clock Recovery with Continuous Calibration for Flexible Packet Length
- Flexible Preamble Format
- Selectable Data Rates: 156·25kb/s, 250kb/s, 312·5kb/s, 500kb/s, 625kb/s and 1Mb/s
- CRC-32 Generator/Checker
- Fast Antenna Diversity with Manual Override
- Battery Level Monitoring
- 8-Bit Parallel Controller Interface

RELATED DOCUMENTS
DE6003 data sheet, DS3506
GPS application notes AN142,143,144,145, 154 and 203 for further design information.

ORDERING INFORMATION
WL100/CG/FP1R - Commercial, Quad Plastic Flatpack
Prior to completion of full device characterisation, pre-production parts will be designated **WL100/PR/FP1R.**

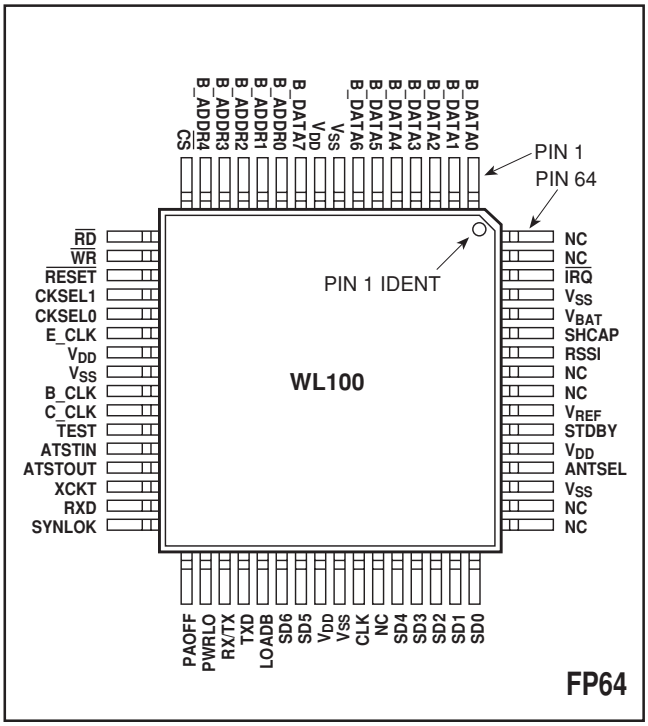


Fig. 1 Pin connections (top view). See Table 8 for pin descriptions.

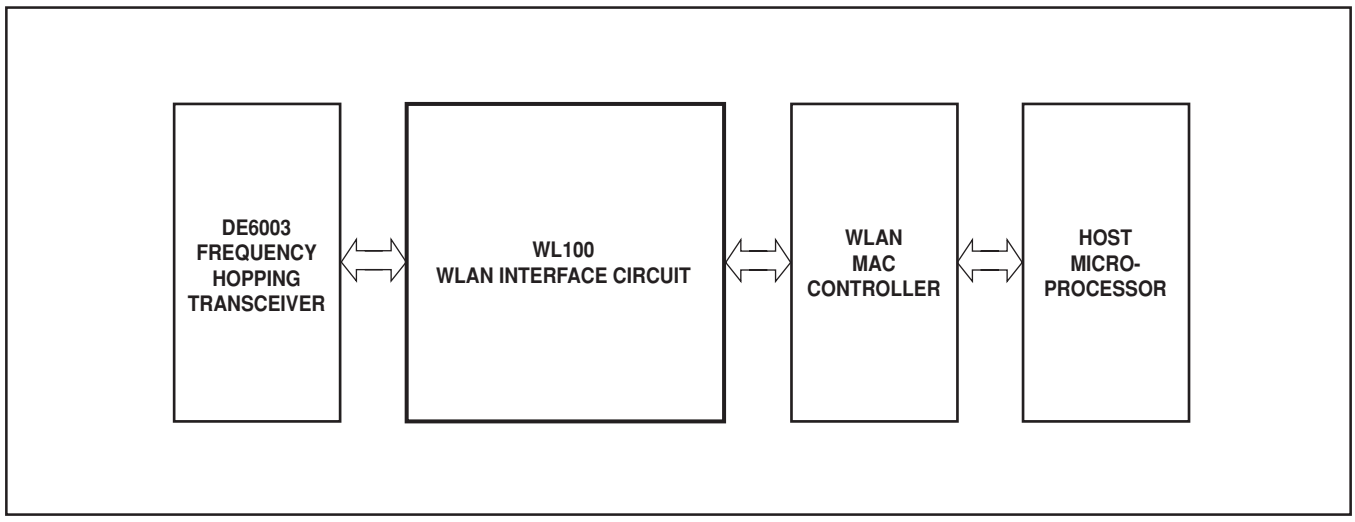


Fig. 2 WLAN system block diagram

GENERAL FUNCTIONALITY

Fig. 4 shows the WL100 Block Diagram and its interaction with the DE6003 and a generic WLAN Media Access Controller (MAC) layer Controller, referred to in the following text as the Controller. The format of a generic data burst/packet that the WL100 receives on the RXD line is shown in Fig. 3. On the radio side, the WL100 conforms to the DE6003 specifications. On the Controller side the WL100 conforms to the general 8-bit Controller external bus specifications. All WL100 registers are accessed by the Controller through the 8-bit B_DATA bus. A typical Controller I/O read/write timing is shown in Fig. 15.

There are five types of registers internal to the WL100 which the Controller can access via the B_DATA bus: Control Registers (write only), Status Registers (read only), Configuration registers (write only), FIFO (read/write) and Data Length Registers (write only).

The Controller uses the control registers to initiate a particular WL100 function. The bit definitions for the WL100 control registers are shown in Fig. 5.

The status registers are used to inform the Controller about the WL100 and DE6003 status. Fig. 6 shows the bit definitions for the WL100 status registers. The Controller makes the decision about a channel status according to the table in Fig. 6.

Fig. 7 shows the 16×8 receive/transmit FIFO and the data length register. The FIFO buffers the data going to/coming from the Controller and provides an uninterrupted data flow between the WL100 and DE6003 at different data rates and system clock speeds. The data length register is used for the CRC calculations during data receive.

The configuration registers are shown in Figs. 8 and 9. They give flexibility to the WL100 so that it can be used in a number of different system applications. Configuration registers can be written to only when the Commence Diversity (CD), Commence Transmission (CT), Commence Reception (CR) and Commence Hopping (CH) bits in a WL100 control register are inactive (high).

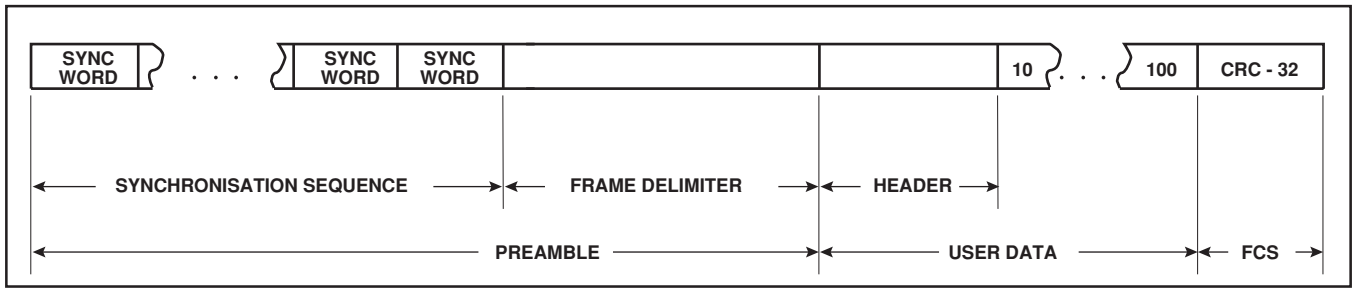


Fig 3 Generic data burst/packet format

Start address	End address	Description
00	02	Control registers
03	-	Unused
04	07	Status registers
08	0B	Unused
0C	-	FIFO
0D	0F	Unused
10	1A	Configuration registers
1B	-	Unused
1C	1D	Data length registers
1E	1F	Unused

Table 1

Table 1 shows how the WL100 registers are mapped into its address space.

The Controller activates the WL100 each time it wants to scan the channel, receive data from the channel or transmit data over it. Prior to the start of a transmit or a receive function, the WL100 will drive the control signals to put the radio in a required mode of operation, according to the DE6003 specification.

The Controller is responsible for updating the frequency control register (Fig.5, ADDR 01), maintaining minimum time between consecutive transmissions, maximum continuous transmit time, radio standby to transmit time, frequency hopping time for transmit and for receive and timely loading of the data length register (Fig. 7, ADDR 1C and1D) for the CRC function.

In the transmit direction, the WL100 receives the user data in 8-bit words from the Controller bus and converts it into a serial data stream. After a preamble sequence has been transmitted, the WL100 calculates CRC, does bit stuffing and transmits a data stream to the radio, appending the CRC at the end. Both transmit and receive data is buffered by the FIFO.

In the receive direction, the WL100 receives a serial NRZ data stream from the radio, strips the preamble, removes the stuffed bits, generates the CRC, converts the serial data into 8-bit words and sends it to the Controller. Once all data have been received, the WL100 checks CRC and writes four CRC bytes into the FIFO in case the Controller needs to read them.

If the WL100 cannot recover the synchronisation sequence within a predefined time, it returns a channel status to the Controller.

BLOCK DIAGRAM DESCRIPTION

Receive/Transmit State Machine

The Receive/Transmit state machine controls the WL100-to-DE6003 interface and is responsible for the receive/transmit control timing, transmit power amplifier control timing, transmitter power level control and channel load pulse timing.

To hop to a new frequency, the CH bit (Fig. 5, ADDR 01, bit 7) has to be set to 0. As a result, a negative LOADB pulse is generated and will load the frequency data SD (0:6) (Fig. 5, ADDR 01, bits 0 to 6) into the DE6003. The Controller does not need to reset the CH bit as the WL100 carries this out as part of the channel select sequence.

To start data transfer, the Controller must set the CT bit to 0 (Fig.5, ADDR 00, bit 4). When all transmit data has been read by the WL100, the CT bit must be reset to 1.

Preamble Generator

A preamble is generated for every transmit data burst sent to the DE6003 on TXD. The preamble is fully programmable (see Fig. 8, ADDR 12 and ADDR 13, bits 0:2 for a sync word bit pattern, ADDR18 for the number of transmitted sync words, and ADDR 13, bits 3:7 and ADDR 14 to 17 for the frame delimiter bit pattern).

Bit Stuffing

The Bit Stuffing logic examines the data stream to the radio and inserts an altered polarity bit relative to the last bit in a selected bit group. A number of bits in a group can be programmed (see Fig. 9, ADDR 19, bits 6 and 7). The DE6003 requires at least one transition after every 16 bit times at 625kb/s data rate to assure adequate bit error rate performance. Thus, to break long sequences of ones or zeros at 312kb/s, bit stuffing after

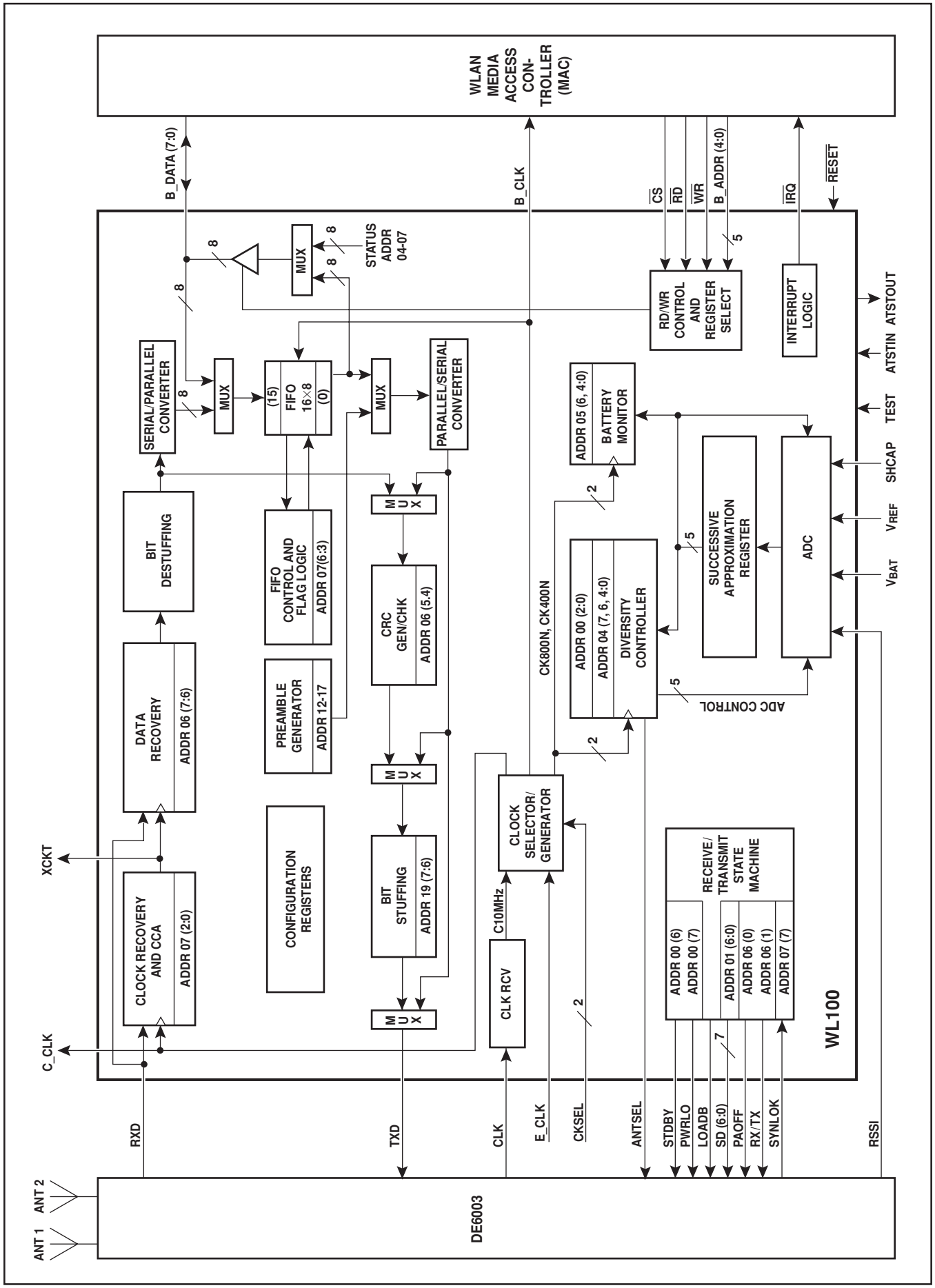


Fig. 4 WL100 chip block diagram

8 bits will be required and for 156kb/s, bit stuffing after 4 bits will be needed. The WL100 performs bit stuffing for user data only. Preamble fields must be selected by a user in a way that a maximum number of consecutive ones or zeros is not violated. Bit stuffing also helps to distinguish between long strings of ones or zeros in a valid data stream and a clear channel (no data and no noise) by the Clear Channel Assessment (CCA) logic.

Bit Destuffing

The Bit Destuffing logic monitors a data sequence from the Data Recovery logic and strips the bits inserted by the bit stuffing logic of the transmitter.

Serial-to-Parallel Converter

This transforms a serial data stream from the bit destuffing logic into parallel byte-wide format and sends it to the FIFO.

FIFO

The FIFO a 16×8, fall-through type. During receive operation it buffers the data coming from the Serial-to-Parallel Converter and makes it available for the Controller to read over the B_DATA bus. During transmit operation it buffers the data coming from the B_DATA bus and makes it available to the Parallel-to-Serial Converter.

FIFO Control and Flag Logic

The FIFO Control and Flag logic controls data flow through the FIFO. Almost Full (AF) and Almost Empty (AE) flags (Fig. 6, ADDR 07, bits 3 and 4) are programmable by FL 0 and FL1(Fig. 9, ADDR 1A, bits 5 and 6) and can be monitored by the Controller as well as Read and Write error indication bits (Fig. 6, ADDR 07, bits 5 and 6). A Read error is caused by attempting to read from the FIFO when it is empty; a Write error is caused by attempting to write to the FIFO when it is full.

Full and Empty flags are also provided (Fig. 6, ADDR 06, bits 2 and 3). All bits are set on the negative edge of the C_CLK clock.

Parallel-to-Serial Converter

The Parallel-to-Serial Converter transforms parallel byte-wide data from the FIFO or from the Preamble Generator to a serial bit stream. The data from the FIFO is sent to the CRC Generator and Bit Stuffing logic. The preamble is sent directly to the TXD output of the chip.

CRC Generator/Checker

The WL100 performs this optional function if instructed to do so by the Controller (see Fig. 5, ADDR 02, bit 1). CRC is generated according to IEEE-802 standard 32-bit AUTODIN-II polynomial.

During transmit the WL100 does not need to know the user data byte count and will automatically append CRC when the CT bit (Fig. 5, ADDR 00, bit 4) is high and the FIFO becomes empty.

During receive the Controller has to provide the WL100 with the data length information (Fig. 7, ADDR 1C and ADDR 1D) some time before the end of a frame to let the WL100 know when to check CRC.

Clock Recovery and Clear Channel Assessment (CCA)

The Clock Recovery and CCA logic recovers the data clock XCKT from the RXD data stream, provides recovered clock to the Data Recovery logic, and determines if the channel is busy or free to transmit. The WL100 starts recovering clock each time the CR bit (Fig. 5, ADDR 00, bit 3) is set low by the Controller. It must stay low for the whole time of CCA or data receive function.

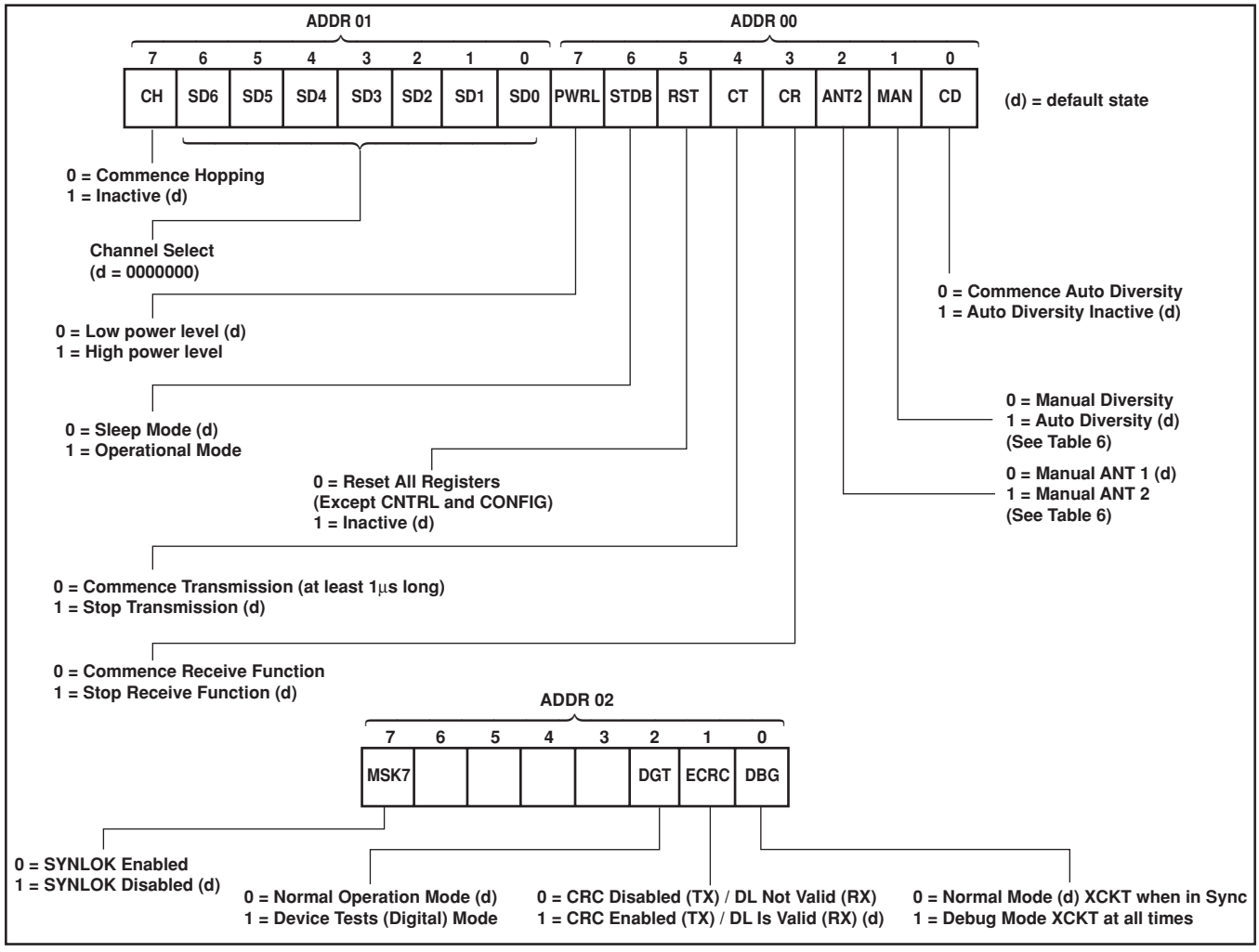


Fig. 5 Control registers (write only)

After the time limit for the synchronisation has expired, the syncdone (SYDN) bit is set (Fig. 6, ADDR 07, bit 2) and interrupt to the controller is generated. At this time the Controller can make a decision about the channel status by examining noise (NS) and long sequence (LONG) bits (Fig. 6, ADDR 07, bits 1 and 0).

Clock Recovery and CCA logic requires 16:1 ratio for an oversampling clock C_CLK. Table 7 shows the oversampling clock rate required for particular selected data transfer rates.

Data Recovery Logic

The Data Recovery logic detects the sequence of sync words and the frame delimiter in the data stream supplied by the Clock Recovery logic according to the Sync Word and Frame Word configuration (see Fig. 8, ADDR 12 and ADDR 14 -17) and separates it from the User Data. If NS or LONG bits (ADDR 07, bits 1 and 0) have been set, the WL100 stops searching for sync sequence. The Controller might choose to poll these bits to get early indication of a free channel prior to expiration of Syncdone Timer.

Once the sync sequence has been detected, the SYNC bit (see Fig. 6, ADDR 06, bit 6) goes high and remains high until the end of the data reception. The FRM bit (see Fig. 6, ADDR 06, bit 7) goes high when a frame delimiter has been detected and stays on until the end of data reception.

Read/Write Control and Register Select

The Read/Write Control and Register Select logic controls the bidirectional B_DATA bus and selects the WL100 registers during the Controller-initiated read and write operations.

Interrupt Logic

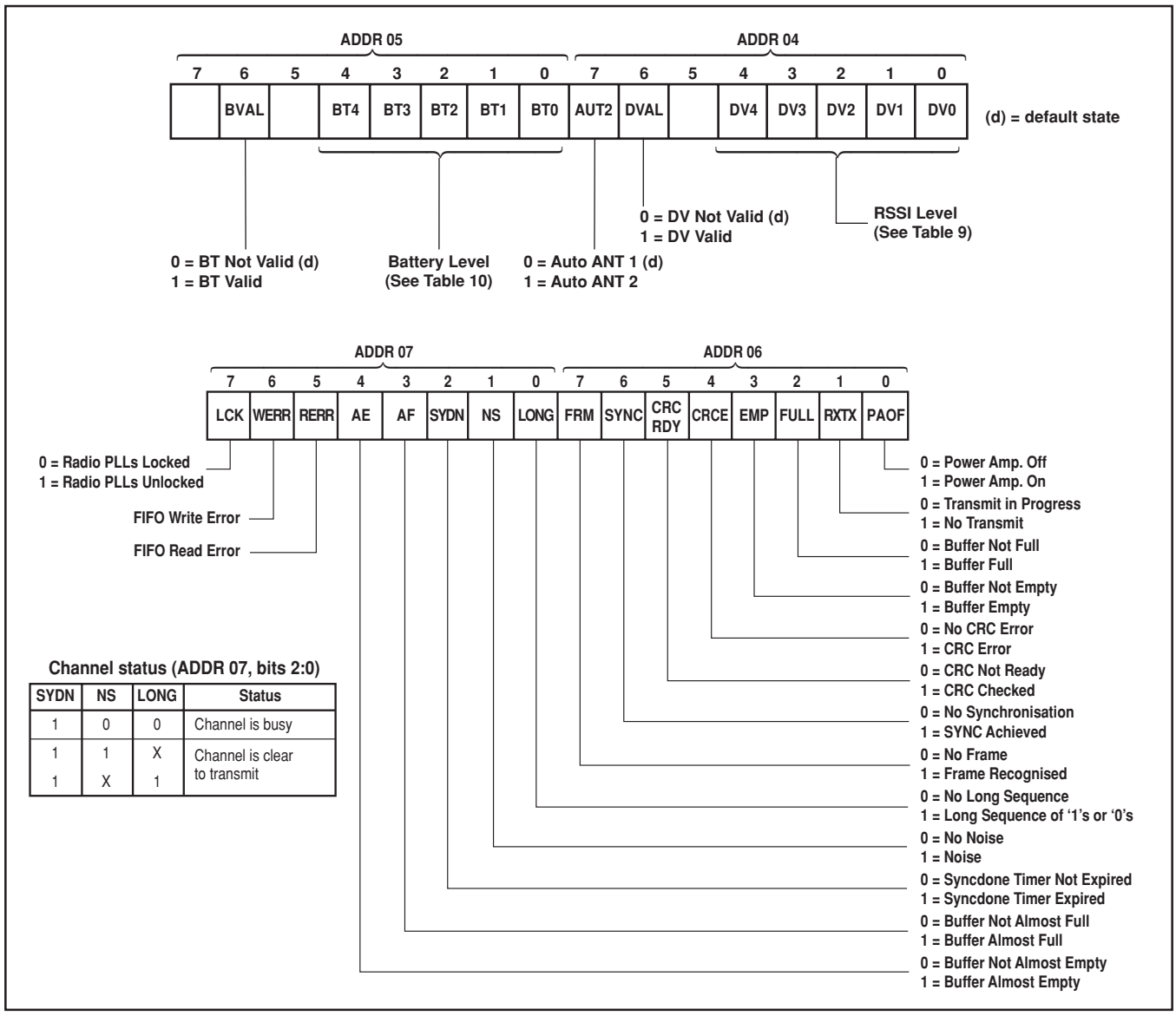
Interrupt logic generates interrupt requests to the Controller when a certain WL100 status has to be reported. At that time, IRQ becomes low and stays low until reset. Table 2 lists all cases when the WL100 generates interrupts together with corresponding interrupt reset conditions.

Radio Synthesiser Unlocked interrupt can be disabled by setting the MSK7 bit high (Fig. 5, ADDR 02, bit 7).

Diversity Controller

The Diversity Controller automatically selects the optimum antenna during receive operations. To start auto diversity, the Controller has to set the auto diversity bit (Fig. 5, ADDR 00, bit 0) low, which has to stay low for at least 1µs, when it can be switched back to high at any time before another diversity function is to be initiated. The circuit performs diversity by comparing the Receive Signal Strength Indication (RSSI) energy levels from both antennas and selecting the one which yields the higher level.

The Diversity Switch can also be controlled manually (Fig. 5, ADDR 00, bits 1 and 2). The RSSI level can be checked at any time by auto operation of the diversity (see Fig. 6, ADDR 04).



Channel status (ADDR 07, bits 2:0)

SYDN	NS	LONG	Status
1	0	0	Channel is busy
1	1	X	Channel is clear to transmit
1	X	1	

Fig. 6 Status registers (read only)

Battery Monitor

The Battery Monitor (input V_{BAT}) allows relative estimation of the remaining operating time for the user in battery-powered applications. Both the Diversity Controller and the Battery Monitor use as an input a digital representation of analog RSSI and battery voltage levels from the 5-bit succesive approximation ADC. The Battery Monitor status register value is updated whenever an auto diversity function is performed (Fig. 6, ADDR 05).

CLK RCV

CLK RCV is a 10MHz low level clock amplifier. An analog circuit, it transforms the nominal ±1 mA square wave current, CLK, from the DE6003 into a digital CMOS level clock.

Clock Selector/Generator

The Clock Selector/Generator selects the clock source for the WL100 (C10MHz clock from the CLK RCV or E_CLK from an external clock oscillator). It supplies the system clock B_CLK for the Controller, C_CLK clock for the Clock Recovery and CCA logic, and CK400N and CK800N clock for the Diversity Controller and the Battery Monitor. Fig. 14 shows the details of the Clock Selector/Generator logic. For DR(2:0) bit settings see Fig. 9, ADDR 19, bits 2:0. Note that, for correct operation, the Receive/Transmit state machine, the Diversity Controller and the Battery Monitor require 10MHz clock. So even if an external oscillator with a clock rate other than 10MHz is used, the low level 10MHz CLK from the DE6003 is still required. When the STDB bit (ADDR 00, bit 6) is reset to '0', all WL100 clocks are disabled except for the control registers and configuration registers clocks; B_CLK clock output also remains active.

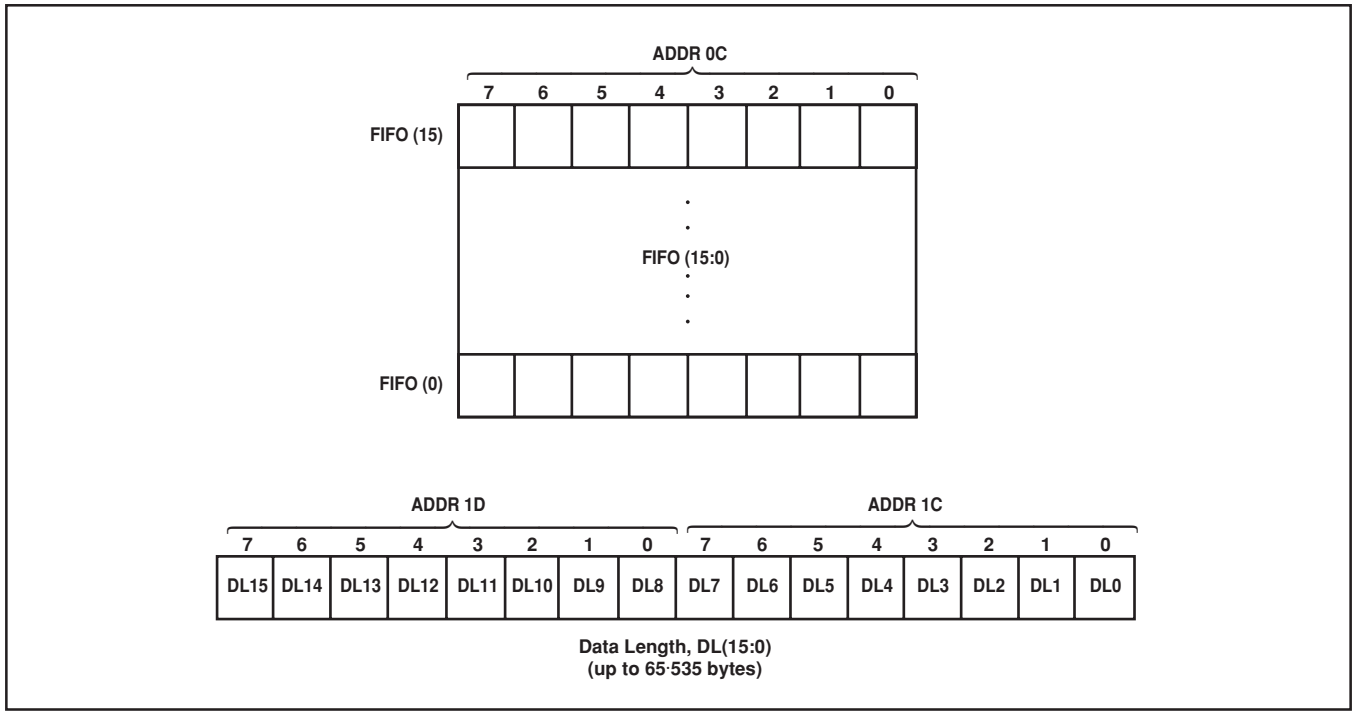


Fig. 7 Data register (FIFO) and data length registers (read/write)

Interrupt	Reset condition	Note
FIFO read error (ADDR 07, bit 5)	RST control bit (ADDR 00, bit 5)	1
FIFO write error (ADDR 07, bit 6)	RST control bit (ADDR 00, bit 5)	1
FIFO almost full (ADDR 07, bit 03)	When the condition is cleared	1
FIFO almost empty (ADDR 07, bit 04)	When the condition is cleared	1
Syncdone Timer expired (ADDR 07, bit 2)	When CR goes high (ADDR 00, bit 3)	2
Radio synthesiser unlocked (ADDR 07, bit 7)	When the condition is cleared	3
CRC ready (ADDR 06, bit 5)	When CRC is read by the Controller or when CR goes high (ADDR 00, bit 3)	1

Table 2 WL100 interrupts

NOTES
1. Set on the negative edge of B_CLK
2. Set on the negative edge of C_CLK
3. Set on the negative edge of 10MHz

CONFIGURATION REGISTERS

Tables 3, 4, and 5, together with Figs. 8 and 9, describe the configuration registers of the WL100.

Table 3 describes the configuration registers that control Clock Recovery and CCA; Table 4 describes the registers controlling the Preamble Generator and Data Recovery mechanism and Table 5 describes other programmable resources.

Bits	Register	Definition	Fig.
JT (1:0)	ADDR 1A	Jitter tolerance for the incoming data (maximum deviation from an ideal pulse. when pulse is still considered valid). Three options.	9
NT (1:0)	ADDR 1A	Noise tolerance (number of occurrences of invalid data until the noise flag is raised). Four options.	9
BS (1:0)	ADDR 19	Bit stuffing algorithm. Four options.	9

Table 3 Clock Recovery and CCA configuration registers

Bits	Register	Definition	Fig.
TSW (7:0)	ADDR 18	Number of Sync Words to be transmitted.	9
BSW (2:0)	ADDR 13	Number of bits in a Sync Word.	8
SW (7:0)	ADDR 12	Sync Word bit pattern.	8
NSW (2:0)	ADDR 19	Number of Sync Words to be recovered before the Receiver is considered to be in sync with the Transmitter.	9
BE (0)	ADDR 1A	Indicates if single bit errors are allowed before Frame Delimiter after synchronisation has been achieved.	9
BFW (4:0)	ADDR 13	Number of bits in the Frame Delimiter.	9
FW(31:0)	ADDR 14, 15, 16, 17	Frame Delimiter bit pattern.	8

Table 4 Configuration registers controlling the Preamble Generator and the Data Recovery mechanism

Bits	Register	Definition	Fig.
ST (15:0)	ADDR 10,11	Time limit for achieving synchronisation (0-2^{16} C_CLK clock cycles).	8
DR(2:0)	ADDR 19	Specifies required oversampling clock rate.	9
FL(1:0)	ADDR 1A	Specifies thresholds for Almost Full and Almost Empty FIFO flags.	9

Table 5 Other programmable resources

Function	MAN (ADDR 00, bit 1)	ANTSEL (pin 52)
Manual	0	ANT 2 (ADDR 00, bit 2)
Auto	1	AUT 2 (ADDR 04, bit 7)

Table 6 Antenna selection table

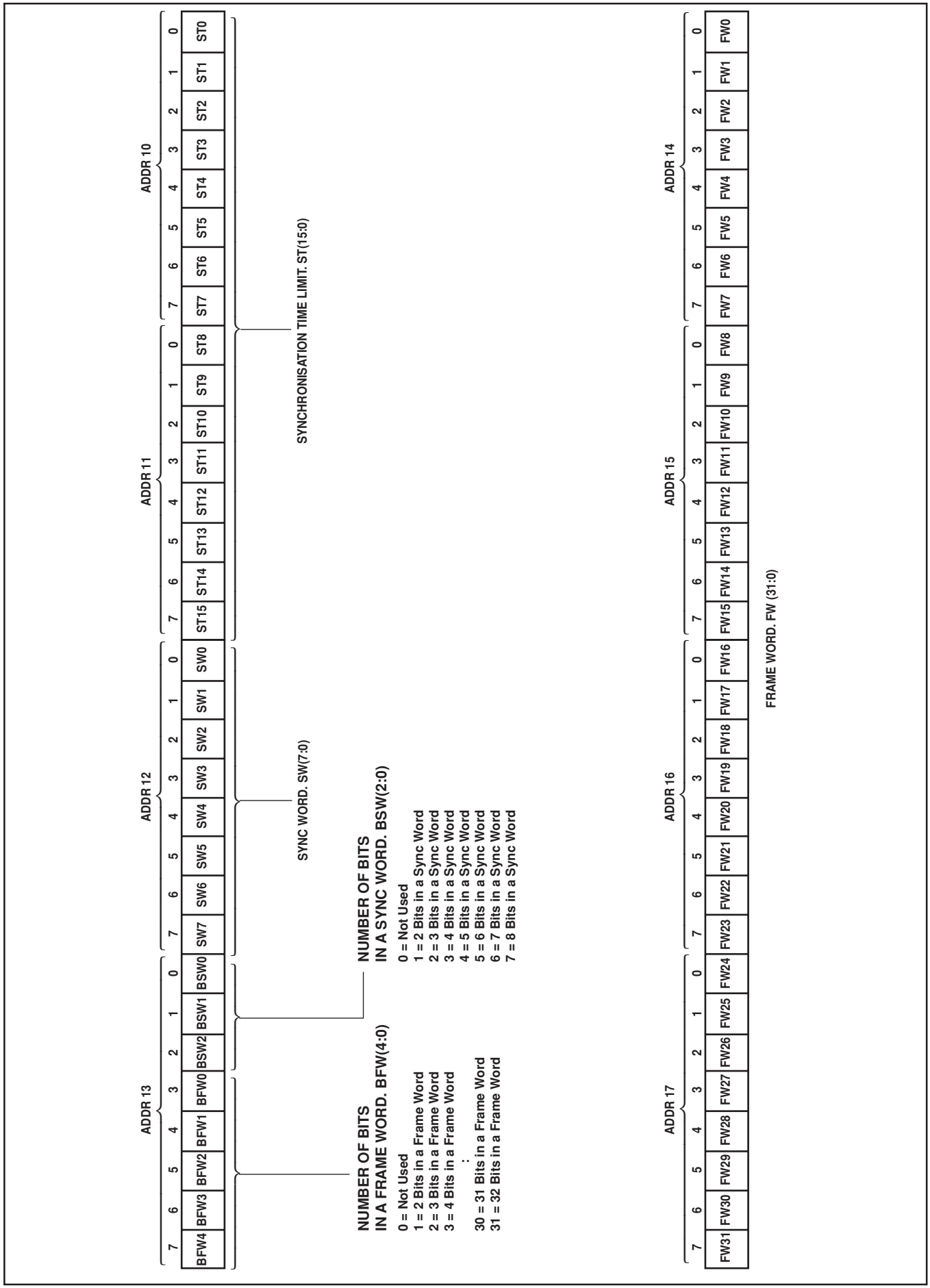


Fig. 8 Configuration registers ADDR 10 through ADDR 17

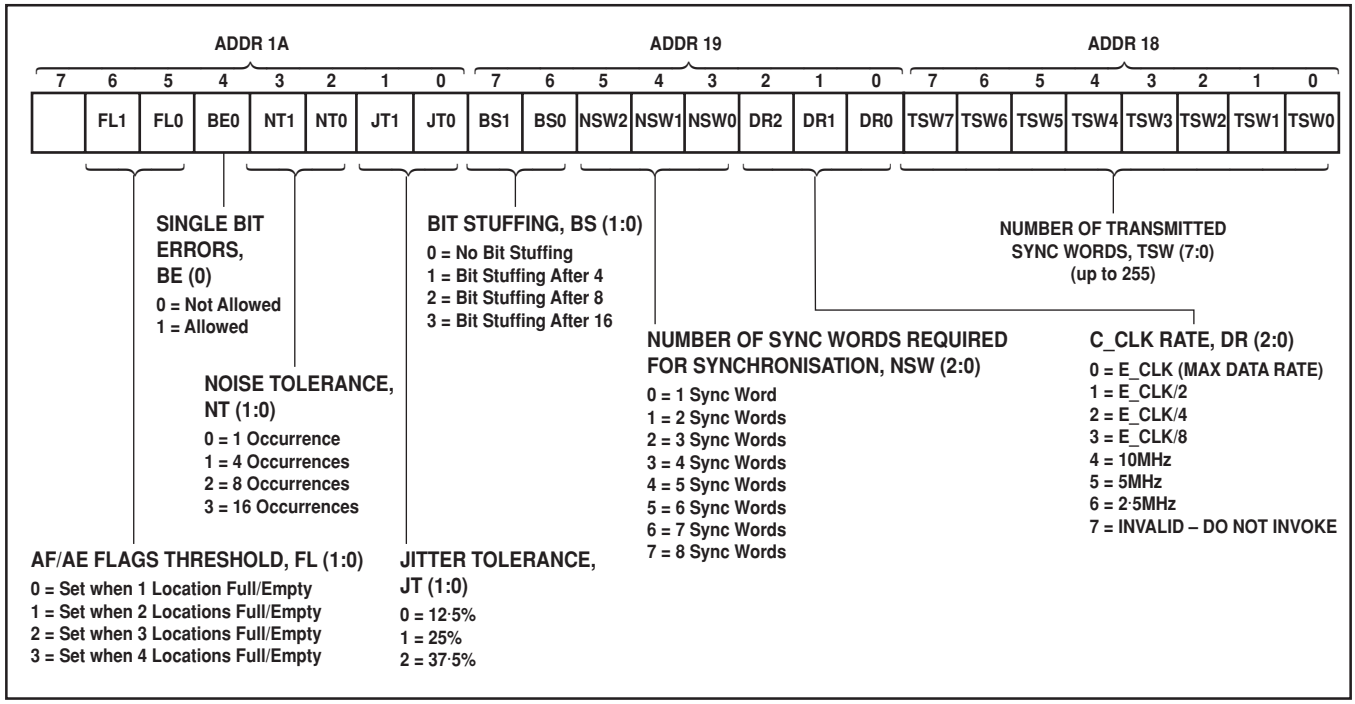


Fig. 9 Configuration registers ADDR 18, ADDR 19 and ADDR 1A

FLOW DIAGRAMS

Figs. 10 through 13 are flow diagrams for a channel hop, antenna diversity and battery monitoring, channel sense, data receive and data transmit functions.

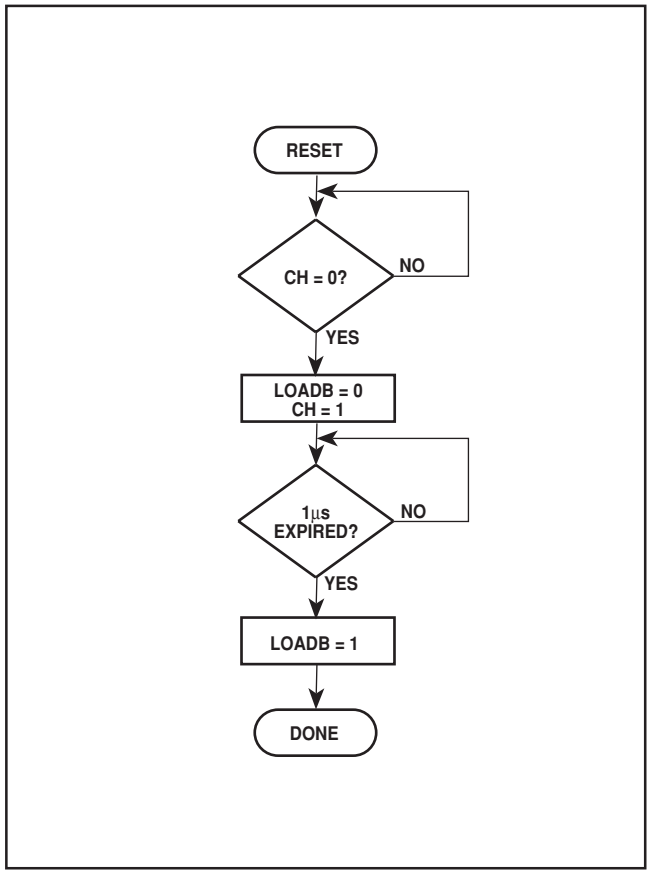


Fig. 10 Channel selection

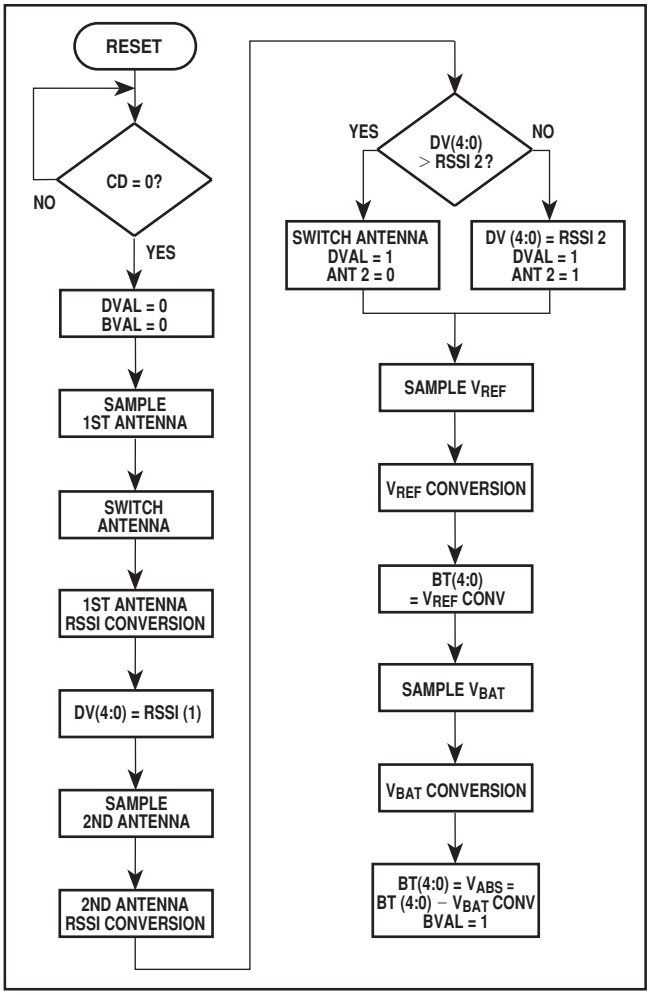


Fig. 11 Antenna diversity and battery monitoring

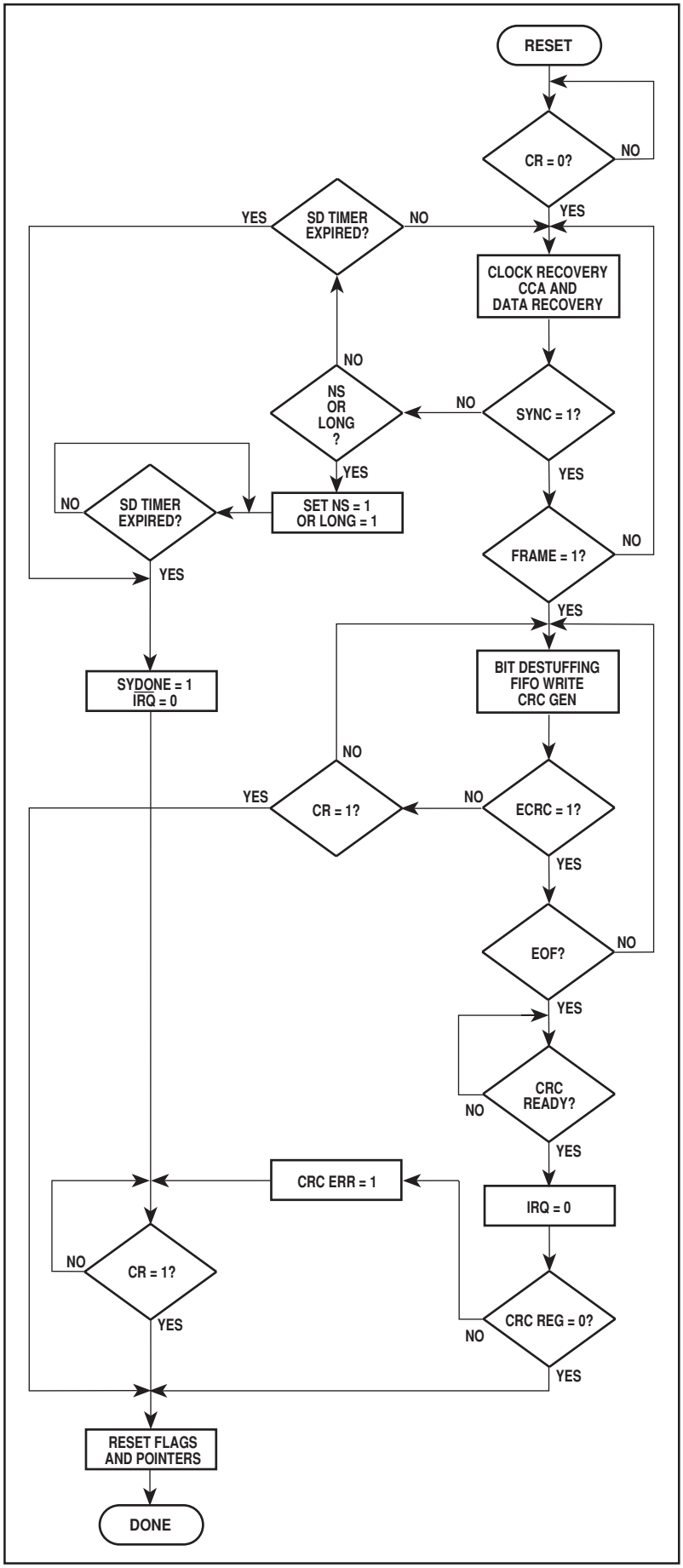


Fig. 12 Channel sense and data receive

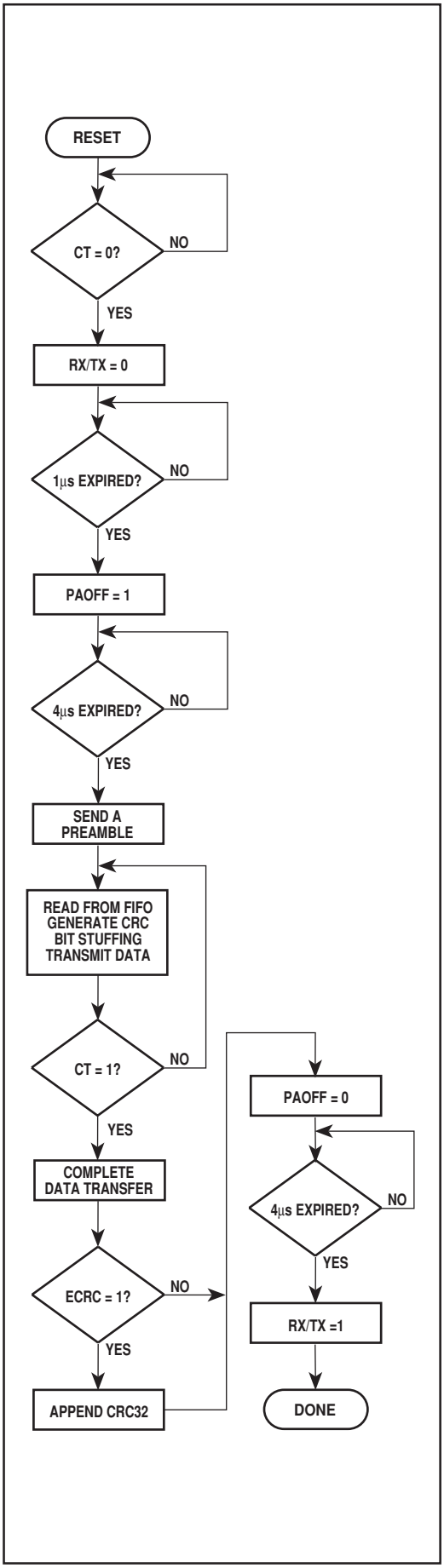


Fig. 13 Data transmit

CLOCK SELECTOR/GENERATOR

Fig. 14 shows the logic of the clock selector/generator. C_CLK rate conntrol bits DR (0:2) are bits 0 through 2 of configuration register ADDR 18 (0:2). Table 7 gives clock rates for data rates from 156·25 kb/s to 1000kb/s.

NOTES

* External oscillator is not required if CLK is used. If both CLK and E_CLK are used, any system clock rate up to 32MHz can be obtained.

** CLK is required in addition to E_CLK to ensure correct DE6003 timing.

*** Represents a minimum E_CLK rate. E_CLK = C_CLK×N (not to exceed 32MHz) can be used if a higher system clock rate is required. Clock must be confirmed with internal clock.

Data rate (kb/s)	Required*** oversampling clock rate C_CLK (MHz)	System clock rate B_CLK (MHz)
1000	16	32/16/10/8/4**
625*	10	10*
500	8	32/16/10/8/4/2**
312·5*	5	10*
250	4	32/16/10/8/4/2/1**
156·25*	2·5	10*

Table 7

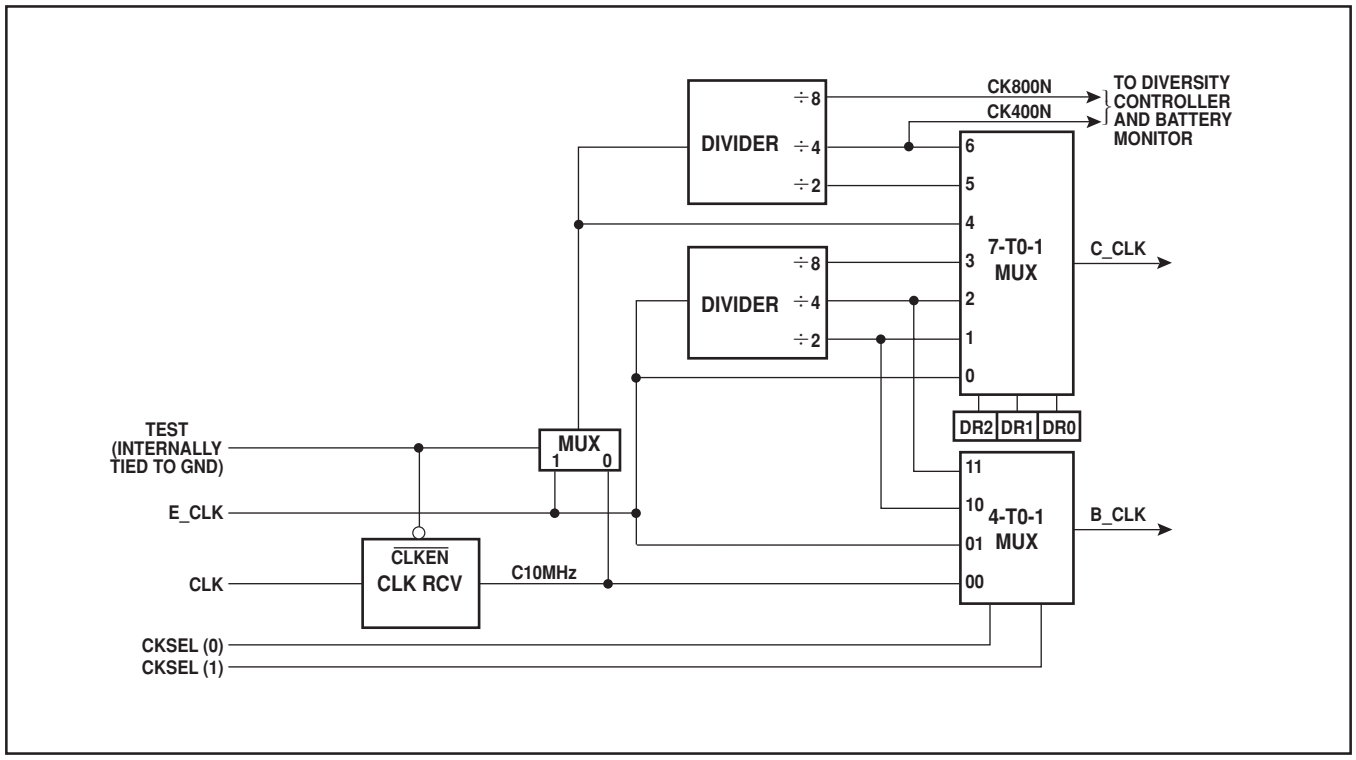


Fig. 14 Clock selector/generator

WL100 CLOCK SPEED.

The WL100 is designed to operate with one or two clock sources CLK and E_CLK.

CLK is primarily used tor oversampling of the data at 625, 312.5 or156.25 kb/s. In addition, the CLK signal is required for operation of the DE6003 control signals.

If an external clock signal (E_CLK) other than 10MHz is used then the CLK clock input must still have a 10MHz clock applied from the DE6003 in order for the DE6003 interface timing to be correct.

Timing problems can also arise if the MAC controller uses a different clock source other than the one used to generate B_CLK. If this is the case and asynchronous clocks are used, the signals from the MAC controller should be re-timed with B_CLK (see Fig. 17)

E_CLK allows the WL100 to be interfaced to microcontrollers with different data bus clock speeds. CLK, supplied from the DE6003, is still required for proper DE6003 control signal timing. The maximum clock speed for E_CLK is 32 MHz.

The B_CLK rate is programmable and is based on the E_CLK rate (see Fig 14).

Pin	Pin	Type	Description
1	B_DATA0	I/O	Data Bus, bit 0
2	B_DATA1	I/O	Data Bus, bit 1
3	B_DATA2	I/O	Data Bus, bit 2
4	B_DATA3	I/O	Data Bus, bit 3
5	B_DATA4	I/O	Data Bus, bit 4
6	B_DATA5	I/O	Data Bus, bit 5
7	B_DATA6	I/O	Data Bus, bit 6
10	B_DATA7	I/O	Data Bus, bit 7
8,24,41,51,61	V_{SS}	GND	Ground
9,23,40,53	V_{DD}	+5V	Positive supply
11	B_ADDR0	I	Address Bus, bit 0
12	B_ADDR1	I	Address Bus, bit 1
13	B_ADDR2	I	Address Bus, bit 2
14	B_ADDR3	I	Address Bus, bit 3
15	B_ADDR4	I	Address Bus, bit 4
16	CS	I	Chip select (active low)
17	RD	I	Read cycle (active low)
18	WR	I	Write cycle (active low)
19	RESET	I	Power on reset (active low)
20	CKSEL1	I	Clock source select, bit 1
21	CKSEL0	I	Clock source select, bit 0
22	E_CLK	I	External clock, 100 ppm stability
25	B_CLK	O	System clock output
26	C_CLK	O	Oversampling clock (test output)
27	TEST	I	Device test, normally tied to GND
28	ATSTIN	I	Used for a device test, internally tied to GND
29	ATSTOUT	O	Used for a device test
30	XCKT	O	Recovered or transmit clock (test output)
31	RXD	I	Receive data input
32	SYNLOK	I	Lock monitor (locked when low)
33	PAOFF	O	Turns off transmit power amp. (active low)
34	PWRLO	O	Power level control (low when zero)
35	RX/TX	O	Controls the radio mode (receive when high)
36	TXD	O	Transmit data output
37	LOADB	O	Channel select load pulse (active low)
38	SD6	O	Channel select code, bit 6
39	SD5	O	Channel select code, bit 5
44	SD4	O	Channel select code, bit 4
45	SD3	O	Channel select code, bit 3
46	SD2	O	Channel select code, bit 2
47	SD1	O	Channel select code, bit 1
48	SD0	O	Channel select code, bit 0
42	CLK	A	10MHz low level clock from DE6003
43,49,50,56,57,63,64	NC		No connection
52	ANTSEL	O	Diversity switch control (Selects ANT1 when low)
54	STDBY	O	Standby mode (active low)
55	V_{REF}	A	Reference voltage 1·23V
58	RSSI	A	Receive signal strength indicator (0V to 5V range, 0·4V to 2·4V linear)
59	SHCAP	A	Sample and hold capacitor input (requires external 50pF capacitor to ground)
60	V_{BAT}	A	Battery voltage, 2·8V to 5·0V range (requires external 1kΩ series resistor)
62	IRQ	OD	Interrupt to the Controller (active low). Requires a 10kΩ pullup resistor to drive the signal high.

Table 8 WL100 pin descriptions

NOTES
I = Input to WL100
O = Output from WL100
OD = Output from WL100 with external pull-up resistor
A = Analog input

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated: T_{AMB} = 0°C to +70°C, V_{DD} = 5V±10%

Static Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CLK					
Input impedance			300	Ω	
Bias		2·5		V	
Input current	0·25	1·0	1·6	mA	
All Other Inputs					
Input voltage low			0·8	V	
Input voltage high	2·0			V	
CKSEL (1:0), E_CLK, TEST, ATSTIN					
Input current		1·25		mA	$V_{IN} = V_{DD}$
All Other Inputs					
Input current			±1	µA	$V_{IN} = V_{DD}$ or V_{SS}
All Outputs					
Output voltage low		0·2	0·4	V	I_{OL} = 6mA
Output voltage high	0·8V_{DD}	0·9V_{DD}		V	I_{OH} = −6mA
RXD, E_CLK					
Input hysteresis, rising		3·1		V	V_{IL} to V_{IH}
Input hysteresis, falling		1·9		V	V_{IH} to V_{IL}
IRQ					
Leakage current			±1	µA	$V_{OUT} = V_{DD}$ or V_{SS}
All Outputs					
Short circuit current	67	135	270	mA	$V_{DD} = V_{OUT}$ = +5·5V
	37	75	150	mA	V_{DD} = +5·5V, V_{OUT} = 0V
Operating Current		1		µA/MHz	Excluding peripheral buffers
All Inputs					
Input capacitance		3		pF	Excluding package leadframe capacitance of bidirectional pins
All Outputs					
Output capacitance		4		pF	Excluding package leadframe capacitance of bidirectional pins
All Bidirectional Pins					
Capacitance		5		pF	Excluding package leadframe
Power Supply					
Current			40	mA	Transmit/Receive at 625kb/s
			5	mA	Standby (STDB = 0)
V_{BAT}					
Voltage range (full)	2·8		5·0	V	
Voltage range (linear)	2·8		3·7	V	

Dynamic Characteristics (see Figs. 15 and 16)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Data rate		156·25		1000	kb/s	
Jitter tolerance				37·5	%	
IRQ low to FIFO full/empty				160	B_CLK cycles	C_CLK (MHz) to B_CLK (MHz) = 4:1, FL = 3
ADC linearity, accuracy			0·5		LSB	V_{REF} = 1·23V
ADC conversion time				2	µs	
RSSI input range		0·4		2·4	V	V_{REF} = 1·23V
B_CLK frequency		1		32	MHz	
I/O address to RD low	(t_1)	25			ns	See Fig. 15
RD low to valid data	(t_2)			16	ns	See Fig. 15
B_DATA set-up to WR low	(t_3)	0			ns	See Fig. 15
I/O address to WR	(t_4)	25			ns	See Fig. 15
RD duration	(t_5)	2			B_CLK cycles	See Fig. 15
WR duration	(t_6)	2			B_CLK cycles	See Fig. 15
DE6003 channel hop time	(t_7)		80		µs	See Fig. 16 and Note 1
LOADB pulse width	(t_8)	1			µs	See Fig. 16
Diversity decision time	(t_9)			9·6	µs	See Fig. 16
RX/TX low to PAOFF high	(t_{10})	1			µs	See Fig. 16
PAOFF high to transmit data	(t_{11})	4			µs	See Fig. 16
PAOFF low to RX/TX high	(t_{12})	4			µs	See Fig. 16
WR to B_DATA hold time	(t_{13})	20			ns	See Fig. 15
RD to B_DATA hold time	(t_{14})	14			ns	See Fig. 15

NOTE 1. Channel hop time, t_7, is specified here as 80µs (typ.) to be consistent with DE6003 requirements.

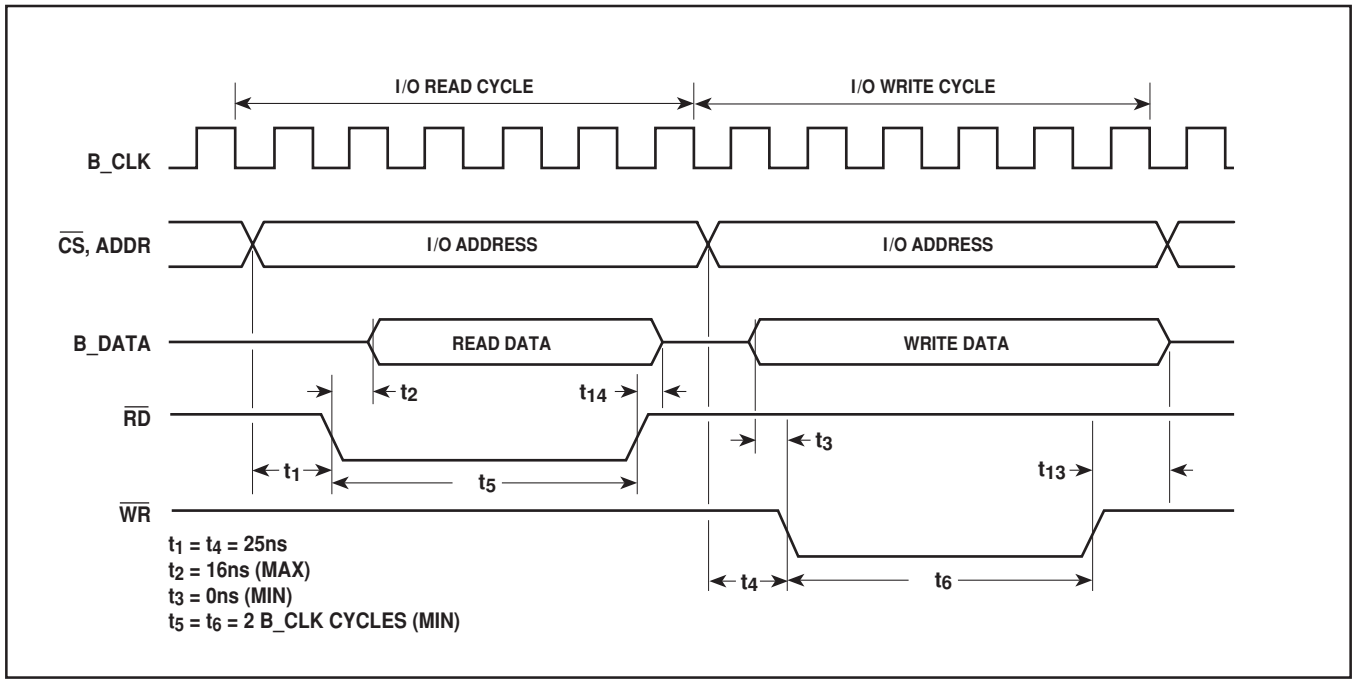


Fig. 15 Typical controller bus timing

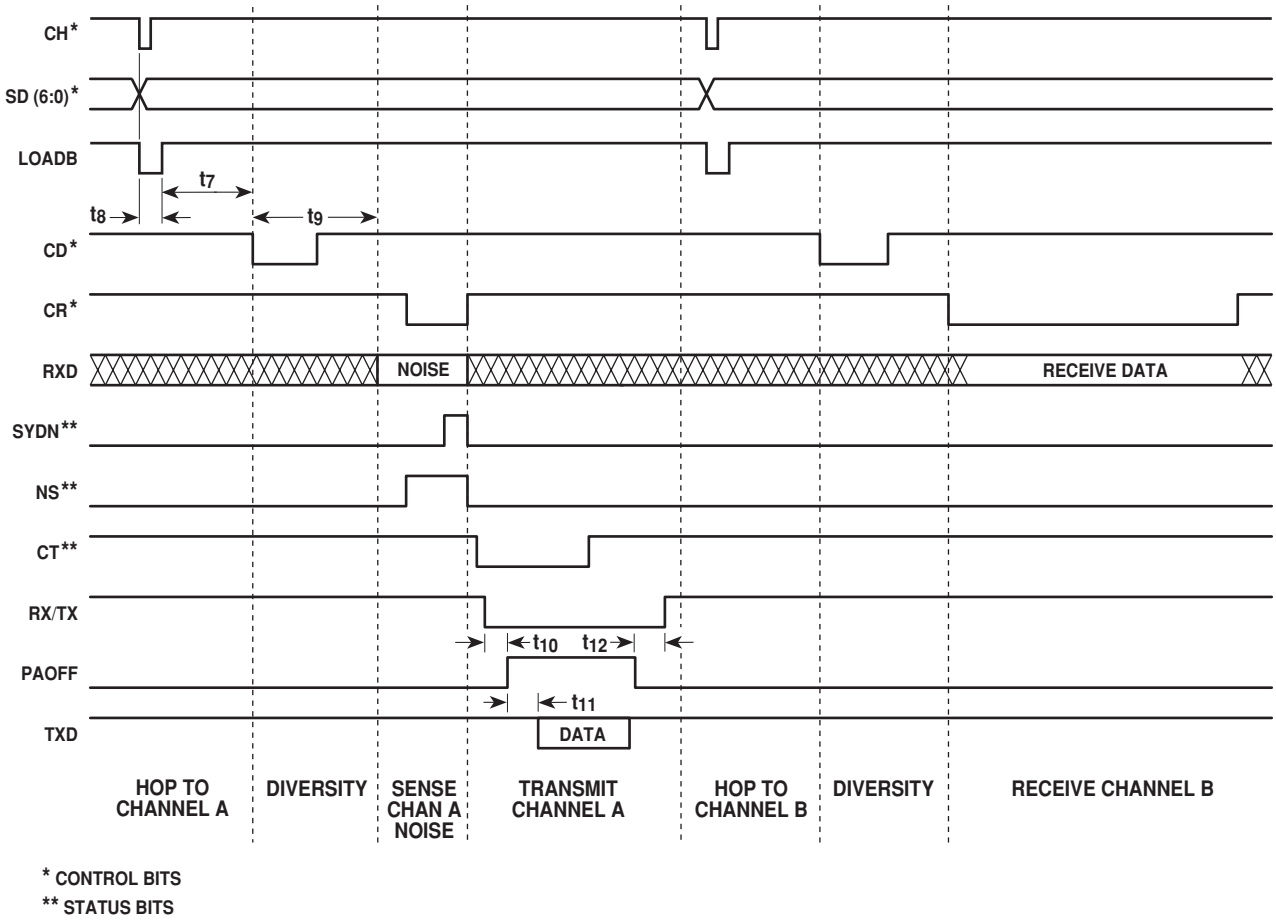
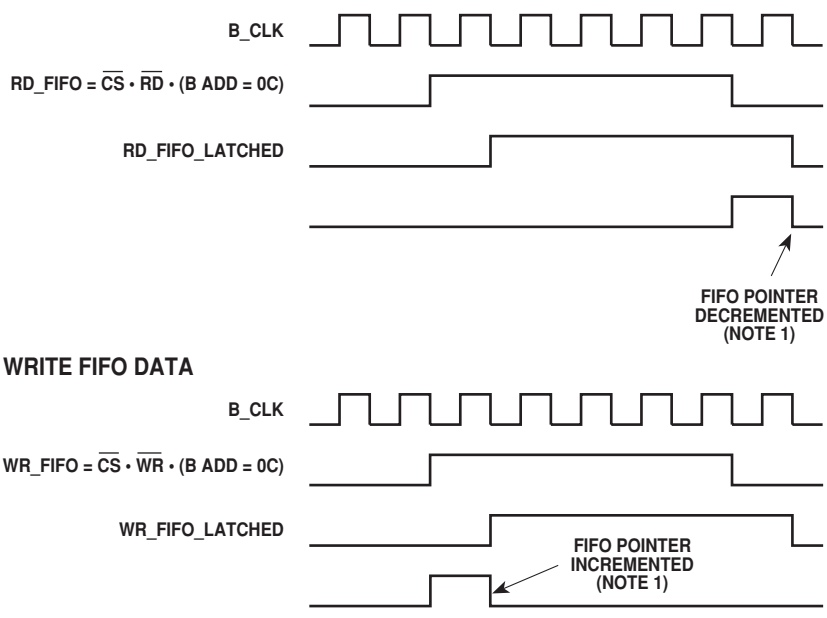
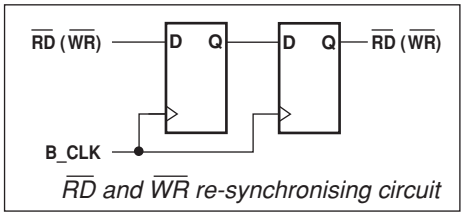


Fig. 16 Timings for WL100 primary operation modes (not to scale)



Note 1.
In asynchronous systems, when the system clock differs from the ones specified in Table 7, the width of these pulses may become negligible and the FIFO will fail to increment/decrement. To avoid these race hazards all controller to WL100 signals could be re-synchronised to B_CLK, but this would take a large amount of hardware. In most applications re-synchronising the read/write strobes should be sufficient, the relationship between the delayed and re-synchronised $\underline{RD}$ and $\underline{WR}$ strobes to $\underline{CS}$, ADDR and DATA should be checked. A re-synchronising circuit is shown below.



$\overline{RD}$ and $\overline{WR}$ re-synchronising circuit

Fig. 17 Read and Write synchronising

RSSI (V)	DV (4:0)	RSSI (V)	DV (4:0)	RSSI (V)	DV (4:0)	RSSI (V)	DV (4:0)
0·00	00000	0·58	01000	1·20	10000	1·82	11000
0·03	00001	0·65	01001	1·27	10001	1·89	11001
0·11	00010	0·73	01010	1·35	10010	1·97	11010
0·19	00011	0·81	01011	1·43	10011	2·05	11011
0·27	00100	0·89	01100	1·51	10100	2·13	11100
0·36	00101	0·96	01101	1·58	10101	2·20	11101
0·42	00110	1·04	01110	1·66	10110	2·28	11110
0·50	00111	1·12	01111	1·74	10111	2·36	11111

Table 9 RSSI values

NOTE : Variation in RSSI values between DE6003 transceivers can be up to 5dB.

V_{BAT} (V)	BT (4:0)	BT (4:0)
<2·83	-	Non-linear
2·83	00101	
2·92	00110	
3·00	00111	
3·07	01000	
3·15	01001	
3·22	01010	±200mV
3·30	01011	
3·37	01100	
3·45	01101	
3·52	01110	
3·60	01111	
3·67	10000	
>3·75	-	Non-linear

Table 10 Battery level monitoring values

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