

## DESCRIPTION

The WM2152 is a high speed 12-bit analogue-to-digital converter operating on a 3.3V supply. This device includes a high bandwidth sample and hold and internal voltage references. Conversion is controlled by a single clock input.

The device has a differential sample and hold input which gives excellent common-mode noise immunity and low distortion. The maximum differential input voltage can be set by the user, via two mode selection pins, to be 1V or 2V. A third PGA mode is designed particularly for single-ended input signals such as composite video sources. Single-ended input signals require one side of the differential input to be tied to an external voltage source.

The device provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. The WM2152 can also accept external reference levels for applications where common or high precision references are required.

The WM2152 provides an out of range indicator flag to indicate when the input signal exceeds the converter's full scale range. An output enable pin allows several devices to share a common bus. Power down mode for the device is under the control of the two mode control pins and takes power consumption down to less than 36 $\mu$ W.

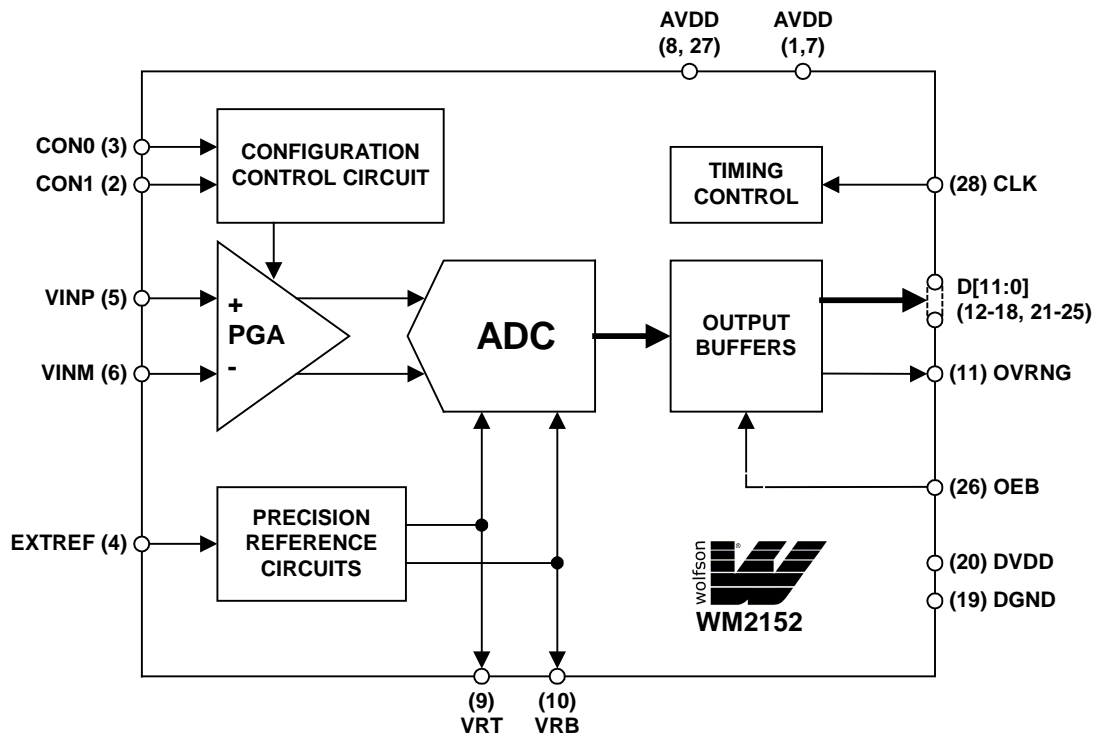
## FEATURES

- 12-bit resolution ADC
- 30MSPS conversion rate
- Programmable Gain Amplifier (PGA)
- Out of range indicator
- Low power - 160mW typical at 3.3V supplies
- Powerdown mode to 30 $\mu$ W typical
- 66dB SNR for 3.58MHz input signal
- -78db THD for 3.58MHz input signal
- 28-pin TSSOP package

## APPLICATIONS

- Direct IF sampling
- Baseband digitisation
- Video Digitisation
- Portable instrumentation
- Digital imaging
- High speed data acquisition

## BLOCK DIAGRAM



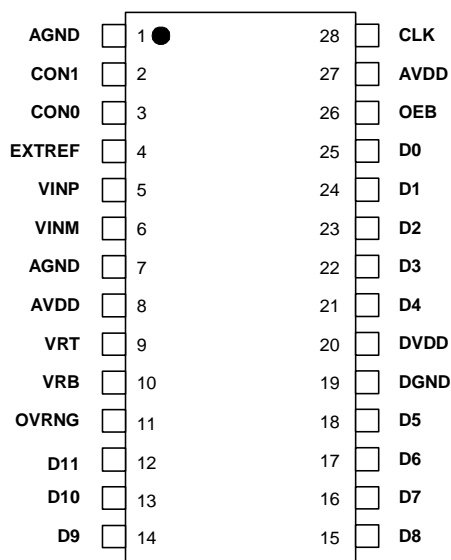
## WOLFSON MICROELECTRONICS LTD

Lutton Court, Bernard Terrace, Edinburgh, EH8 9NX, UK  
 Tel: +44 (0) 131 667 9386  
 Fax: +44 (0) 131 667 5176  
 Email: sales@wolfson.co.uk  
 www.wolfsonmicro.com

Product Preview data sheets contain specifications for products in the formative phase of development. These products may be changed or discontinued without notice.

©2001 Wolfson Microelectronics Ltd.

## PIN CONFIGURATION



## ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM2152CDT	0 to +70°C	28-pin TSSOP
XWM2152IDT	-40 to +85°C	28-pin TSSOP

## PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AGND	Supply	Analogue Ground (for Timing Circuitry)
2	CON1	Digital Input	Mode control pin 1
3	CON0	Digital Input	Mode control pin 0
4	EXTREF	Digital Input	Reference select pin
5	VINP	Analogue Input	Positive analogue input
6	VINM	Analogue Input	Negative analogue input
7	AGND	Supply	Analogue ground
8	AVDD	Supply	Analogue power supply
9	VRT	Analogue I/O	Upper ADC reference voltage
10	VRB	Analogue I/O	Lower ADC reference voltage
11	OVRNG	Digital Output	Out of range indicator
12	D11	Digital Output	Data output bit 11 (MSB)
13	D10	Digital Output	Data output bit 10
14	D9	Digital Output	Data output bit 9
15	D8	Digital Output	Data output bit 8
16	D7	Digital Output	Data output bit 7
17	D6	Digital Output	Data output bit 6
18	D5	Digital Output	Data output bit 5
19	DGND	Supply	Digital ground
20	DVDD	Supply	Digital power supply
21	D4	Digital Output	Data output bit 4
22	D3	Digital Output	Data output bit 3
23	D2	Digital Output	Data output bit 2
24	D1	Digital Output	Data output bit 1
25	D0	Digital Output	Data output bit 0 (LSB)
26	OEB	Digital Input	Output enable (low = enable, high = disable)
27	AVDD	Supply	Analogue Power Supply (for Timing Circuitry)
28	CLK	Digital Input	ADC conversion clock

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DGND	-0.3V	+4.0V
Input clock supply voltage, CLKVDD to CLKGND	-0.3V	+4.0V
Analogue supply voltage, AVDD to AGND	-0.3V	+4.0V
Maximum ground difference between AGND, DGND and CLKGND	-0.3V	+0.3V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V
Voltage range CLK input	CLKGND - 0.3V	CLKVDD + 0.3V
Operating junction temperature range, T <sub>J</sub>	-40°C	+150°C
Storage temperature	-65°C	+150°C
Lead temperature (1.6mm from package body for 10 seconds)		+300°C

## ELECTRICAL CHARACTERISTICS

**Test Conditions:**AVDD = DVDD = 3.3V,  $f_{CLK} = 30\text{MHz}$ , EXTREF = AGND, Mode=1,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC Characteristics</b>						
Resolution			12			bits
Integral Nonlinearity	INL	All modes	-2.5	$\pm 1.2$	+2	LSB
Differential Nonlinearity	DNL	All modes		$\pm 0.4$	$\pm 1$	LSB
Missing Codes		All modes	No missing codes guaranteed			
Offset Error		All modes		0.5	1.2	%FSR
Gain Error		All modes		0.5	3.5	%FSR
<b>Dynamic Performance (Note 1)</b>						
Effective number of bits	ENOB	$f_{IN} = 3.58\text{MHz}$		10.9		bits
		$f_{IN} = 10\text{MHz}$	10.6	10.9		bits
		$f_{IN} = 15\text{MHz}$		10.8		bits
Total harmonic distortion	THD	$f_{IN} = 3.58\text{MHz}$		-76		dB
		$f_{IN} = 10\text{MHz}$		-74	-65	dB
		$f_{IN} = 15\text{MHz}$		-72.5		dB
	SNR	$f_{IN} = 3.58\text{MHz}$		68		dB
		$f_{IN} = 10\text{MHz}$	66	68		dB
		$f_{IN} = 15\text{MHz}$		67.7		dB
Signal to noise and distortion ratio	SINAD	$f_{IN} = 3.58\text{MHz}$		67.4		dB
		$f_{IN} = 10\text{MHz}$	65.6	67.4		dB
		$f_{IN} = 15\text{MHz}$		66.6		dB
Spurious free dynamic range	SFDR	$f_{IN} = 3.58\text{MHz}$		78.1		dB
		$f_{IN} = 10\text{MHz}$	67	76.4		dB
		$f_{IN} = 15\text{MHz}$		74.6		dB
Differential phase	DP			0.12		deg
Differential gain	DG			0.01		%
<b>Analogue Input Signal to (VINP – VINM)</b>						
Input Span		Mode=1, VREF = 1V	-0.5		0.5	V
		Mode=2, VREF = 1V	-1		1	V
		Mode=3, VREF = 1V	0		1	V
Input (VINP or VINM) range		All modes	0		AVDD	V
Input capacitance	$C_{IN}$	All modes		6		pF
Analogue input bandwidth				180		MHz
Power supply rejection ratio	PSRR			54		dB
<b>Conversion Characteristics</b>						
Conversion frequency	$f_{CLK}$		5		30	MHz
Pipeline delay				5		cycles of CLK
Aperture delay	$t_A$			2.0		ns
Aperture jitter				2.0		ps rms
<b>Internal Voltage References (Note 3)</b>						
Upper reference voltage	VRT			2.15		V
Lower reference voltage	VRB			1.15		V
Differential reference voltage (VRT-VRB)	VREF		0.95	1	1.05	V
Differential reference voltage (VRT-VRB) accuracy			-5		+5	%
Power up time of references from standby	$t_{PU}$			100		$\mu\text{s}$

**Test Conditions:**AVDD = DVDD = 3.3V,  $f_{CLK} = 30\text{MHz}$ , EXTREF = AGND, Mode=1,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>External Voltage References</b>						
Externally applied VRT reference range			2		2.5	V
Externally applied VRB reference range			1.05		1.3	V
Externally applied differential reference range (VRT-VRB)			0.75		1.05	V
Reference Input Resistance (VRT to VRB)				9		k $\Omega$
<b>Digital Inputs / Outputs</b>						
Input LOW level	$V_{IL}$				0.2 x VDD	V
Input HIGH level	$V_{IH}$		0.8 x VDD			V
High level output voltage	$V_{OL}$	$I_{OH}=50\mu\text{A}$	DVDD-0.4			V
Low level output voltage	$V_{OH}$	$I_{OL}=-50\mu\text{A}$			0.4	V
High Impedance Output Current					$\pm 1$	$\mu\text{A}$
Rise/Fall time		$C_{LOAD}=10\text{pF}$		5.5		ns
<b>Power Supplies</b>						
CLKVDD supply current	$I_{AA1}$	$f_{CLK} = 30\text{MHz}$	3.0	3.3	3.6	mA
AVDD supply current	$I_{AA2}$			35		mA
DVDD supply current	$I_{DD}$			10		mA
Total supply current	$I_{TOT}$	$f_{CLK} = 30\text{MHz}$		48.3		mA
Total supply current in standby mode	$I_{SB}$	$f_{CLK} = 0\text{MHz}$			10	$\mu\text{A}$
Power consumption		$f_{CLK} = 30\text{MHz}$		168	220	mW

**Notes**

1. Input amplitudes for all single tone dynamic tests are all -0.5dBFS.
2. Inputs for two-tone IMD are 4.4MHz and 4.5MHz, each at -7dBFS.
3. The internal reference voltage is not intended for use driving off-chip.

### TYPICAL SYSTEM PERFORMANCE

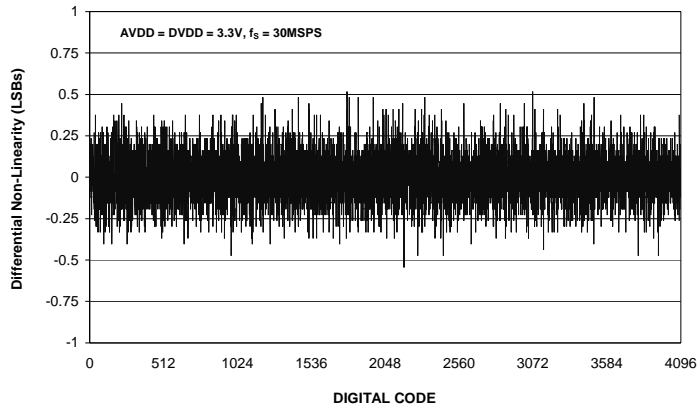


Figure 1 Differential Non-Linearity

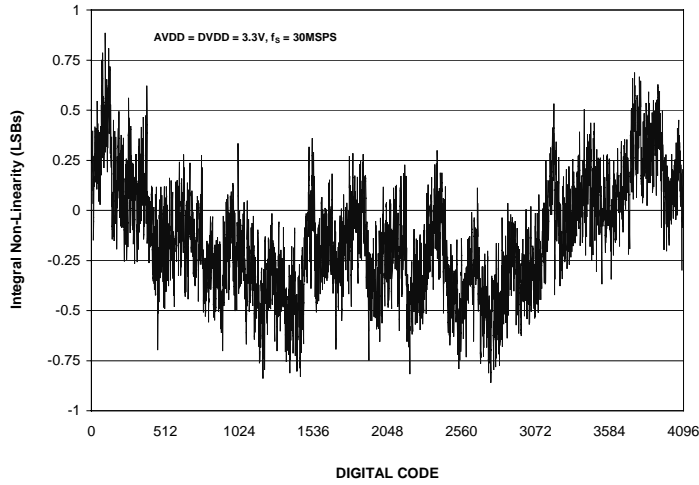
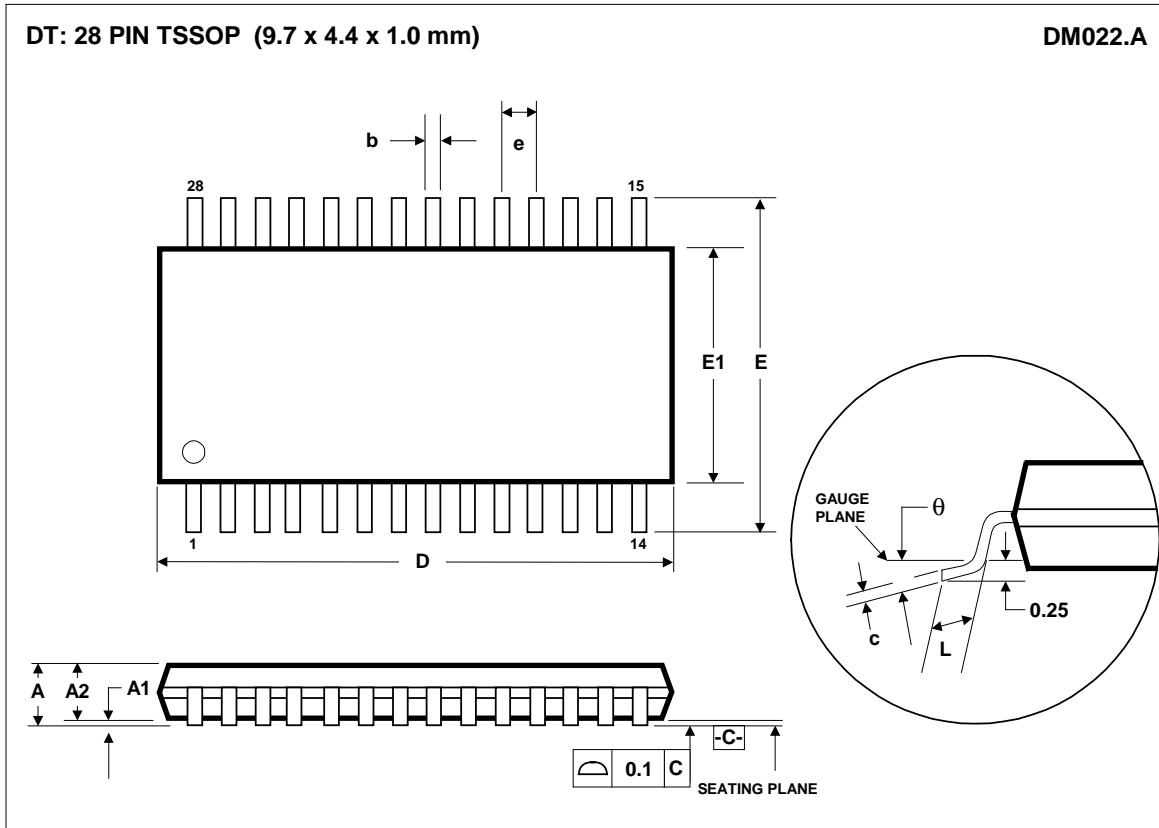


Figure 2 Integral Non-Linearity

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A <sub>1</sub>	0.05	-----	0.15
A <sub>2</sub>	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	9.60	9.70	9.80
e	0.65 BSC		
E	6.4 BSC		
E <sub>1</sub>	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0°	-----	8°
REF:	JEDEC.95, MO-153		

- NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.  
 D. MEETS JEDEC.95 MO-153, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.