WM2614

Quad 12-bit Serial Input Voltage Output DAC

Production Data, June 1999, Rev 1.0

FEATURES

- **Quad 12-bit DAC voltage output DAC**
- **Dual 2.7V to 5.5V supply (separate digital and analogue supplies)**
- **DNL ±0.4 LSB, INL ±1.5 LSB**
- **Low power consumption:**
  - **5.5mW, slow mode – 5V supply**
  - **3.3mW, slow mode – 3V supply**
- **TMS320, (Q)SPI™, and Microwire™ compatible serial interface**
- **Programmable settling time of 4µs or 12µs typical**

APPLICATIONS

- **Battery powered test instruments**
- **Digital offset and gain adjustment**
- **Battery operated/remote industrial controls**
- **Machine and motion control devices**
- **Wireless telephone and communication systems**
- **Speech synthesis**
- **Arbitrary waveform generation**

ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2614CDT	0° to 70°C	16-pin TSSOP
WM2614IDT	-40° to 85 °C	16-pin TSSOP

DESCRIPTION

The WM2614 is a quadruple 12-bit voltage output, resistor string, digital-to-analogue converter. Each DAC can be individually powered down under software control. A hardware controlled mode is provided that powers down all DACs. Power down reduces current consumption to 10nA.

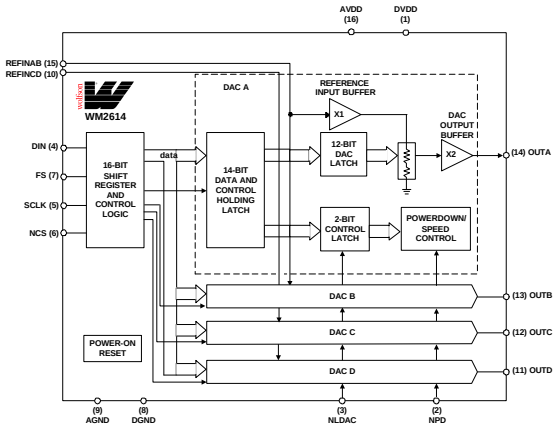
The device has been designed to interface efficiently to industry standard microprocessors and DSPs, including the TMS320 family. The WM2614 is programmed with a 16-bit serial word comprising of a DAC address, individual DAC control bits and a 12-bit value.

The WM2614 has provision for two supplies: one supply for the serial interface (DVDD, DGND) and one for the DACs, reference buffers and output buffers (AVDD, AGND). This enables a typical application where the device can be controlled via a microprocessor operating on a 3V supply, with the DACs operating on a 5V supply. Alternatively, the supplies can be tied together in a single supply application.

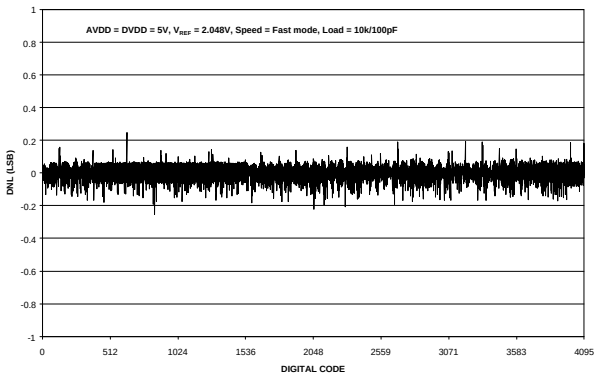
Excellent performance is delivered with a typical DNL of 0.4 LSBs. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The output stage is buffered by a x2 gain near rail-to-rail amplifier, which features a Class AB output stage. DACs A and B can have a different reference voltage to DACs C and D.

The device is available in a 16-pin TSSOP package. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

BLOCK DIAGRAM



TYPICAL PERFORMANCE



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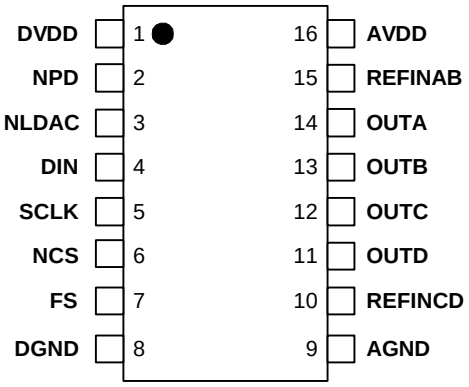
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	DVDD	Supply	Digital supply.
2	NPD	Digital input	Power down. Powers down all DACs overriding their individual power down settings and all output stages. This pin is active low.
3	NLDAC	Digital input	Load DAC. Digital input active low. NLDAC must be taken low to update the DAC latch from the holding latches.
4	DIN	Digital input	Serial data input.
5	SCLK	Digital input	Serial clock input.
6	NCS	Digital input	Chip select. This pin is active low.
7	FS	Digital input	Frame synchronisation for serial output data.
8	DGND	Ground	Digital ground.
9	AGND	Ground	Analogue ground.
10	REFINCD	Analogue input	Voltage reference input for DACs C and D.
11	OUTD	Analogue output	DAC D output.
12	OUTC	Analogue output	DAC C output.
13	OUTB	Analogue output	DAC B output.
14	OUTA	Analogue output	DAC A output.
15	REFINAB	Analogue input	Voltage reference input for DACs A and B.
16	AVDD	Supply	Analogue supply.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION		MIN	MAX
Supply voltages, DVDD to DGND, AVDD to AGND			7V
Supply voltage differences, AVDD to DVDD		-2.8V	2.8V
Digital input voltage		-0.3V	DVDD + 0.3V
Reference input voltage		-0.3V	AVDD + 0.3V
Operating temperature range, T_A	WM2614CDT WM2614IDT	0°C -40°C	70°C 85°C
Storage temperature		-65°C	150°C
Lead temperature 1.6mm (1/16 inch) soldering for 10 seconds			260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	AVDD, DVDD		2.7		5.5	V
High-level digital input voltage	V_{IH}	DVDD = 2.7V to 5.5V	2			V
Low-level digital input voltage	V_{IL}	DVDD = 2.7V to 5.5V			0.8	V
Reference voltage to REFINAB, REFINCD	V_{REF}	See Note			AVDD - 1.5	V
Load resistance	R_L		2	10		kΩ
Load capacitance	C_L				100	pF
Serial clock rate	f_{SCLK}				20	MHz
Operating free-air temperature	T_A	WM2614CDT	0		70	°C
		WM2614IDT	-40		85	°C

Note: Reference voltages greater than AVDD/2 will cause output saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

Test Conditions:
R_L = 10kΩ, C_L = 100pF. AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static DAC Specifications						
Resolution			12			bits
Integral non-linearity	INL	See Note 1		±1.5	±4	LSB
Differential non-linearity	DNL	See Note 2		±0.4	±1	LSB
Zero code error	ZCE	See Note 3		3	±12	mV
Gain error	GE	See Note 4		0.25	±0.6	% FSR
D.c. power supply rejection ratio	d.c. PSRR	See Note 5		0.5		mV/V
Zero code error temperature coefficient		See Note 6		10		ppm/°C
Gain error temperature coefficient		See Note 6		10		ppm/°C
DAC Output Specifications						
Output voltage range			0		AVDD - 0.1	V
Output load regulation		2kΩ to 10kΩ load See Note 7		0.1	0.25	%
Power Supplies						
Active supply current	I_{DD}	No load, V_{IH} = DVDD, V_{IL} = 0V				mA
		AVDD = 5V, V_{REF} = 2.048V Slow		1.6	2.4	
		AVDD = 5V, V_{REF} = 2.048V Fast		3.8	5.6	
		AVDD = 3V, V_{REF} = 1.024V Slow		1.2	1.8	
		AVDD = 3V, V_{REF} = 1.024V Fast See Note 8		3.2	4.8	
Power down supply current		No load, all digital inputs 0V or DVDD See Note 9		0.01	10	µA
Dynamic DAC Specifications						
Slew rate		DAC code 128 to 4095, 10%-90% Slow Fast See Note 10	 0.5 2.5	 1.0 4.0		 V/µs V/µs
Settling time		DAC code 128 to 4095 Slow Fast See Note 11		 12.0 4.0		 µs µs
Glitch energy		Code 2047 to 2048		10		nV-s
Signal to noise ratio	SNR	fs = 400ksps, f_{OUT} = 1kHz, BW = 20kHz, See Note 12	66	74		dB
Signal to noise and distortion ratio	SNRD	fs = 400ksps, f_{OUT} = 1kHz, BW = 20kHz, See Note 12	54	66		dB
Total harmonic distortion	THD	fs = 400ksps, f_{OUT} = 1kHz, BW = 20kHz, See Note 12		-68	-56	dB
Spurious free dynamic range	SPFDR	fs = 400ksps, f_{OUT} = 1kHz, BW = 20kHz, See Note 12	56	70		dB

Test Conditions:
R_L = 10kΩ, C_L = 100pF. AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference						
Reference input resistance	R_{REFIN}			10		MΩ
Reference input capacitance	C_{REFIN}			5		pF
Reference feedthrough		V_{REF} = $1V_{PP}$ at 1kHz + 1.024V dc, DAC code 0		-75		dB
Reference input bandwidth		V_{REF} = $0.2V_{PP}$ + 1.024V dc DAC code 2048				
		Slow		0.5		MHz
		Fast		1		MHz
Digital Inputs						
High level input current	I_{IH}	Input voltage = DVDD			1	µA
Low level input current	I_{IL}	Input voltage = 0V			-1	µA
Input capacitance	C_I			3		pF

Notes:

1. **Integral non-linearity** (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).
2. **Differential non-linearity** (DNL) is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
3. **Zero code error** is the voltage output when the DAC input code is zero.
4. **Gain error** is the deviation from the ideal full scale output excluding the effects of zero code error.
5. **Power supply rejection ratio** is measured by varying AVDD from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
6. **Zero code error** and **Gain error** temperature coefficients are normalised to V_{REF}.
7. **Output load regulation** is the difference between the output voltage at full scale with a 10kΩ load and 2kΩ load. It is expressed as a percentage of the full scale output voltage with a 10kΩ load.
8. $\mathbf{I_{DD}}$ is measured while continuously writing code 2048 to the DAC. For V_{IH} < DVDD - 0.7V and V_{IL} > 0.7V supply current will increase.
9. **Typical supply current** in power down mode is 10nA. Production test limits are wider for speed of test.
10. **Slew rate** results are for the lower value of the rising and falling edge slew rates.
11. **Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.
12. **SNR, SNRD, THD** and **SPFDR** are measured on a synthesised sinewave at frequency f_{OUT} generated with a sampling frequency fs.

SERIAL INTERFACE

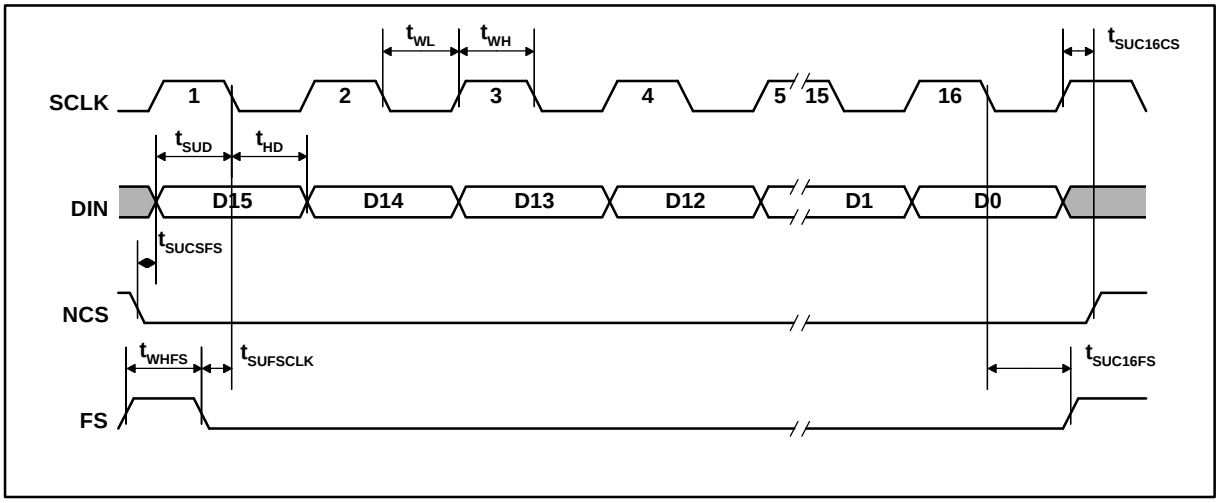


Figure 1 Timing Diagram

Test Conditions:
R_L = 10kΩ, C_L = 100pF. AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SUCSFS}	Setup time NCS low before negative FS edge.	10			ns
$t_{SUFSCLK}$	Setup time FS low before first negative SCLK edge.	8			ns
$t_{SUC16FS}$	Setup time, sixteenth negative SCLK edge after FS low on which D0 is sampled before rising edge of FS.	10			ns
$t_{SUC16CS}$	Setup time, sixteenth positive SCLK edge (first positive after D0 sampled) before NCS rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and the NCS rising edge.	10			ns
t_{WHCLK}	Pulse duration, SCLK high.	25			ns
t_{WLCLK}	Pulse duration, SCLK low.	25			ns
t_{SUDCLK}	Setup time, data ready before SCLK falling edge.	8			ns
t_{HDCLK}	Hold time, data held valid after SCLK falling edge.	5			ns
t_{WHFS}	Pulse duration, FS high.	20			ns

TYPICAL PERFORMANCE GRAPHS

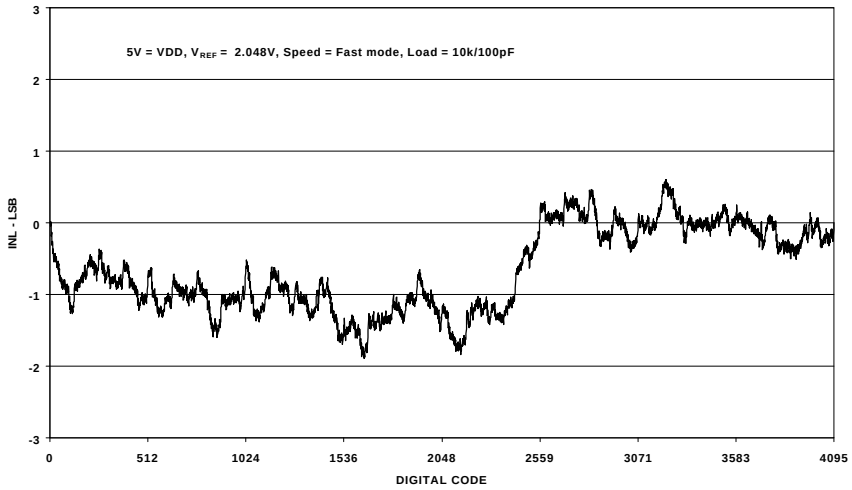


Figure 2 Integral Non-Linearity

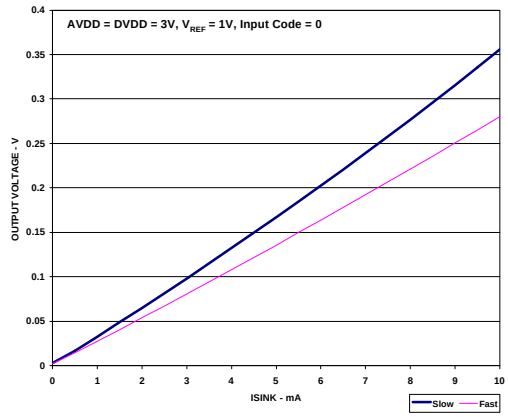


Figure Sink 3 Current AVDD = DVDD = 3V

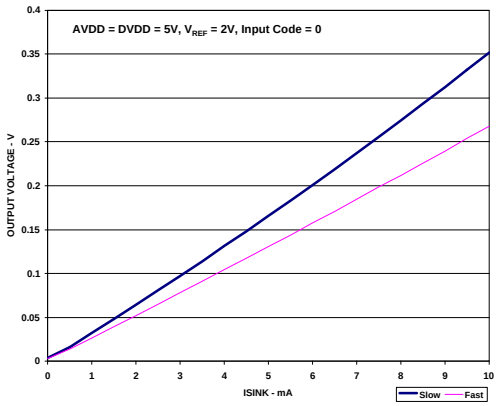


Figure 4 Sink Current AVDD = DVDD = 5V

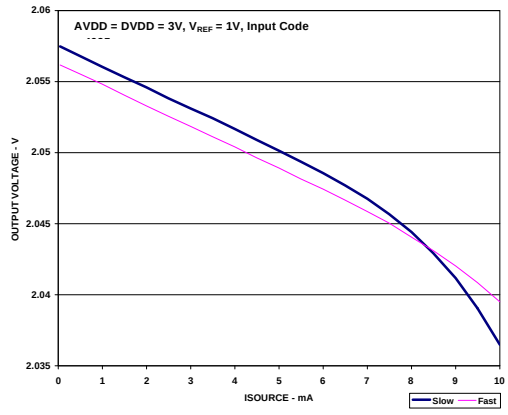


Figure 5 Source Current AVDD = DVDD = 3V

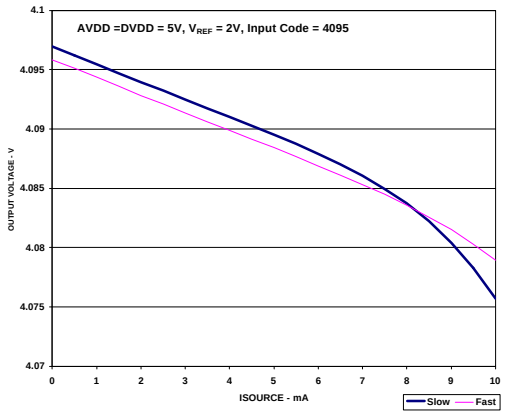


Figure 6 Source Current AVDD = DVDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The device uses a resistor string network buffered with an op amp to convert 12-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$\text{Output voltage} = 2(V_{REF})\frac{CODE}{4096}$$

INPUT			OUTPUT
1111	1111	1111	$2(V_{REF})\frac{4095}{4096}$
	:		:
1000	0000	0001	$2(V_{REF})\frac{2049}{4096}$
1000	0000	0000	$2(V_{REF})\frac{2048}{4096} = V_{REF}$
0111	1111	1111	$2(V_{REF})\frac{2047}{4096}$
	:		:
0000	0000	0001	$2(V_{REF})\frac{1}{4096}$
0000	0000	0000	0V

Table 1 Binary Code Table (0V to $2V_{REFIN}$ Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

EXTERNAL REFERENCE

The reference voltage input is buffered which makes the DAC input resistance independent of code. The REFIN pin has an input resistance of 10MΩ and an input capacitance of typically 5pF. The reference voltage determines the DAC full-scale output.

HARDWARE CONFIGURATION OPTIONS

The device has two configuration options that are controlled by device pins.

DEVICE POWER DOWN

The device can be powered-down by pulling pin NPD (Pin 2) high. This powers down all DACs overriding their individual power down settings. This will reduce power consumption to typically 10nA. When the power down function is released the device reverts to the DAC code set prior to power down.

SIMULTANEOUS DAC UPDATE

The NLDAC pin (Pin 3) can be held high to prevent serial word writes from updating the DAC latches. By writing new values to multiple DACs then pulling NLDAC low, all new DAC codes are loaded into the DAC latches simultaneously.

SERIAL INTERFACE

Explanation of data transfer:

First, the device has to be enabled with NCS set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the next rising edge on SCLK or FS causes the content of the shift register to be moved to the DAC holding latch. If NLDAC is low, the DAC latch will also updated immediately.

The serial interface of the device can be used in two basic modes:

- four wire (with chip select)
- three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). If there is no need to have more than one device on the serial bus, then NCS can be tied low.

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the device timing. The maximum serial rate is:

$$f_{SCLK}max = \frac{1}{t_{WCH\,min} + t_{WCL\,min}} = 20MHz$$

The digital update rate is limited to an 800ns period, or 1.25MHz frequency. However, the DAC settling time to 12 bits limits the update rate for large input step transitions.

SOFTWARE CONFIGURATION OPTIONS

The 16 bits of data can be transferred with the sequence shown in Table 2. D11-D0 contains the 12-bit data word. D15-D12 hold the programmable options.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A1	A0	PWR	SPD	New DAC value (12 bits)											

Table 2 Register Map

DAC ADDRESSING

A particular DAC (A, B, C, D) within the device is selected by A1 and A0 within the input word.

A1	A0	DAC ADDRESS
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

PROGRAMMABLE SETTLING TIME

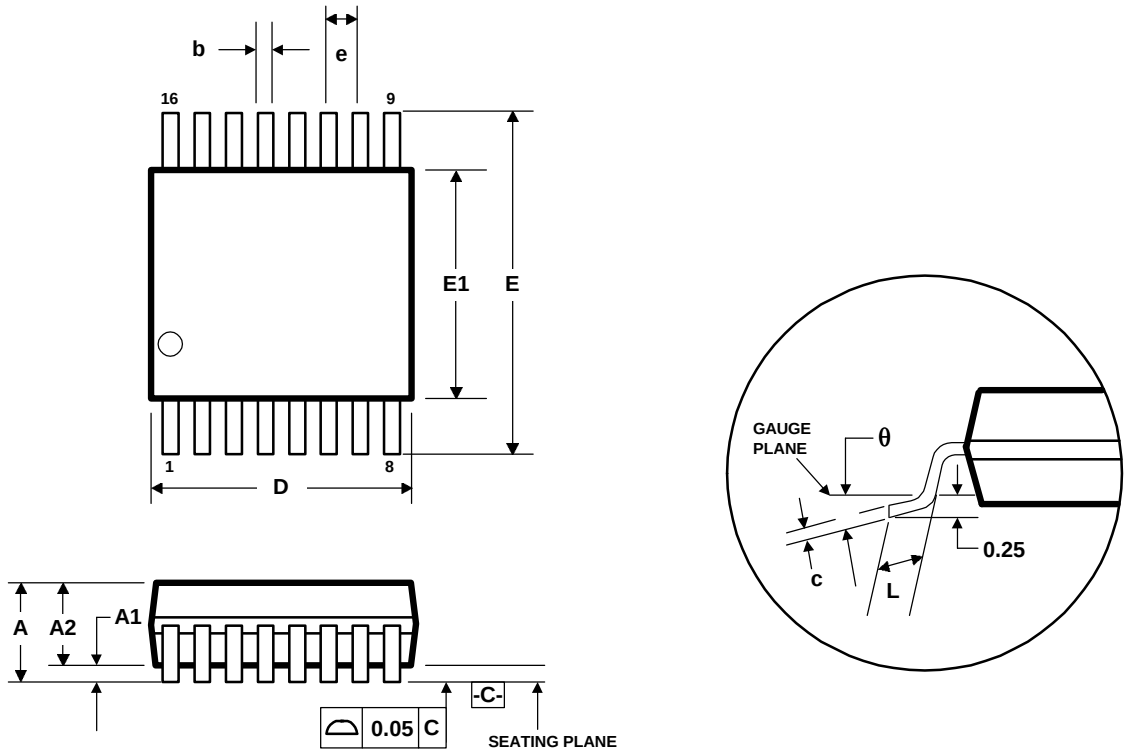
Settling time is a software selectable 12µs or 4µs, typical to within ±0.5LSB of final value. This is controlled by the value of D12 and associated DAC address. A ONE defines a settling time of 4µs, a ZERO defines a settling time of 12µs for that DAC.

PROGRAMMABLE POWER DOWN

The power down function is controlled by D13. A ZERO configures that DAC as active, a ONE configures that DAC into power down mode. When the power down function is released the device reverts to the DAC code set prior to power down.

PACKAGE DIMENSIONS

DT: 16 PIN TSSOP (5.0 x 4.4 x 1.0 mm) **DM013.A**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	4.90	5.00	5.10
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.