



WM2638 Dual 12-Bit Serial Input Voltage Output DAC with Internal reference

Production Data, Rev 1.0, July 1999

FEATURES

- Two 12-bit voltage output DACs
- Single 2.7V to 5.5V supply operation
- DNL ± 0.4 LSBs, INL ± 2 LSBs
- Low power consumption
 - 12mW typical in fast mode
 - 6mW typical in slow mode
- TMS320, (Q)SPI™, and Microwire™ compatible serial interface
- Programmable settling time 1 μ s or 3.5 μ s typical
- Power down mode 10nA

APPLICATIONS

- Battery powered test instruments
- Digital offset and gain adjustment
- Battery operated/remote industrial controls
- Machine and motion control devices
- Cellular telephones
- Wireless telephones and communication systems
- Speech synthesis
- Arbitrary waveform generation

ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE |
|----------|--------------|------------|
| WM2638CD | 0° to 70°C | 8-pin SOIC |
| WM2638ID | -40° to 85°C | 8-pin SOIC |

DESCRIPTION

The WM2638 is a dual 12-bit voltage output, resistor string, digital-to-analogue converter. A software controlled power down mode is provided that reduces current consumption to 10nA.

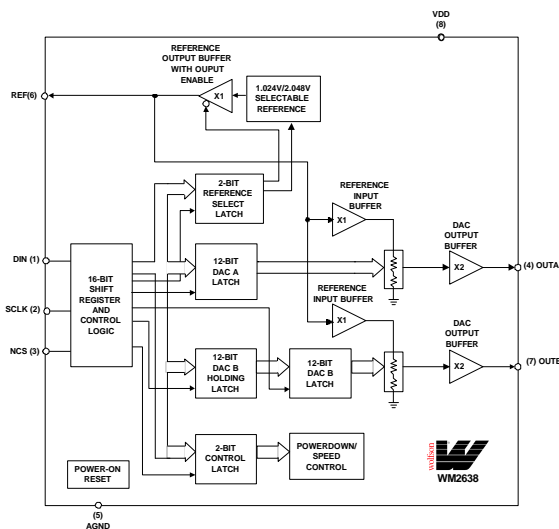
The WM2638 features an internal programmable voltage reference simplifying overall system design. A reference voltage may also be supplied externally.

The device has been designed to interface efficiently to industry standard microprocessors and DSPs, including the TMS320 family. The WM2638 is programmed with a 16-bit serial word comprising of a latch address, mode control bits and DAC or control data.

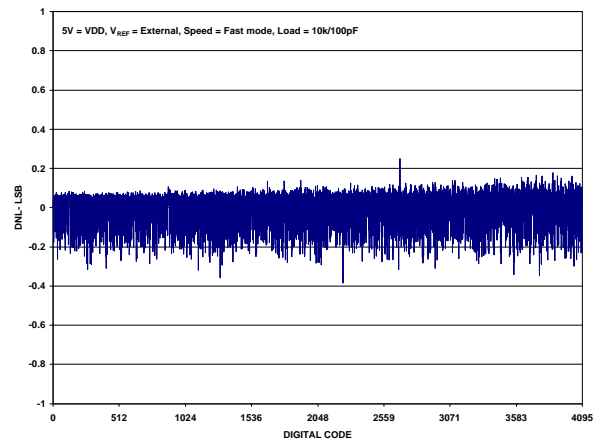
Excellent performance is delivered with a typical DNL of 0.4LSBs. The programmable settling time allows the designer to optimise speed versus power consumption. The output stage is buffered by a x2 gain near rail-to-rail amplifier.

The device is available in an 8-pin SOIC package ideal for space-critical applications. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

BLOCK DIAGRAM



TYPICAL PERFORMANCE



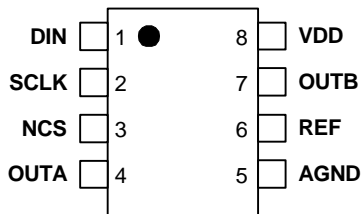
WOLFSON MICROELECTRONICS LTD
Lutton Court, Bernard Terrace, Edinburgh, EH8 9NX, UK
Tel: +44 (0) 131 667 9386
Fax: +44 (0) 131 667 5176
Email: sales@wolfson.co.uk
http://www.wolfson.co.uk

Production Data contains final specifications current on publication date. Supply of products conforms to Wolfson Microelectronics' Terms and Conditions.

Last printed 15/07/99 15:58

©1999 Wolfson Microelectronics Ltd.

PIN CONFIGURATION



PIN DESCRIPTION

| PIN NO | NAME | TYPE | DESCRIPTION |
|--------|------|-----------------|--------------------------------------|
| 1 | DIN | Digital input | Serial data input. |
| 2 | SCLK | Digital input | Serial clock input. |
| 3 | NCS | Digital input | Chip select. This pin is active low. |
| 4 | OUTA | Analogue output | DAC A analogue output. |
| 5 | AGND | Supply | Analogue ground. |
| 6 | REF | Analogue I/O | Reference voltage input/output. |
| 7 | OUTB | Analogue output | DAC B analogue output |
| 8 | VDD | Supply | Positive power supply. |

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

| CONDITION | | MIN | MAX |
|---|---------|-------|------------|
| Supply voltage, VDD to AGND | | | 7V |
| Digital input voltage range to AGND | | -0.3V | VDD + 0.3V |
| Reference input voltage range to AGND | | -0.3V | VDD + 0.3V |
| Output voltage at OUT from external source | | | VDD + 0.3V |
| Operating temperature range, T _A | WM2638C | 0°C | 70°C |
| | WM2638I | -40°C | 85°C |
| Storage temperature | | -65°C | 150°C |
| Lead temperature 1.6mm (1/16 inch) soldering for 10 seconds | | | 260°C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-------------------|-----------------|-----|-----|-----------|------|
| Supply voltage | VDD | | 2.7 | | 5.5 | V |
| High-level digital input voltage | V _{IH} | | 2 | | 0.8 | V |
| Low-level digital input voltage | V _{IL} | | | | | V |
| Reference voltage to REF | V _{REF} | | | | VDD - 1.5 | V |
| Load resistance | R _L | | 2 | | | kΩ |
| Load capacitance | C _L | | | | 100 | |
| Serial clock rate | F _{SCLK} | | | | 20 | |
| Operating free-air temperature | T _A | WM2638C | 0 | | 70 | °C |
| | | WM2638I | -40 | | 85 | °C |

Note: Reference voltages greater than VDD/2 will cause saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------|--|-----|--|--|--|
| Static DAC Specifications | | | | | | |
| Resolution | | | 12 | | | bits |
| Integral non-linearity | INL | See Note 1 | | ± 2.0 | ± 4.0 | LSB |
| Differential non-linearity | DNL | See Note 2 | | ± 0.4 | ± 1 | LSB |
| Zero code error | ZCE | See Note 3 | | | ± 24 | mV |
| Gain error | GE | See Note 4 | | | ± 0.6 | % FSR |
| D.c. power supply rejection ratio | DC PSRR | See Note 5 | | 0.5 | | mV/V |
| Zero code error temperature coefficient | | See Note 6 | | 10 | | ppm/ $^{\circ}C$ |
| Gain error temperature coefficient | | See Note 6 | | 10 | | ppm/ $^{\circ}C$ |
| DAC Output Specifications | | | | | | |
| Output voltage range | | | 0 | | $V_{DD} - 0.4$ | V |
| Output load regulation | | 2k Ω to 10k Ω load See Note 7 | | ± 0.1 | ± 0.25 | % |
| Power Supplies | | | | | | |
| Active supply current | I_{DD} | No load, $V_{IH} = V_{DD}$, $V_{IL} = 0V$ $V_{DD} = 5V$, $V_{REF} = 2.048V$, Internal Slow Fast $V_{DD} = 5V$, $V_{REF} = 2.048V$, External Slow Fast $V_{DD} = 3V$, $V_{REF} = 1.024V$, Internal Slow Fast $V_{DD} = 3V$, $V_{REF} = 1.024V$, External Slow Fast See Note 8 | | 2.2 4.3 1.8 3.9 1.8 3.8 1.5 3.5 | 2.7 5.2 2.2 4.8 2.3 4.7 1.9 4.3 | mA mA mA mA mA mA mA mA |
| Power down supply current | | No load, all digital inputs 0V or VDD, See Note 9 | | 0.01 | 10 | μA |
| Dynamic DAC Specifications | | | | | | |
| Slew rate | | DAC code 32 to 4095, 10%-90% Slow Fast See Note 10 | | 1.5 8.0 | | V/ μs V/ μs |
| Settling time | | DAC code 32 to 4095 Slow Fast See Note 11 | | 3.5 1.0 | | μs μs |
| Glitch energy | | Code 2047 to 2048 | | 10 | | nV-s |
| Signal to noise ratio | SNR | $f_s = 400ksp/s$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 12 | 69 | 74 | | dB |
| Signal to noise and distortion ratio | SNRD | $f_s = 400ksp/s$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 12 | 58 | 67 | | dB |

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---------------|--|-------|------------|-------|------------|
| Total harmonic distortion | THD | $f_s = 400ksp/s$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 12 | | -69 | -57 | dB |
| Spurious free dynamic range | SPFDR | $f_s = 400ksp/s$, $f_{OUT} = 1kHz$, BW = 20kHz See Note 12 | 57 | 72 | | dB |
| Reference configured as input | | | | | | |
| Reference input resistance | R_{REFIN} | | | 10 | | M Ω |
| Reference input capacitance | C_{REFIN} | | | 55 | | pF |
| Reference feedthrough | | $V_{REF} = 1V_{PP}$ at 1kHz + 1.024V dc, DAC code 0 | | -60 | | dB |
| Reference input bandwidth | | $V_{REF} = 0.2V_{PP} + 1.024V$ dc DAC code 2048 Slow Fast | | 1.0 1.0 | | MHz MHz |
| Reference configured as output | | | | | | |
| Low reference voltage | $V_{REFOUTL}$ | | 1.003 | 1.024 | 1.045 | V |
| High reference voltage | $V_{REFOUTH}$ | $V_{DD} > 4.75V$ | 2.027 | 2.048 | 2.069 | V |
| Output source current | I_{REFSRC} | | | | 1 | mA |
| Output sink current | I_{REFSNK} | | -1 | | | mA |
| Load Capacitance | | | | | 100 | pF |
| PSRR | | | | -48 | | dB |
| Digital Inputs | | | | | | |
| High level input current | I_{IH} | Input voltage = V_{DD} | | | 1 | μA |
| Low level input current | I_{IL} | Input voltage = 0V | | | -1 | μA |
| Input capacitance | C_I | | | 8 | | pF |

Notes:

- Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).
- Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
- Zero code error** is the voltage output when the DAC input code is zero.
- Gain error** is the deviation from the ideal full scale output excluding the effects of zero code error.
- Power supply rejection ratio** is measured by varying V_{DD} from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
- Zero code error** and **Gain error** temperature coefficients are normalised to full scale voltage.
- Output load regulation** is the difference between the output voltage at full scale with a 10k Ω load and 2k Ω load. It is expressed as a percentage of the full scale output voltage with a 10k Ω load.
- I_{DD} is measured while continuously writing code 2048 to the DAC. For $V_{IH} < V_{DD} - 0.7V$ and $V_{IL} > 0.7V$ supply current will increase.
- Typical supply current** in power down mode is 10nA. Production test limits are wider for speed of test.
- Slew rate** results are for the lower value of the rising and falling edge slew rates
- Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.
- SNR, SNRD, THD** and **SPFDR** are measured on a synthesised sinewave at frequency f_{OUT} generated with a sampling frequency f_s .

SERIAL INTERFACE

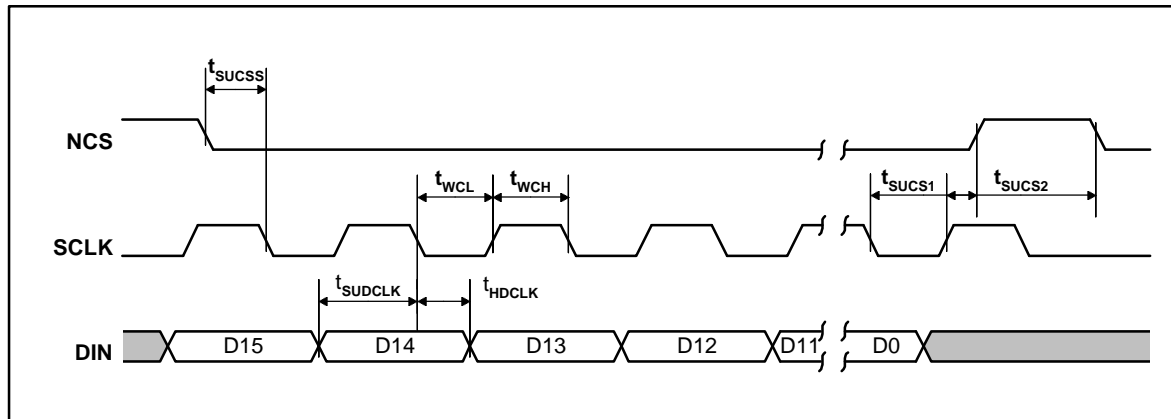


Figure 1 Timing Diagram

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|-----|-----|-----|------|
| t_{sucss} | Setup time NCS low before SCLK low | 10 | | | ns |
| t_{sucs1} | Setup time, rising edge of SCLK to rising edge of NCS, external end of write | 10 | | | ns |
| t_{sucs2} | Setup time, rising edge of SCLK to falling edge of NCS, start of next write cycle | 5 | | | ns |
| t_{wcl} | Pulse duration, SCLK high | 25 | | | ns |
| t_{wch} | Pulse duration, SCLK low | 25 | | | ns |
| t_{sudclk} | Setup time, data ready before SCLK falling edge | 10 | | | ns |
| t_{hdclk} | Hold time, data held valid after SCLK falling edge | 5 | | | ns |

TYPICAL PERFORMANCE GRAPHS

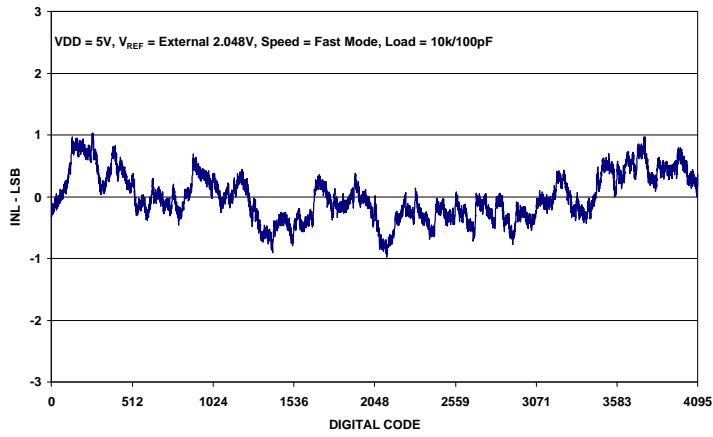


Figure 2 Integral Non-Linearity

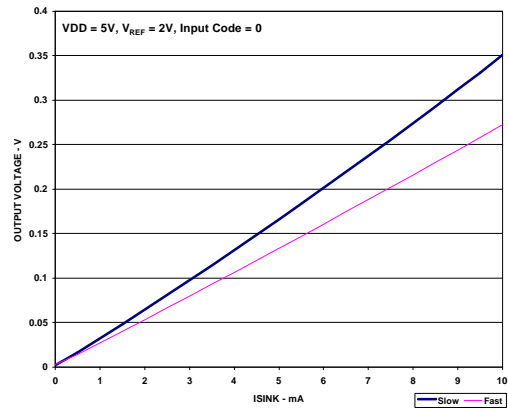
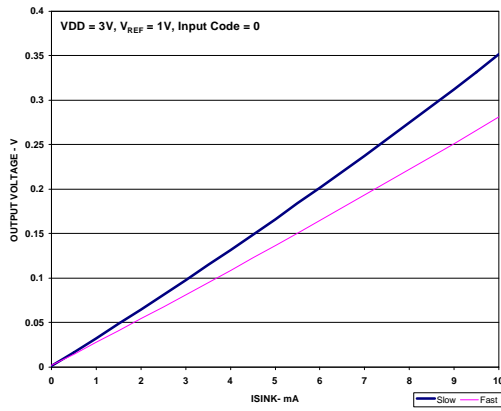


Figure 3 Sink Current VDD = 3V

Figure 4 Sink Current VDD = 5V

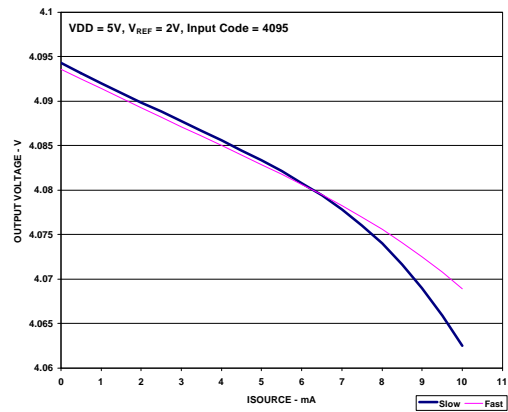
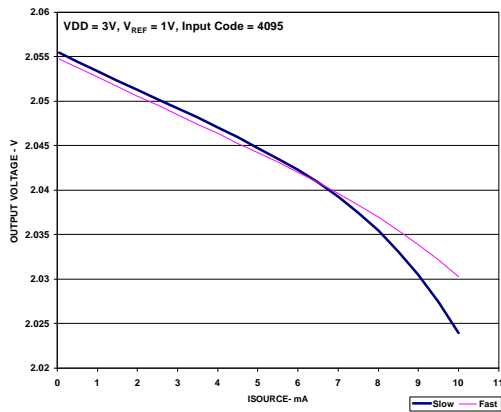


Figure 5 Source Current VDD = 3V

Figure 6 Source Current VDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The device uses a resistor string network buffered with an op amp to convert 12-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$\text{Output voltage} = 2(V_{\text{REF}}) \frac{\text{CODE}}{4096}$$

| INPUT | | | OUTPUT |
|-------|------|------|--|
| 1111 | 1111 | 1111 | $2(V_{\text{REF}}) \frac{4095}{4096}$ |
| | : | | : |
| 1000 | 0000 | 0001 | $2(V_{\text{REF}}) \frac{2049}{4096}$ |
| 1000 | 0000 | 0000 | $2(V_{\text{REF}}) \frac{2048}{4096} = V_{\text{REF}}$ |
| 0111 | 1111 | 1111 | $2(V_{\text{REF}}) \frac{2047}{4096}$ |
| | : | | : |
| 0000 | 0000 | 0001 | $2(V_{\text{REF}}) \frac{1}{4096}$ |
| 0000 | 0000 | 0000 | 0V |

Table 1 Binary Code Table (0V to 2V_{REF} Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC registers to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

SERIAL INTERFACE

When chip select (NCS) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The falling edge of the SCLK input shifts the data into the input register. After 16 bits have been transferred, the next rising edge on SCLK or NCS then transfers the data to the DAC latch. When NCS is high, input data cannot be clocked into the input register (see Table 2).

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the device timing. The maximum serial rate is:

$$f_{\text{SCLKmax}} = \frac{1}{t_{\text{WCHmin}} + t_{\text{WCLmin}}} = 20\text{MHz}$$

The digital update rate is limited to an 800ns period, or 1.25MHz frequency. However, the DAC settling time to 12 bits limits the update rate for large input step transitions.

SOFTWARE CONFIGURATION OPTIONS

The 16 bits of data can be transferred with the sequence shown in Table 2. D11-D0 contains the 12-bit data word. D15-D12 hold the programmable options which are summarized in Table 3.

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|---|-----|----|----|----|----|----|----|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R1 | SPD | PWD | R0 | New DAC value or control register value | | | | | | | | | | | |

Table 2 Serial Word Format

PROGRAMMABLE SETTLING TIME

Settling time is a software selectable 3.5 μ s or 1 μ s typical, to within ± 0.5 LSB of final value. This is controlled by the value of D14. A ONE defines a settling time of 1 μ s, a ZERO defines a settling time of 3.5 μ s.

PROGRAMMABLE POWER DOWN

The power down function is controlled by D13. A ZERO configures the device as active, or fully powered up, a ONE configures the device into power down mode. When the power down function is released the device reverts back to the DAC code set prior to power down.

REGISTER ADDRESSING

A separate internal control register is available. This is accessed from the register access bits R1 (Bit D15) and R0 (Bit D12).

| R1 (BIT D15) | R0 (BIT D12) | REGISTER |
|-----------------|-----------------|--|
| 0 | 0 | Write data to DAC B and BUFFER |
| 0 | 1 | Write data to BUFFER |
| 1 | 0 | Write data to DAC A and update DAC B with BUFFER content |
| 1 | 1 | Write data to control register |

Table 3 Programmable Options

The contents of the control register, shown below in Table 3, are used to program the internal reference function

| | | | | | | | | | | | |
|-----|-----|----|----|----|----|----|----|----|----|------|------|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| x | x | x | x | x | x | x | x | x | X | REF1 | REF0 |

Table 4 Control Register Contents

PROGRAMMABLE INTERNAL REFERENCE

The reference can be sourced internally or externally under software control. If an external reference voltage is applied to the REF pin, the device must be configured to accept this.

If an external reference is selected, the reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10M Ω and an input capacitance of typically 55pF. The reference voltage determines the DAC full-scale output.

If an internal reference is selected, a voltage of 1.024V or 2.048V is available. The internal reference can source up to 1mA and can therefore be used as an external system reference.

| REF1 (BIT D1) | REF0 (BIT D0) | REGISTER |
|------------------|------------------|----------|
| 0 | 0 | External |
| 0 | 1 | 1.024V |
| 1 | 0 | 2.048V |
| 1 | 1 | External |

Table 5 Internal Reference Options

Examples:

1. Set internal reference voltage to 2.048V

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | x | 0 | 1 | x | x | x | x | x | x | x | x | x | x | 1 | 0 |

2. Write new DAC A value and update DAC A output

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|------------------------|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | x | 0 | 0 | New DAC A output value | | | | | | | | | | | |

FUNCTION OF THE LATCH CONTROL BITS (D15 AND D12)

PURPOSE AND USE OF THE DOUBLE BUFFER

Normally only one DAC output can change after a write. The double buffer allows both DAC outputs to change after a single write. This is achieved by the two following steps.

- A double buffer only write is executed to store the new DAC B data without changing the DAC A and B outputs.
- Following the previous step, a write to latch A is executed. This writes the serial interface register (SIR) data to latch A and also writes the double buffer contents to latch B. Thus both DACs receive their new data at the same time and so both DAC outputs begin to change at the same time.

Unless a double buffer only write is issued, the latch B and double buffer contents are identical. Thus, following a write to latch A or B with another write to latch A does not change the latch B contents.

Three data transfer options are possible. All transfers occur immediately after NCS goes high (or on the sixteenth positive SCLK edge, whichever is earlier) and are described in the following sections).

LATCH A WRITE, LATCH B UPDATE (D15 = HIGH, D12 = LOW)

The serial interface register (SIR) data are written to latch A and the double buffer latch contents are written to latch B. The double buffer contents are unaffected. This program bit condition allows simultaneous output updates of both DACs.

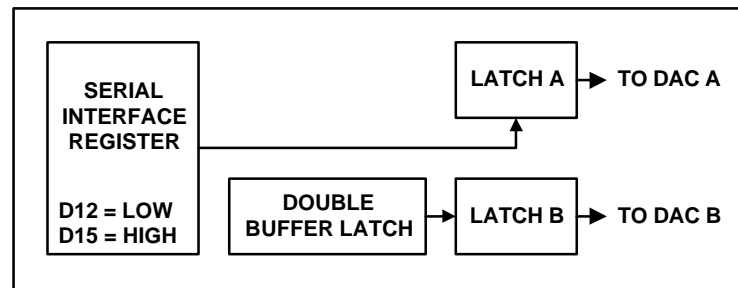


Figure 2 Latch A Write, Latch B Update

LATCH B AND DOUBLE BUFFER 1 WRITE (D15 = LOW, D12 = LOW)

The SIR data are written to both latch B and the double buffer. Latch A is unaffected.

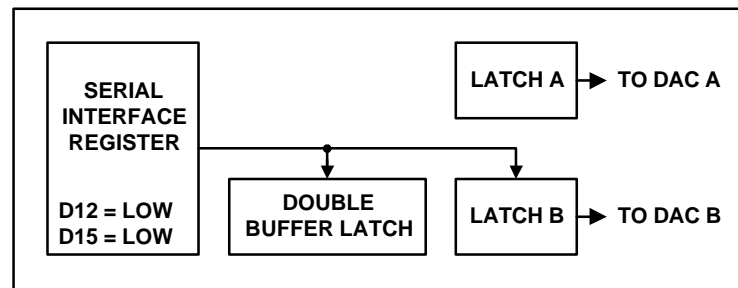


Figure 3 Latch B and Double Buffer Write

DOUBLE BUFFER ONLY WRITE (D15 = LOW, D12 = HIGH)

The SIR data are written to the double buffer only. Latch A and B contents are unaffected.

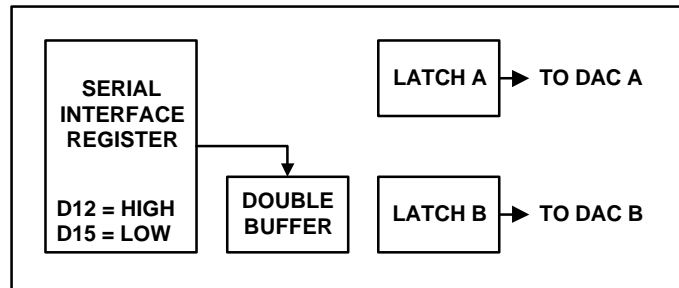


Figure 4 Double Buffer Only Write

OPERATIONAL EXAMPLES

1. changing the latch A data from zero to full code

Assuming that latch A starts at zero code (e.g. after power up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

```
1X00 1111 1111 1111
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode.

The latch B contents and DAC B output are not changed by this write unless the double buffer contents are different from the latch B contents. This can only be true if the last write was a double buffer-only write.

2. changing the latch B data from zero to full code

Assuming that latch B starts at zero code (e.g. after power up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

```
0X00 1111 1111 1111
```

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The data (bits D0 to D11) are written to both the double buffer and latch B.

The latch A contents and the DAC A output are not changed by this write.

3. double buffered change of both DAC outputs

Assuming that DACs A and B start at zero code (e.g. after power up), if DAC A is to be driven to mid-scale and DAC B to full-scale, and if the outputs are to begin rising at the same time, this can be achieved as follows:

First,

```
0d01 1111 1111 1111
```

is written (bit D15 on the left, D0 on the right) to the serial interface. This loads the full-scale code into the double buffer but does not change the latch B contents and the DAC B output voltage. The latch A contents and the DAC A output are also unaffected by this write operation.

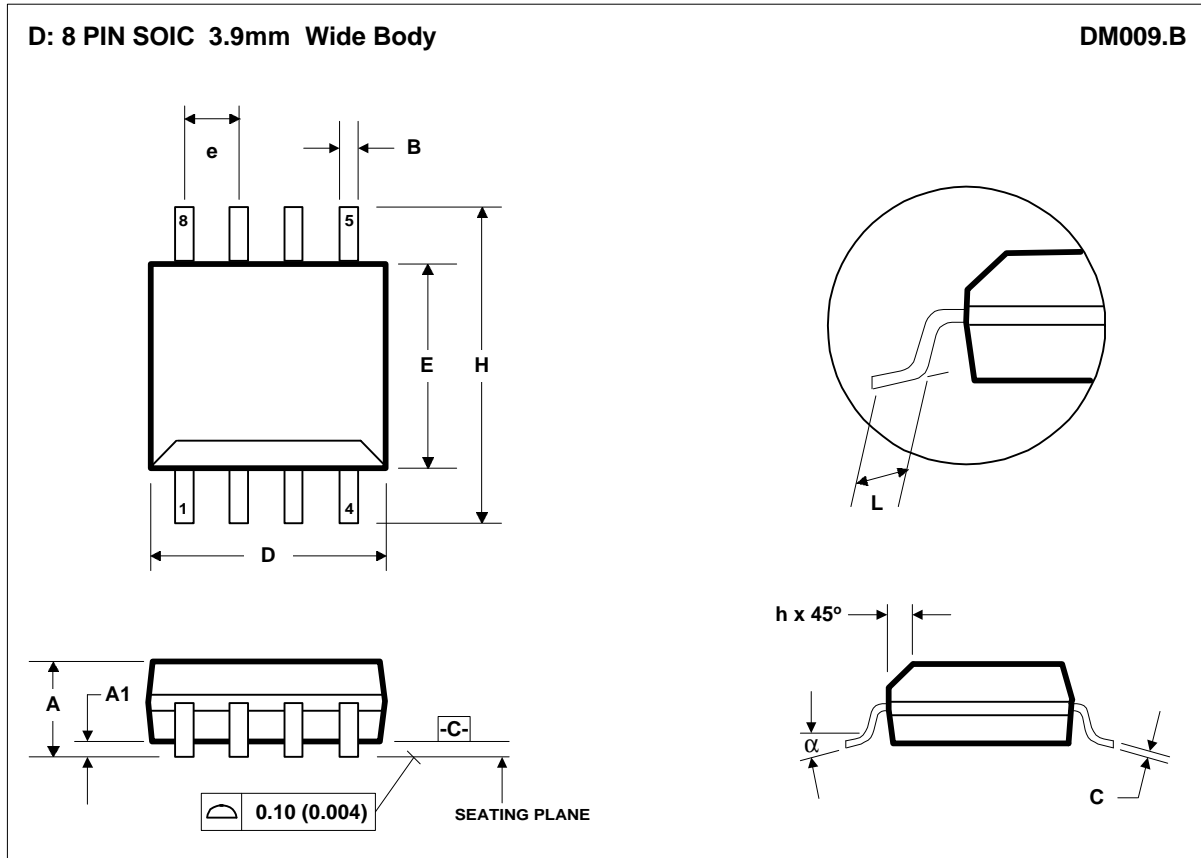
Changing from fast to slow to fast mode changes the supply current which can glitch the outputs, and so D14 (designated by d in the above data word) should be set to maintain the speed mode set by the previous write.

Next,

```
1d00 1000 0000 0000
```

is written (bit D15 on the left, D0 on the right) to the serial interface. This writes the mid-scale code (100000000000) to latch A and also copies the full-scale code from the double buffer to latch B. Both DAC outputs thus begin to rise after the second write.

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | Dimensions (Inches) | |
|----------------|------------------|------|---------------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.0532 | 0.0688 |
| A ₁ | 0.10 | 0.25 | 0.0040 | 0.0098 |
| B | 0.33 | 0.51 | 0.0130 | 0.0200 |
| C | 0.19 | 0.25 | 0.0075 | 0.0098 |
| D | 4.80 | 5.00 | 0.1890 | 0.1968 |
| e | 1.27 BSC | | 0.050 BSC | |
| E | 3.80 | 4.00 | 0.1497 | 0.1574 |
| h | 0.25 | 0.50 | 0.0099 | 0.0196 |
| H | 5.80 | 6.20 | 0.2284 | 0.2440 |
| L | 0.40 | 1.27 | 0.0160 | 0.0500 |
| α | 0° | 8° | 0° | 8° |
| REF: | JEDEC.95, MS-012 | | | |

- NOTES:
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
 D. MEETS JEDEC.95 MS-012, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.